TECHNICAL MANUAL

GENERAL SUPPORT AND DEPOT MAINTENANCE MANUAL

TEST SET, NAVIGATIONAL COMPTUER-CONTROL INDICATOR AN/ASM-386 (FSN 6625-404-3280)

H E A D Q U A R T E R S , D E P A R T M E N T O F T H E A R M Y
FEBRUARY 1972

WARNING

Be careful when working with the 115-volt power connections. SERIOUS INJURY or DEATH may result from contact with these terminals.

CAUTION

This equipment contains highly sophisticated, complicated circuitry. Maintenance personnel should not attempt any maintenance without reading and fully understanding the applicable section relating to that maintenance.

TECHNICAL MANUAL
No.11-6625-2441-45

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., 18 February 1972

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NOTE

This volume contains chapters 1 through 5 and appendixes A and B. Wire lists, appendix C, are contained in TM 11-6625-2441-45-2.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual covers general support and depot maintenance procedures for Test Set, Navigational Computer-Control Indicator AN/ASM386 (test set). Circuit analyses, troubleshooting and removal and replacement, and testing procedures are also included. The complete manual consists of three manuals. TM 11-6625-2441-45-1 contains the introductory data, principles of operation, maintenance chapters, list of references, and the program listing; TM 11-6625-2441-45-2 and TM 11-6625-2441-45-3 contains the wire lists.

b. Publications that complete coverage for this equipment include three other manuals: TM 11-6625 2441-12, Operator's and Organizational Maintenance Manual; TM 11-6625--2441-20P, Organizational Repair Parts and Special Tools List; and TM 11-6625-2441-45P, General Support and Depot Maintenance Repair Parts and Special Tools List.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

NOTE

Applicable forms and records are covered in TM 11-6625-2441-12.

1-3. Reporting of Equipment Publication Improvements

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commanding General, U.S. Army Electronics Command, ATTN: AMSEL-MA-AN, Fort Monmouth, N.J. 07703.

CHAPTER 2

PRINCIPLES OF OPERATION

Section I. BLOCK DIAGRAM ANALYSIS

2-1. General

The test set processes and distributes signals necessary to test navigational computers and control-indicators, and to perform a self-test operation. The processing operation is controlled by data received from the tape reader. The test set uses tape data and data from the unit under test to perform specific routines as required by particular tests. The relationship of Logic Control Unit TS-2912/ASM-386 (LCU), Signal Conditioning Unit TS-2913/ASM-386 (SCU), tape reader, and Adapter, Self Test MX-8586/ ASM-386 (self-test adapter) is illustrated in figure 2-1. The functions of the LCU, SCU, and self-test adapter are discussed in the following subparagraphs. Reference designations for the LCU, SCU, and self-test adapter are 1A1, 2A1, and 3A4 respectively. All subassemblies of these units are prefixed with the unit designation.

a. LCU. The speed and direction of the tape reader drive are determined by control signals received from the LCU. The tape reader applies tape data to the LCU where the type of data is determined and processed accordingly. The processed data is used in the LCU and is applied to the SCU and self-test adapter or the unit under test. Power for operation of the LCU is provided by the SCU. Test data indicating a go or no-go condition of the unit under test, or the test set, is received from the SCU. The condition of the test data is displayed in the LCU front panel displays and indicators and, when so indicated, to the tape reader as a stop or rerun signal. The control-indicator signal and power supply voltages are applied through the LCU to the SCU. The power supply voltages are connected to the external monitoring equipment (oscilloscope and digital voltmeter) and the signals are processed and returned to the LCU for display. Clock

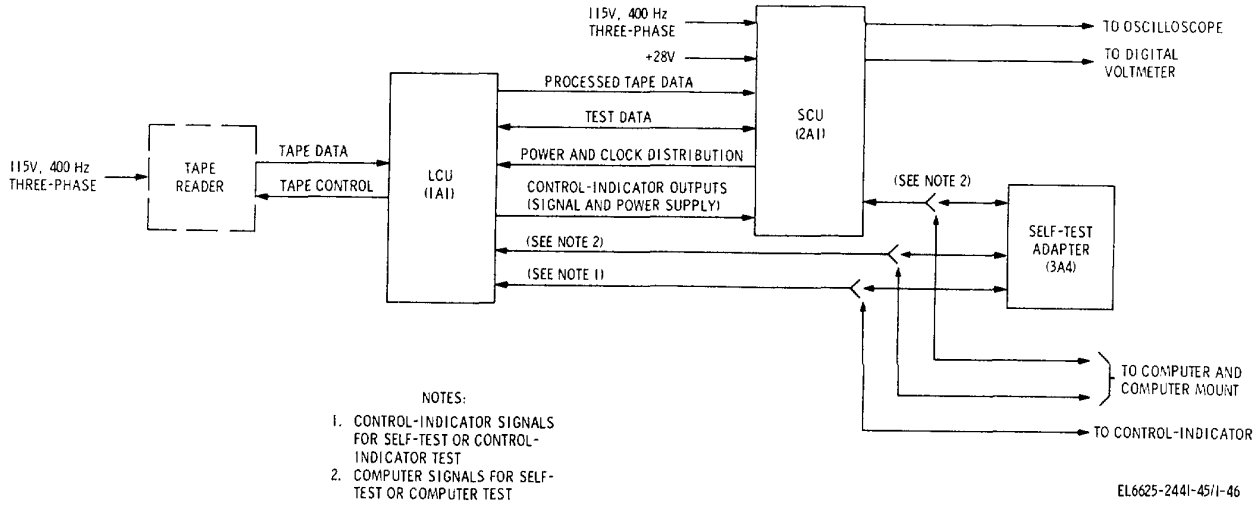


Figure 2-1. Test Set, Navigational Computer-Control Indicator AN/ASM-386, block diagram.

signals required for operation of the test set are generated in the LCU and distributed to the SCU, and to the unit under test upon demand.

b. SCU. The SCU receives 115 Vac and +28 V primary power and distributes operating voltages.

Connection of the navigational computer, control indicator, and test set voltages to external monitoring equipment is provided through front panel POWER MONITOR switch. Processed data from the LCU which requires further modification is processed in the SCU and applied to the unit under test. Processed data is also used by the SCU, in conjunction with data from the unit under test, to perform various test routines. Test data signals are applied to the LCU for processing go/no-go indications.

c. Self-test Adapter. The self-test adapter is used to provide continuity of signals between the LCU and the SCU during self-test of the test set.

Resistors in the self-test adapter provide loads for signals as required.

2-2. Test Set, General Description
(fig. 2-2)

a. Interface. The test set dynamically simulates any signal which a computer or control indicator normally sees during system operation. Each computer or control-indicator input and output is analyzed for correctness against the known correct respective output or input stored on the program tape. Organization of the computer external avionics subassemblies servicing program enables the test set to simulate only one of these external avionics systems at a time, which greatly minimizes the test set complexity.

b. Major and Minor Tests. The tape program is made up of major and minor test routines. Each major test can have a maximum of 100 minor tests. A major test is usually associated with a major function of the test sets, computer, or control-indicator. The program is organized on a test priority level; the most important functional areas are analyzed first. With the computer, the test set exercises the computer memory fill and read electronics first. Once the test set has established that the memory and associated computer electronics are in working order, the program loads many operational subroutines into the computer memory for use in subsequent fault-diagnostic programs.

(1) Each test routine does not necessarily yield a definite result which leads directly to the faulty assembly. In some cases, the faulty assembly must be determined through deductive test techniques. In this technique, the operator selects the next test number by referring to the appropriate maintenance manual. The operator uses this manual by finding the page associated with the major or minor test number displayed on the LCU panel. Here the test result which compares with the test result displayed on the LCU panel is selected. Associated with the selected test result are instructions which give direction for the fault-diagnosis procedure.

(2) Each major functional requirement of the test set, computer, and the control-indicator is assigned a major test number. The test set is capable of handling 100 major test numbers.

Each major test is subdivided into minor tests (1 up to 100). The TEST NUMBER/MAJOR, MINOR indication is the basis of correlation between the program tape and the appropriate maintenance manual.

c. Program Tapes. All programs essential for maintenance of the test set, computer, and control-indicator are provided by tapes. Each tape is programmed to include the functions that simulate the related equipment of the unit under test. The computer tape contains data that simulates the signals (input and output) of the appropriate associated avionics. The control indicator tape is programmed to simulate input and output signals that interface with the control indicator in normal system applications. Self-test, tape includes functions which are required to exercise portions of the computer and control indicator.

(1) *Computer tapes.* Computer test and diagnostic operations are programmed for both test set and computer control. The computer memory is filled with a diagnostic program, which is verified in the test set by direct, comparison, then used to test and fault isolate computer circuits. Analog portions of the computer are exercised by digital data from the tape that is converted to analog signals in the test set. Additional tapes may be used to fill the computer memory with operational programs.

(2) *Control-indicator tape.* The control indicator tape provides data that is converted in

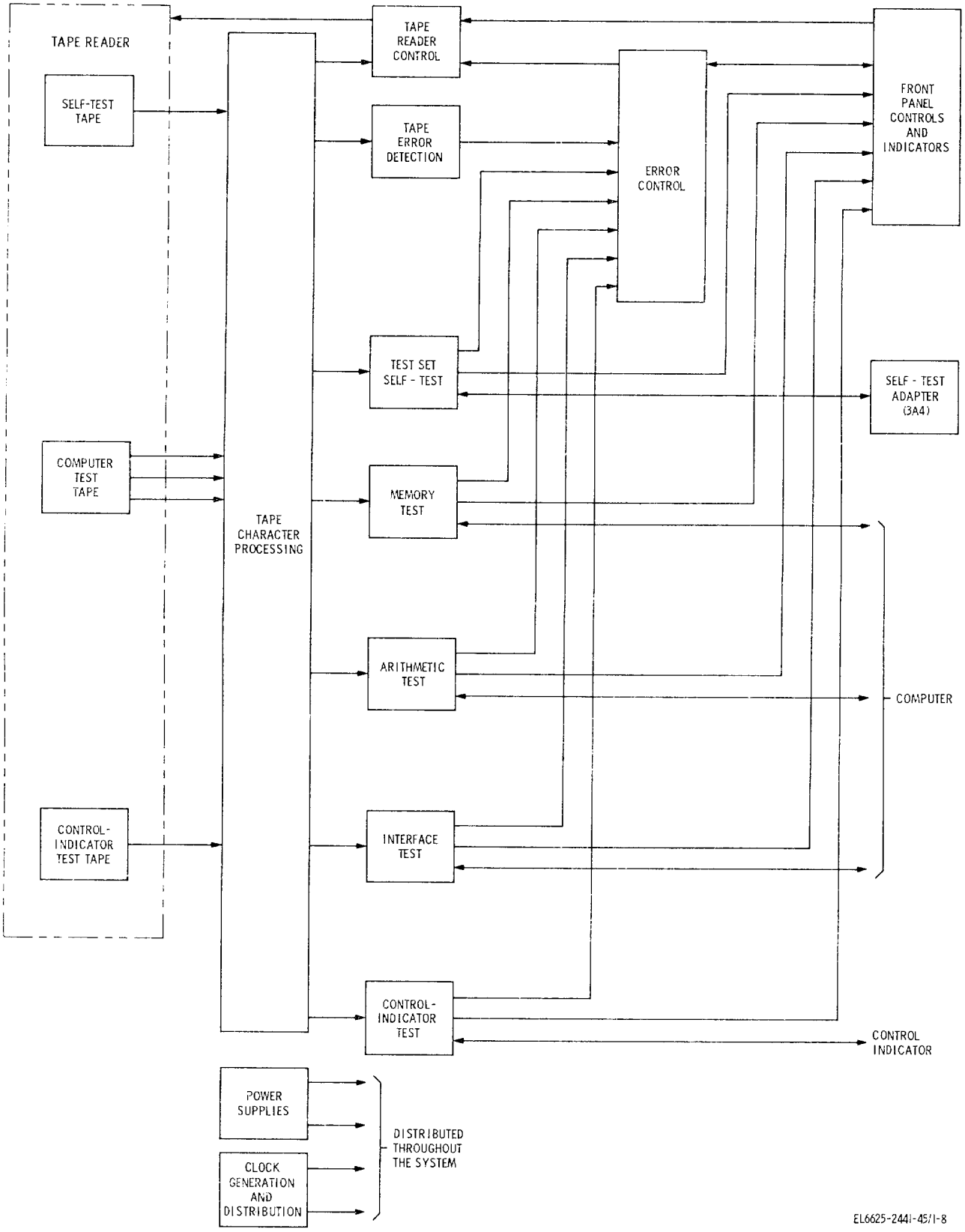


Figure 2-2. Test Set, Navigational Computer-Control Indicator AN/ASM-386, Functional block diagram.

the test set to simulate input and output signals.

The majority of the control-indicator tests require visual monitoring of control-indicator panel indicators and manipulation of control-indicator panel controls. Predetermined data generated by the control-indicator is compared with tape data in the test set. Results of these comparisons are displayed on test set front panel indicators.

(3) *Self-test tape.* The self-test tape thoroughly analyzes the units of the test set.

Data received from the tape reader is applied to the circuits of the test set where it is processed in much the same manner as under actual test operation. This data is then compared with additional tape data and the results are displayed on test set status indicators. Refer to paragraph 2-19 for a detailed description of the self-test tape application.

d. Power Control. The test set controls the primary power to the unit under test and the SCU power supply. All voltages generated by the computer or the control-indicator can be monitored by the test set.

2-3. Tape Reader Control

The tape reader is both manually and automatically controlled. Initially, the operator starts the tape reader and can stop it at any time. For a tape-search to a specific major test, the tape reader automatically seeks out the desired number and halts at that number. The location of the desired number, versus the tape location prior to search, has no effect on the ability of the tape reader to locate the number. The tape reader is normally under program control and requires a minimum of operator response after the program has been initiated. The tape reader is automatically controlled during memory fill and verify operation. After its initial start by the operator, the tape reader will automatically fill and rewind, then verify and rewind the operational program tape before halting. The tape reader, while under program control, may be controlled manually. For test set maintenance, the tape reader can be single stepped by using the test panel controls.

2-4. Error Detection and Control

The test set error detection consists of comparing the output of the unit under test against the 2-4 correct output value provided by the tape. A bit-by-bit comparison takes place; the location of the bits in error are stored in an error register. The contents of this error register are displayed to the operator upon conclusion of the fault analysis. The information displayed on the TEST STATUS REGISTERS display (TM 11-6625-2441-12) is used in conjunction with appropriate maintenance manual for further maintenance instructions. The test set monitors the contents of the error register looking for a non-zero condition. When a 1 appears in the error register, indicating that an error has occurred, the no-go flag (flip-flop) is set. The test set reacts to this no-go state under program control which may or may not halt the fault analysis immediately.

2-5. Error Display

The TEST STATUS REGISTERS display indicates the location of an error in a particular comparison result. Conversion of this error location into a maintenance instruction can be found in the appropriate maintenance manual. The converted information reveals the probable functional area that contains a malfunction.

2-6. Self-Test

Two methods of testing the test set are provided; one method is through the use of a self-test tape that is programmed to exercise all the electronic stages. Another method is the monitoring of key areas of the test set during checkout of the computer or the control-indicator.

a. Programmed Tape, Self-Test. The test set is furnished with a self-test program tape. The tape is used to determine the operational status of the test set. Under the tape program control, the test set analyzes its own outputs, conversion and comparison techniques, and control processes.

b. In-Process Self-Test. The in-process self-tests monitor control and interpretation circuits for disallowed states. Another area of in-process tests monitors the manipulation of data within the test set. Each data word is sensed for saturation to insure that no errors are introduced into the data by the test set. A third form of in-process testing involves the processing of information read from the tape. Here the test set monitors the transfer of data from the tape through horizontal and

vertical parity bits, The test set also checks the tape for format errors. Each tape must be generated following a strict set of format rules. The test set checks whether or not the tape has been correctly generated.

2-7. Computer Memory Test

An operational tape is used to fill the computer memory with a block of words (1,024 words maximum). The words are read back from memory and compared with the contents of the tape to ascertain the operational validity of the computer memory and the associated electronics. In the process of checking the memory, memory address (NIA) register and memory buffer (MB) register are also checked. A discrepancy in the comparison causes a no-go flag to be set and the fault is displayed on the LCU front panel.

2-8. Computer Arithmetic and Control Logic Test

To test the arithmetic and control functions of the computer, data is loaded from the test tape into memory. The data consists of subroutines that test the arithmetic and control logic counters and registers. Two methods are used for detecting malfunctions. One, the computer is programmed to detect errors in the arithmetic and control logic counters and registers. The test set in this case is a passive element only and waits for the computer to indicate an error. The test set is then programmed to perform certain routines to isolate the malfunction to a specific area in the computer. Another method for testing the validity of the computer counters and registers is to load known tape data into an individual or a group of registers, then read and compare the contents of the registers with the known tape data. Any discrepancies in the comparison are displayed on the LCU front panel.

2-9. Computer Interface Test

The computer interfaces with various avionics (platform, control-indicator, etc) in the navigation set. To check the computer's interface operational capabilities, the test set can supply and receive from the computer, signals associated with each avionic equipment under program control. With the test set simulating the avionics, each area of the computer interface is checked out. Input signals to the computer are the EIP signals, and outputs from the computer are the EOP signals.

a. EIP, EOP Digital Simulation. The test set is capable of simulating all digital inputs required by the computer. The Lest set uses several data registers which, under program control line multiplexing, store the computer digital outputs. The data is then compared with the known correct tape output for fault analysis.

b. EIP, EOP Analog Simulation. The procedure for testing the analog circuits in the computer are as follows:

(1) Test signals of known amplitude, both ac and dc, are generated in the test set, and applied to the appropriate input channel of the analog-to-digital converter of the compute,, and the digital output is processed arid compared with the known input. A no-go condition indicates a malfunction in the digital-to-analog converter of the computer with fault isolation to two trays.

(2) Assuming a go condition at (1) above, the digital-to-analog converters in the computer are then addressed to generate an output signal (ac and dc). These signals are properly scaled in the test set and routed back into the computer through the channels previously tested in (1). A no-go at this point indicates a failure in the particular digital-to-analog channel addressed with fault isolation to one tray.

(3) The synchro outputs from the computer are routed to synchro termination networks in the test set in parallel with the synchro inputs to the computer. The synchro output channels of the computer are then addressed to generate an output angle. The sine and cosine outputs from the synchro termination networks are then switched into the ac channel tested in (1), and the output angle verified. A no-go indicates a failure in that particular synchro output channel with fault isolation to one tray.

(4) Assuming a go condition from (3) above, a three-wire synchro signal is applied to the test set and then back through the computer synchro-to-digital channel. A fail to compare in the computer indicates a malfunction in that particular channel of the synchro-to-digital converter with fault isolation to one tray.

(5) Discrete outputs and inputs to the computer are made T2L compatible and are exercised as required through control logic in the test.

2-10. Application of Power

The test set controls not only its own power sequencing but that of the unit under test also. The final turnon control for both the test set and the unit under test (computer or control indicator) is located on the LCU. The computer turnon is interlocked so that computer primary power cannot be turned on until the cooling air blower, located on the computer mounting fixture, is functioning.

Section II. DETAIL CIRCUIT ANALYSIS

2-11. Memory Fill and Verify
(fig. 5-3)

The memory fill and verify test routine exercises the computer memory write and read electronics to determine the functional validity of the memory and its associated controls and registers. Under tape program control, a memory sector (with storage capacity of 1,024 words) is filled with data supplied by the test set tape. The content of the memory is then read back and compared with the original tape data. If no errors exist, the memory is functioning properly. The presence of an error stops the tape and the error is displayed. Interpretation of the display and the necessary corrective action are provided in the appropriate maintenance manual. An overall description of the fill and verify function and a timing analysis of the modified fill and verify function follow.

a. Memory Fill, General Description. After the front panel switches have been initialized, the tape reader moves to a selected tape address and then continues on to a memory fill (MFIL) instruction. The memory fill instruction is decoded after processing, and the decoded bit initiates control logic for tape movement and memory register loading. The first data from the tape is the memory address, indicating where in memory the first data will be loaded. Tape memory data is loaded into the A-register, and tinder memory fill control shifts the memory address into the computer program counter (CP) register. The A-register is then cleared. The tape follows with a data word, which is stored in the A-register and parallel loaded into the computer memory buffer (MB) register. A clear-write memory cycle is initiated to write the MB register data into the location specified by the CP register. The CP register is then at increment one count, another data word from the tape enters the A-register and is loaded into the MB register. Another memory cycle is initiated and the data written at the new location specified by the CP register. The CP register is incremented another count. The operation continues until a stop fill instruction is provided by the tape.

b. Memory Verify, General Description. During memory verify, the memory verify instruction is generated, providing a bit for initiating the control logic. Memory verify is initialized when the memory fill instruction has been executed in the auto mode, the end of the tape has been reached, and the MEMORY switch is set to VERIFY. Memory verify is also initialized when in the major mode and memory fill has been executed for the selected major address. Following the memory fill, memory verify is executed for the selected major address. During memory verify, following the loading of the A-register from tape, a read-restore cycle is initiated transferring memory data into the MB register. The contents of MB register are loaded into the test set B-register and compared to A-register data. Following the compare, a second read-restore is initiated to verify the first read-restore operation. The contents of MB register are loaded into the B-register; a second comparison of A- and B-registers is performed and the results are stored in the C-register, A 1 in the C-register indicates an error for that bit comparison. The C,P register is loaded in the display multiplexer, ready for display as the current memory address. If a failure to compare occurs, the no-go flag is set and the tape stops. If the STOP/RESET push-button is pressed, the C-register is displayed showing the results of the comparison. At any other time, the CP register bits in the display multiplexer are displayed providing a read-out of the faulty memory address. If the comparison is good, the CP register is incremented by one, new data is read into the A-register from tape, and a

new memory word is read and restored from memory to the MB register. The contents of MB register are loaded into the B-register and a comparison of A- and B-registers performed. The cycle continues until a stop memory fill (SMFL) instruction is encountered.

c. Memory Fill and Verify, Timing Analysis.

The following paragraphs detail the sequential timing analysis of the memory fill and memory verify functions.

(1) Memory fill, timing analysis. Depending on front panel switch settings, the desired tape address is found either through a tape search, when the MODE switch is at MAJOR or MINOR, or the tape starts at address 00. Following the tape address character, a memory fill instruction character is detected. The second character of the memory fill instruction (fig. 2-3), when entered into the instruction register, is decoded along with the first instruction character to provide the memory fill instruction bit time (IBT). The IBT pulse sets a fill-verify flip-flop indicating a memory fill function and activates the clear-write function of memory. Following the instruction word, the tape provides a data word of four characters that contains the memory start address. Following the start address, an end-of-data character is provided by the tape. The test set senses the end-of-data character and generates a signal clearing the computer CP register and the memory cycle (CM) register. At the next clock time, the CM register is loaded with a count of 8 to establish the eight-step sequence for loading the memory, and the CP register is loaded with the memory address to provide the computer logic with the first loading address in memory. When CM and CP registers have been loaded, the initialization complete flip-flop is set. The tape puts out a data word consisting of one to seven characters, depending on program design, which is stored in the A-register. An end-of-data character appears at the end of the data word. The control logic generates a load MB pulse when the four data bits of the end-of-data character have been sensed (reset D). Data from the A-register is then loaded into the MB register. A memory interleave pulse and a clock control pulse are generated at the same time, causing the computer to write the contents of the MB register into memory a' the address specified by the CP register. The CM register provides an eight-bit count for the memory-loading procedure. After loading the memory, the CP register is incremented one count for the new memory address, and the fill instruction cycle starts again. This process continues until a stop memory fill instruction is received. In either case, a verify mode may be entered to verify the data written in memory.

(2) Memory verify, tinning analysis. A memory verify mode results from either of the following conditions. The MODE switch is at AUTO, the MEMORY switch at VERIFY, and memory verify IBT, or the MODE switch is at MAJOR, the MEMORY switch at VERIFY, an>] stop memory fill IBT. In the firs-t condition, the complete tape is read into memory. At the end of the tape, a verify instruction is read forcing the tape to reverse direction to its beginning (address 00) and the verify procedure starts. When the tape reaches the end, a verify instruction is read a second time; the tape again reverses direction to its starting address, but this time the tape movement halts. In the second condition, if the MEMORY switch is set to VERIFY, the fill and verify process will only check the selected major address. After reading and decoding the memory verify instruction, four characters are read from the tape to providethe memory address and are loaded in the CP register. Data characters from the tape are then loaded into the A-register. The end-of-data character (fig. 2-3), due to the verify instruction, will inhibit loading the MB register (QTC13* true) and inhibit the clear-write command (QTC21*), providing a read-restore memory command to the computer. A memory interleave and a clock control pulse initiate the read-restore memory function by loading the memory data into the MB register. The CP register is not incremented at this time because two read-restore and compare cycles are completed for each memory data word. On the second read and compare, the CP register is incremented. When the read MB and read MA/ pulses are generated, data from MB register is shifted into the B-register and the MA register data shifted into the display multiplexer of the test set. The data stored in A-register is compared with the data stored in B-register on a bit-by-bit basis and the results are stored in the C-register. If comparison is good, the whole procedure of read-restore and compare is repeated for the new memory address stored in the incremented CP register. This process is continued until a stop memory fill instruction is decoded. If a compare error is sensed, a tape stops and the memory

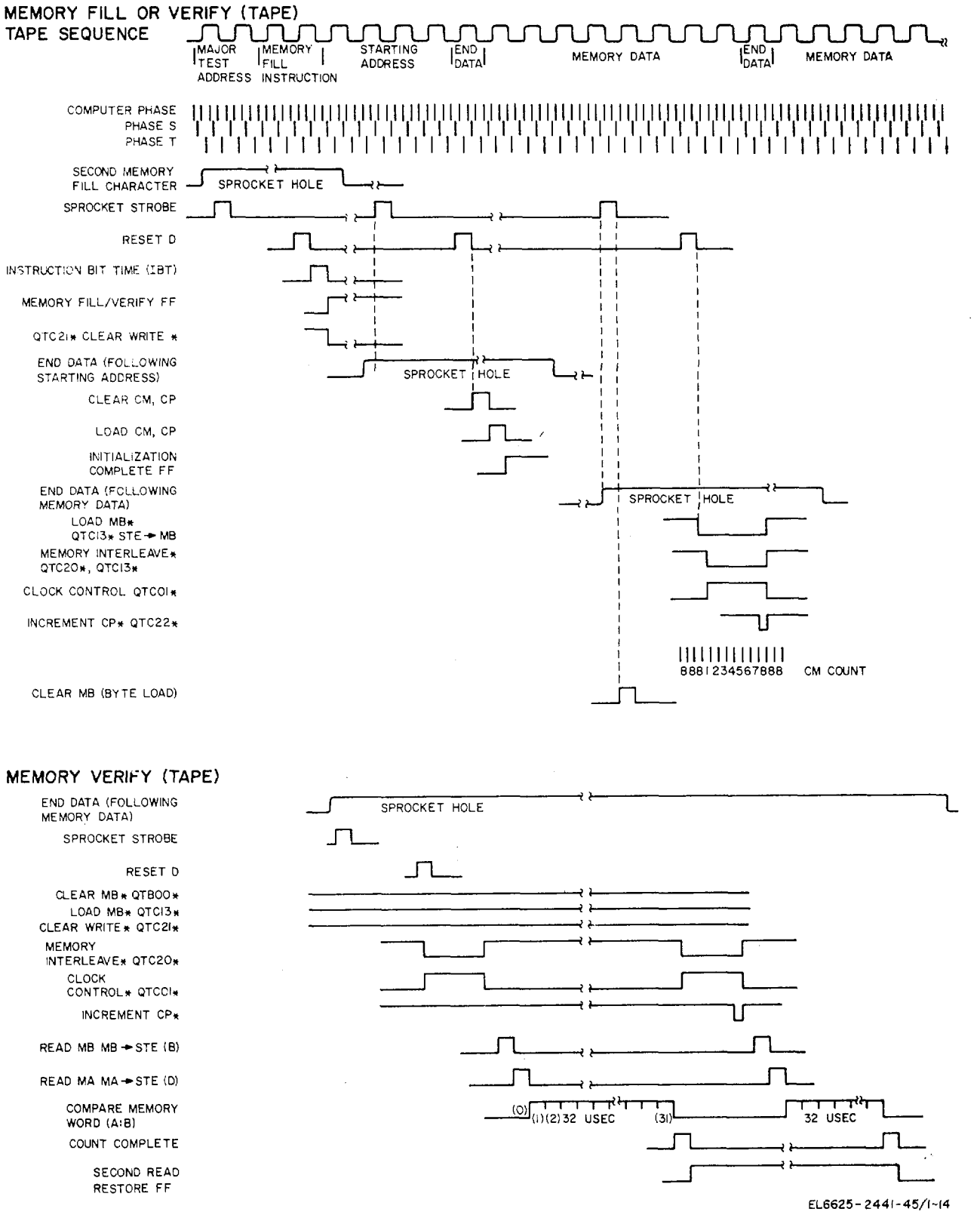


Figure 2-3. Memory fill and verify, timing diagram.

address is displayed; pushing the STOP/RESET button displays the C-register, showing which bit failed. During a memory verify cycle, an error could be a result of either an incorrect memory verify or an incorrect test instruction result both results are displayed.

d. Worst Case Fill and Verify, Timing Analysis (fig. 2-4). The worst case memory fill and verify check is performed when the computer test tape is mounted in the tape reader. An instruction, load and verify worst case memory test, is decoded generating an IBT pulse which sets the worst case memory test (WCMT) flip-flop. After the second instruction character from tape, the memory starting address from tape is placed in the A-register. An end-of-data strobe occurs at the end of the memory address. The CM and CP registers are cleared, and at the next clock pulse, the CP register is loaded with the contents of the A-register (memory address) and the CM register is loaded with a count of 8 in preparation for a memory cycle. Initialization is now complete. The worst case memory data word is then read from tape and stored in the A-register. The worst case memory data word is programmed as an alternating 1-0 pattern. Following the end-of-data character, the tape reader is stopped and not used again until the worst case memory test is concluded. The A-register data is loaded into the MB register and the clear-write operation proceeds in the same manner as described in b above. On the next memory write cycle, instead of new data being read from tape, the A-register is right shifted (end around) one bit to provide new data contents to the A-register. A clear-write cycle is initiated and the new data is stored in memory and the new incremented CP address. Similar operations continue until the ten low-order bits of the CP register are saturated signifying that a 1,024-word sector in memory has been loaded. A saturated CP register (count of 1023) will set up the memory verify mode. Verification of the loaded data now begins. The CP register is cleared (CP = 0) and the clear-write flip-flop (QTC21*) is set indicating a read-restore command. Read MB and read MA pulses are generated shifting the MB register contents into the B-register and the MA contents to the display multiplexer. The A- and B-registers are compared. A second read-restore cycle is initiated to check the first restore and is then followed by a compare. If any compare fails, the no-go flag is set and remains set. Following the two comparisons, the CP register is incremented one count by resetting QTC22* for one clock period. The A-register is shifted right one bit and a verify cycle is started once again. The cyclic action continues until the CP counter reads 1023. During this cycle when the second read and compare has been established, the CP register is incremented to 0, worst case mode test flip-flop reset (the end worst case test flip-flop had been set during CP = 1023 and reset during CP = 0), and a restart tape reader pulse generated. The tape reader is restarted and the program checks, via a branch instruction, whether the no-go flag was set.

e. Single Load and Single Read Memory, Timing Analysis. The program provides the capability of either writing a single word in memory from A-register (SLMA) or from the C-register (SLMC). The program also provides the capability for reading out a single word from memory (SREM) at the specified address. Procedural steps for accomplishing a single loading are the same as for a fill cycle except the tape halts after the first word has been written in memory (fig. 2-5). To write in memory from the A-register, the SLMA instruction causes the memory address to be loaded into CP register. Simultaneously, the CM register is filled with a count of 8 in preparation for a memory cycle. A second operand (following the memory address) may follow. In any case, whether the A-register is loaded from tape or not, and end-of-data bit following the second data word will initiate loading of the MB register from the A-register. A clear-write cycle is initiated by memory interleave (QTC20*) and clock run (QTCO1*) to write the data into memory location specified by the CP register. The CP register is incremented completing the cycle. For writing in memory from the C-register, the SLMC instruction causes the memory address to be loaded in the A-register and then in the CP register. Simultaneously, the CM register is loaded with an 8 in preparation for a memory cycle. Following end-of-data character for the memory address, the data word from tape is loaded into the C-register. A second end-of-data character loads the data from C-register to the MB register. A clear-write memory cycle is initiated to write the data into the memory location specified by the CP register. An SREM instruction is initiated when the instruction is sensed and decoded. The memory address is loaded into A-register. When the first end-of-data character occurs, CP and CM registers

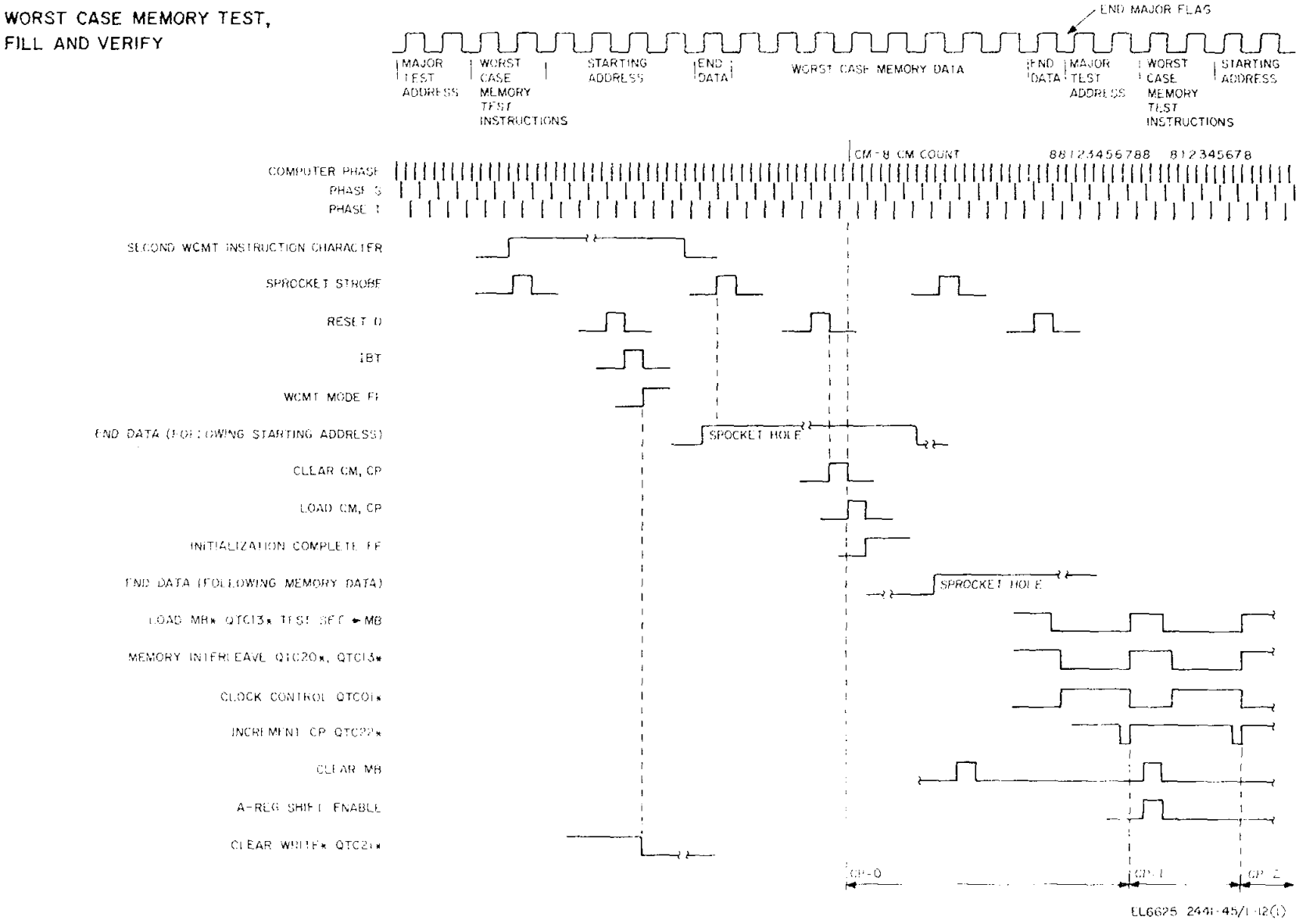


Figure 2-4 (1). Worst case memory fill and verify, timing diagram (part 1 of 3).

WORST CASE MEMORY TEST, FILL AND VERIFY

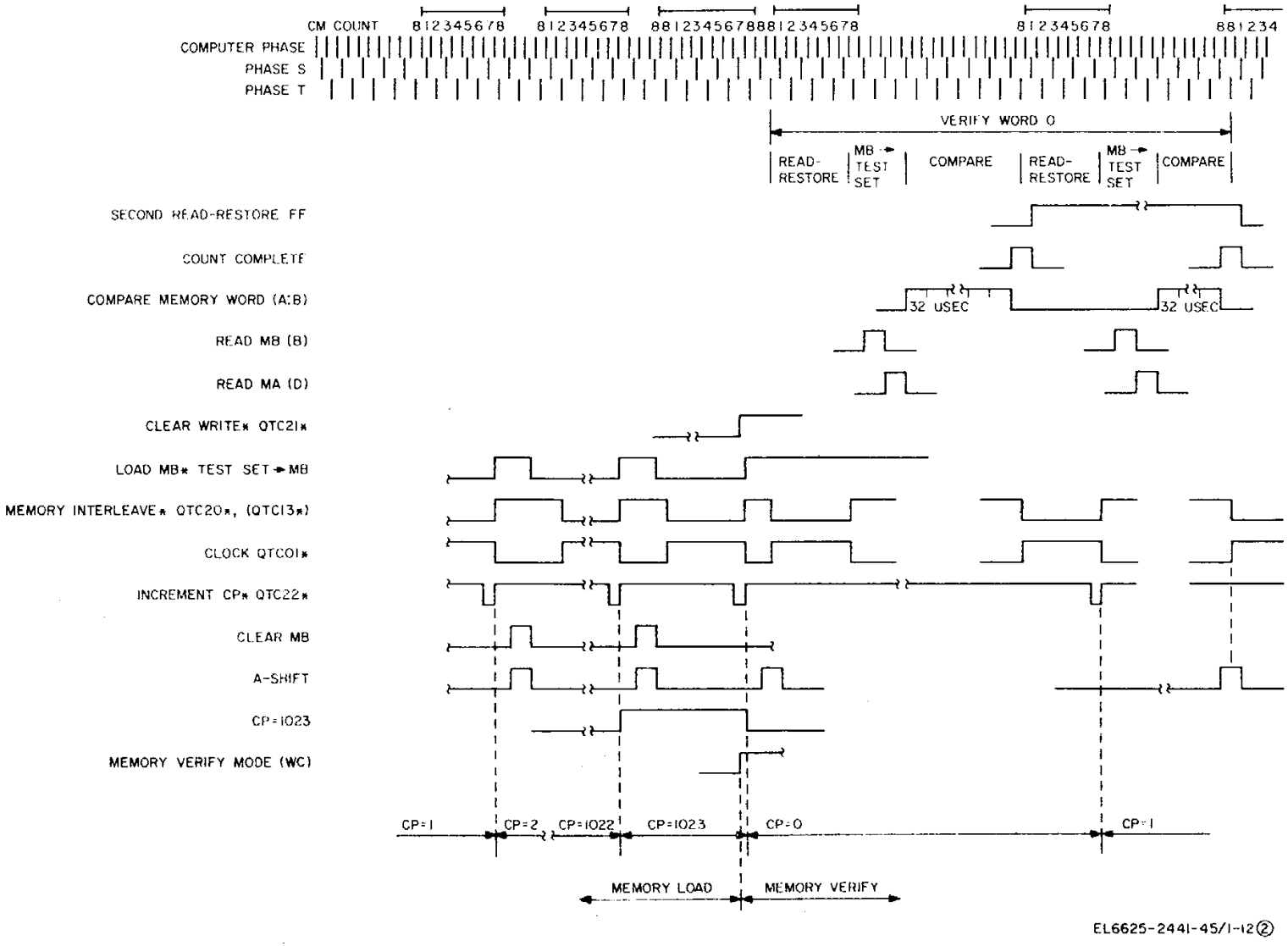


Figure 2-4 (2). Worst case memory fill and verify, timing diagram (part 2 of 3).

WORST CASE MEMORY TEST, FILL AND VERIFY

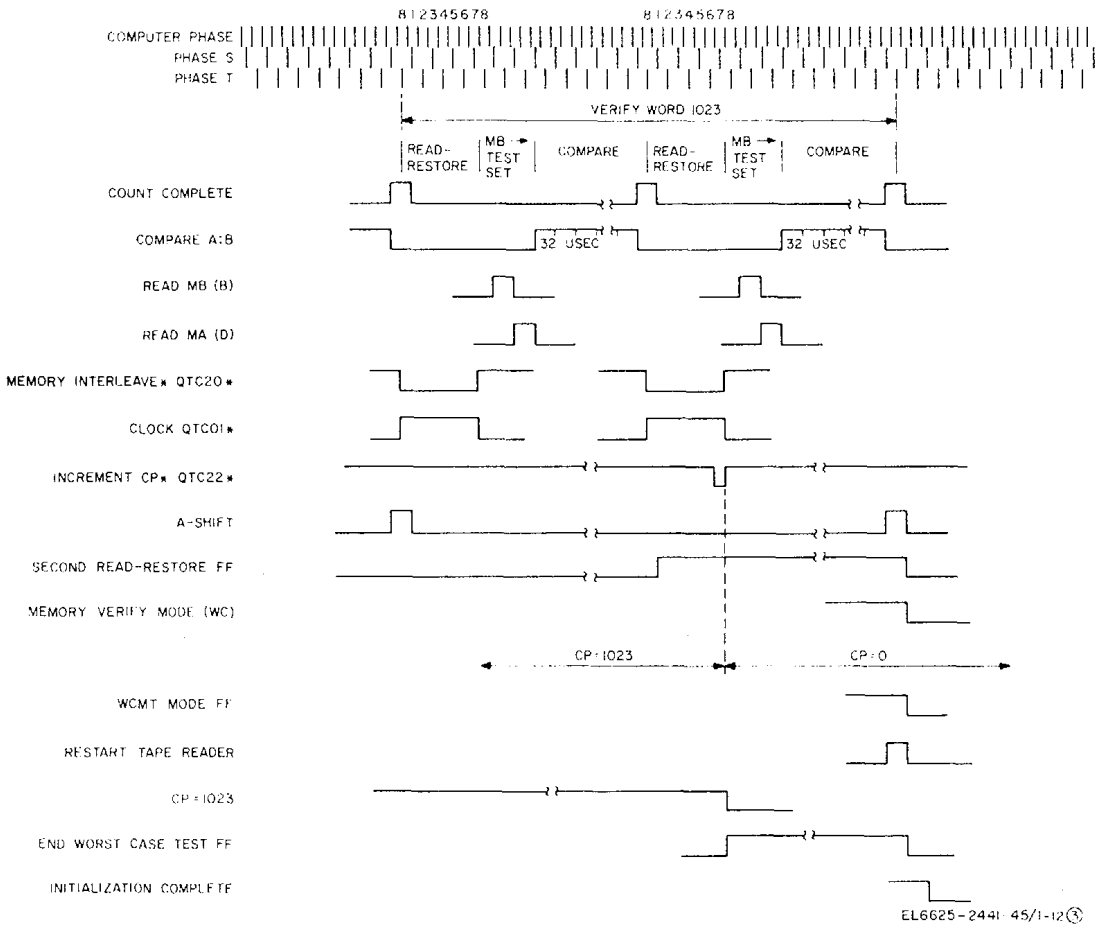


Figure 2-4 (3). Worst case memory fill and verify, timing diagram (part 3 of 3).

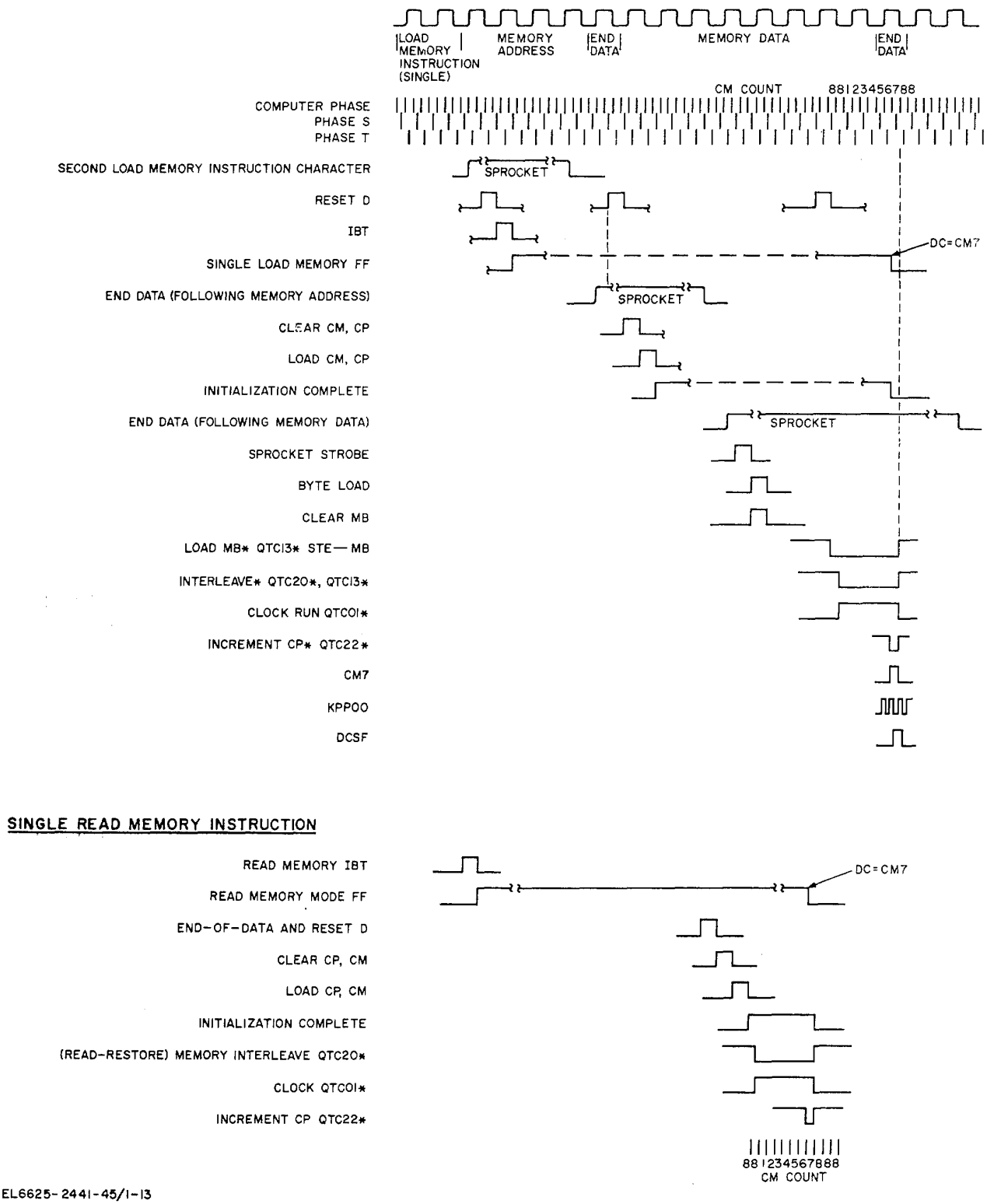


Figure 2-5. Single instruction memory fill and verify, timing diagram.

are cleared, and on the next clock pulse CP register is loaded from the A-register and CM register filled with a count of 8. A read-restore signal and a clock pulse initialize the read-restore cycle, and the memory data from the address specified in the CP register is loaded into the MB register. The CP register is incremented one bit, completing the cycle.

2-12. Load and Read-Compare
(fig. 2-6 and 5-4)

The program provides for loading computer registers, either in groups or individually, with tape data to check the operational validity of specific registers. A read-compare instruction allows the contents of the selected computer register to be read and compared with the tape data. bit by bit. Any discrepancy in the compare generates a no-go flag and provides a display of the malfunctioning bit. The following subparagraphs describe the load and read-compare functions for the registers.

a. Load. Loading word no. 1 into the computer causes a particular routine to be performed, and the resultant output to be applied to the test set. Word no. 1 consists of the data loaded into

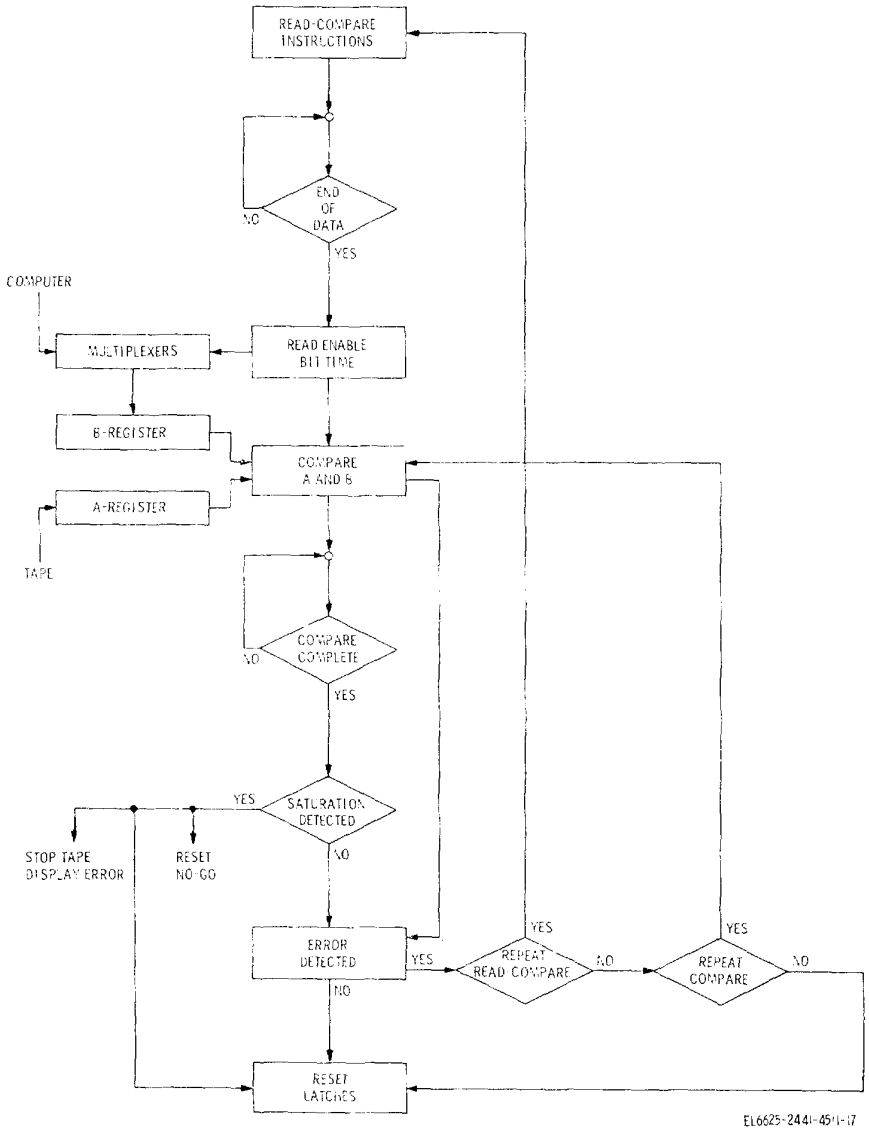


Figure 2-6. Read-compare program, flow chart.

the CA, CE, CI, and CP computer registers. These registers can be loaded in parallel or individually, depending on the data to be provided by the computer. Additional logic is provided for loading the CM and MB registers. These registers can only be loaded individually. Loading the MB register can be controlled by an instruction word, or the memory fill and verify operation (refer to para 2-11). This capability requires an MB register control logic circuit, through which the enable signals are applied. Logic is also provided to load and read-compare an additional computer memory unit (XMB), if a second memory unit should be installed. Loading is initiated by enabling the load control logic with an instruction word. The A-register is loaded with data from the program tape and the computer registers are cleared, enabling the drivers to load the selected computer register or registers with the contents of the A-register.

(1) The load control logic receives an instruction from the tape control and processing logic (para 2-20), to load either CA, CE, CI, CP, CM, NIB, XMB, or word no. 1. The load logic activated by this instruction is latched (fig. 2-7). The logic senses the presence or absence of the first data character from the tape. If tape data is present, the A-register is cleared and loaded with data from the tape. if tape data is not present, the existing A-register data is utilized.

(2) Control bits received from the tape control and processing logic, enables the register and A-register; clock signal. Data from the tape is loaded into the A-register in byte serial form, consisting of 1 to 7 bytes, depending on which computer register or registers have been selected. The contents of the A-register are parallel shifted to all computer register Livers through the register output multiplexer.

(3) Following the data word that loaded the A-register, an end-of-data pulse is applied to the load control logic. This causes a clear pulse to be applied to the computer, clearing the selected register or registers and enabling the driver logic for the selected register or registers. The enabled driver logic loads the data in the respective computer register, and the load latch logic is reset.

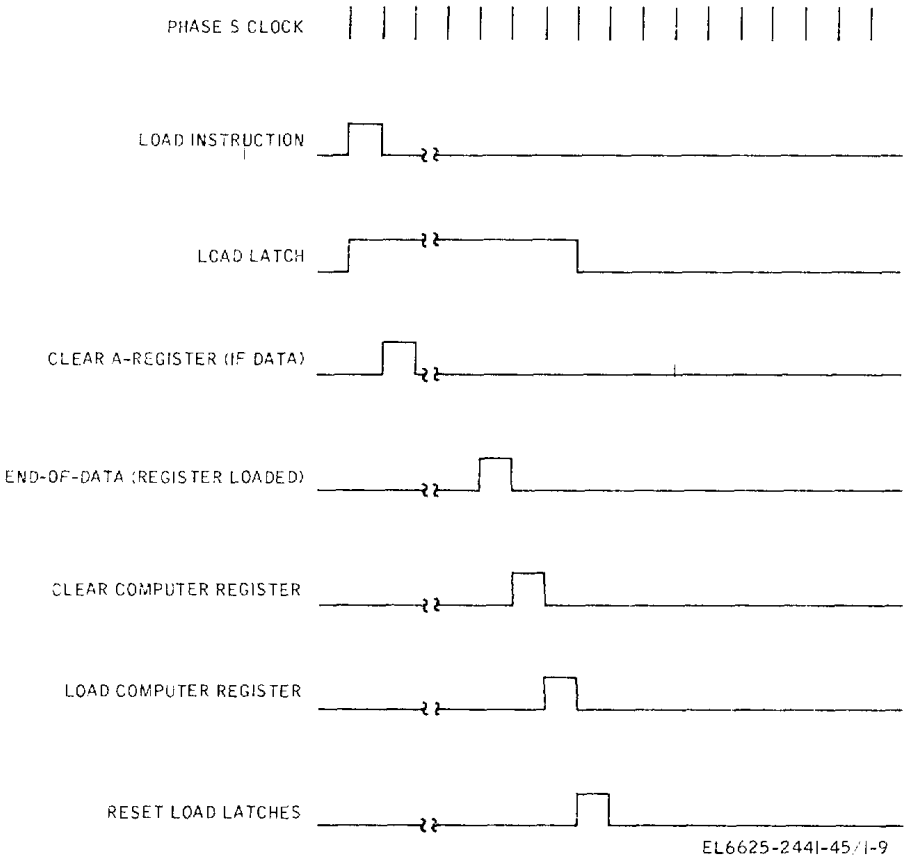


Figure 2-7. Computer register loading, timing diagram.

b. Read-compare. A read-compare instruction causes loading of computer data into the B- register and comparison with data in the A- register (fig. 2-7). The results of the comparison are applied to the C-register (fig. 2-8). If there is an error in the comparison, an automatic self-test routine is performed within the test set to determine whether the failure is due to a malfunction in the computer or the test set. Read-compare is initiated by enabling the read-compare logic with an instruction word. The A-register is loaded with data from the tape and the B-register loaded from the computer; the A- and B-registers are bit shifted to the comparator and the results of the comparison are stored in the C-register.

(1) The read-compare logic receives an instruction from the tape control and processing logic to read-compare a particular computer register or word. The read-compare logic activated by this instruction is latched. The logic senses the presence or absence of the first data character of' the tape. If tape data is present, the A-register is; cleared and loaded with tape data. If tape data is, not present, the existing A-register data is, utilized.

(2) Data is loaded into the A-register in the same manner as in a(2) above. The data conlsists3 of 1 to 7 bytes, depending on the register or word selected.

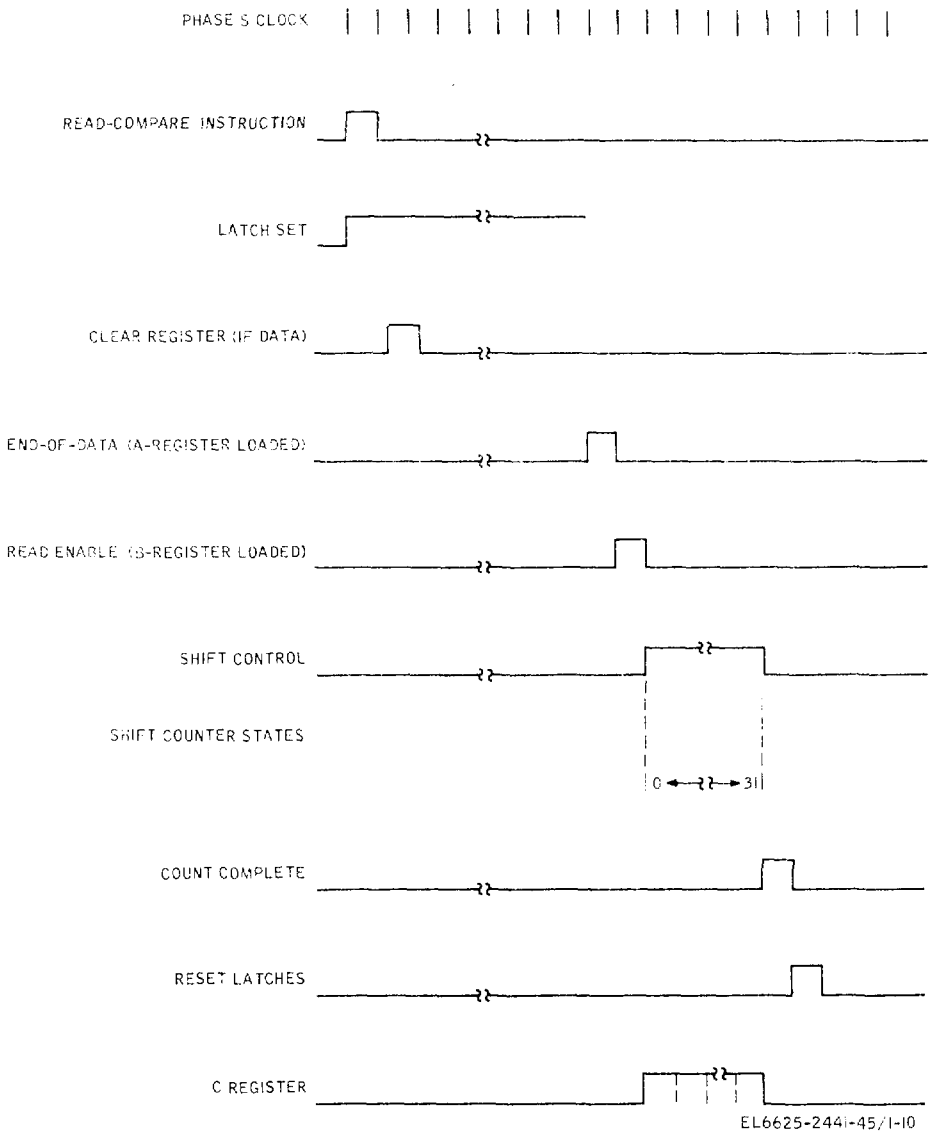


Figure 2-8. Read-compare, timing diagram.

(3) Following the data word that loaded the A-register, an end-of-data pulse is applied to the read-compare control logic. This enables the input multiplexer, the register input multiplexer, and the shift control logic. The B-register is loaded, and the shift control logic applies a clock signal to the A-, B-, and C-registers. Data is always present at the input multiplexer. Only the multiplexer enable signals are needed to initiate loading of the B-register.

(4) The contents of the A- and B-registers are bit serially shifted into the comparator logic. The content of each bit location of the A-register is compared with the content of the same bit location in the B-register; the result is shifted into the C-register. At the end of the comparison operation, a count complete pulse is generated and the latches reset. The A- and B-registers are continually checked for saturation (all l's). Saturation of either or both the A- and B-registers indicates that a flip-flop in the saturated TM 11-6625-2441-45-1 register has malfunctioned. If this condition exists the latches are reset, the test set malfunction light is on1, and the tape is stopped.

c. Read-Compare Reiteration (fig. 2-9). Any comparison failure causes the error control to apply a signal to the read-compare control logic. To ascertain the existence of an error, the entire read-compare routine is then repeated. If the failure persists, the error control causes only the compare function to be repeated. If the failure is still evident, a branch on no-go instruction causes various routines to be performed within the computer, to further isolate the fault.

2-13. Branch Control Function
(fig. 2-10)

The branch function provides for branching to a specific address and continuing the program with

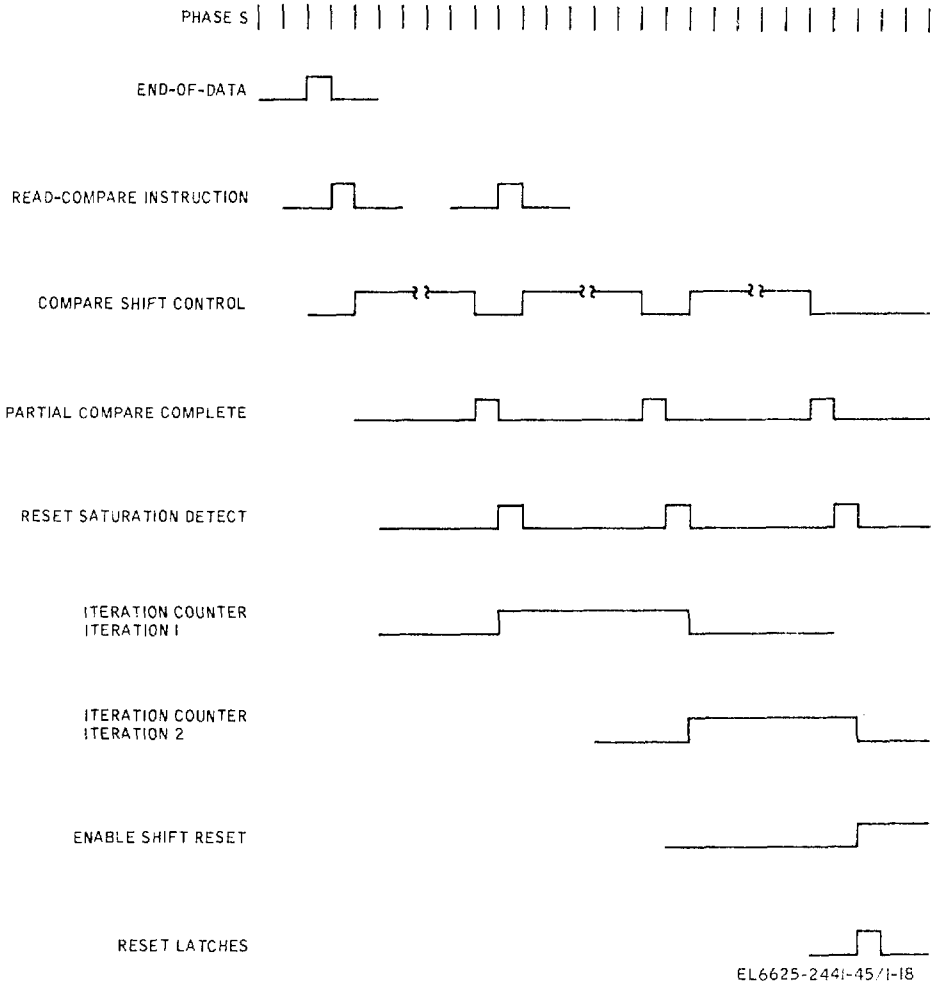


Figure 2-9. Read-compare reiteration, timing diagram.

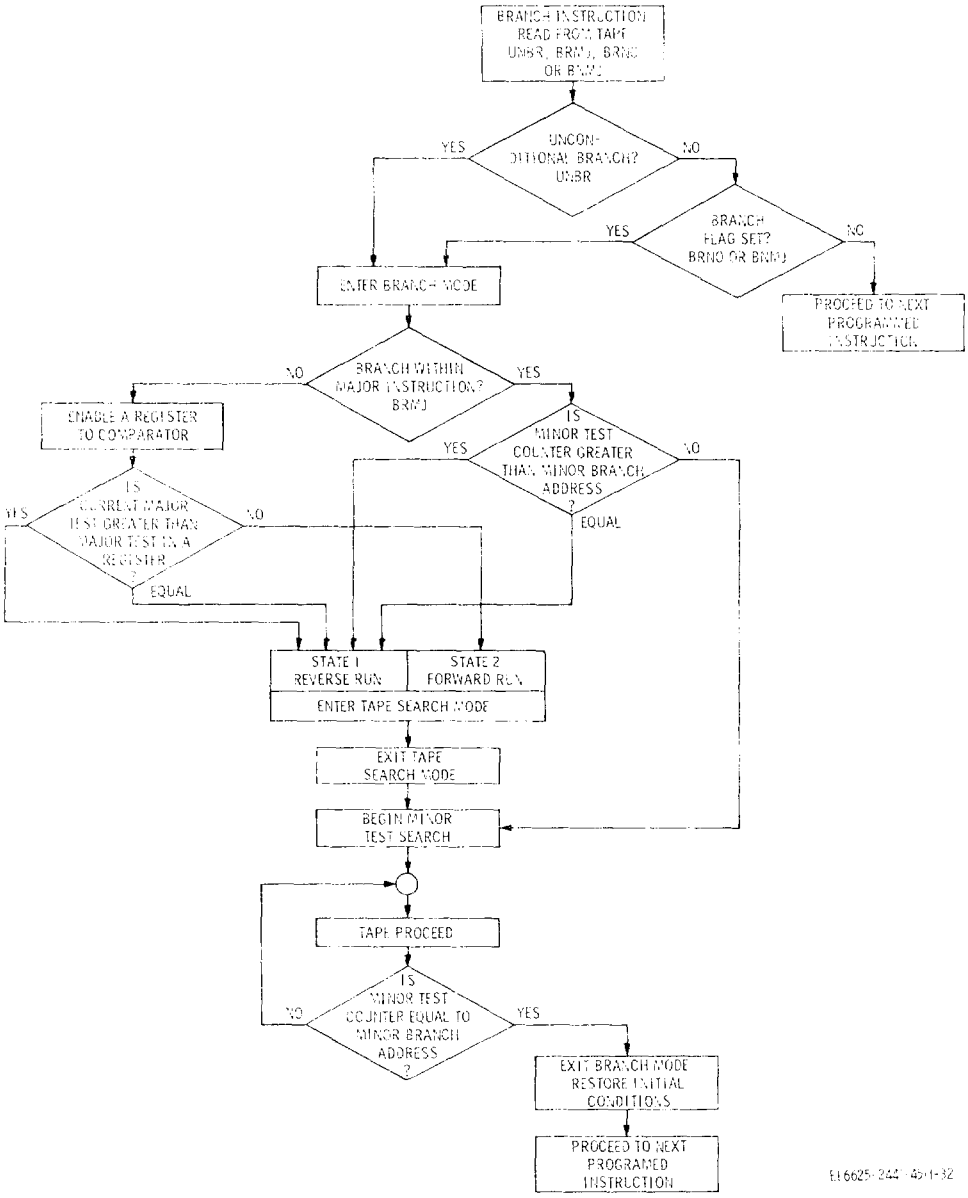


Figure 2-10. Branch control function, flow chart.

the instruction stored at that address. A branch function is initiated by one of four tape instructions: unconditional branch (UNBR), branch on major mode (BRMJ), branch on no-go flag (BRNO), and branch on no-go flag when within a major mode (BRMJ).

a. Unconditional Branch. An unconditional branch instruction read from the tape causes the logic to enter the branch mode. Data from the tape following the branch instruction consists of major and minor test numbers to which a branch is desired. The data is loaded into bits 17 through 32 of the A-register. The minor test number occupies the low-order bits (17 through 24) and the major test number is stored in bits 25 through 32. A comparison is then made between the major test number stored in the A-register and the major test number currently displayed. The result of the comparison causes the tape to run forward or reverse (tape search mode) so the tape search logic can make a comparison between the current major test number and the desired major test number. If the major test number [n the A-register is greater than the current major test number, the tape reader runs forward; if less,

the tape reader reverses. During tape search, the tape always runs at high speed. Refer to paragraph 2-20 for a detailed description of the tape search function. After a comparison has been made, the tape search mode is terminated and the test set remains in the branch mode. The minor test search is entered and the tape runs forward at low speed. In a minor test search, the tape always runs forward because the search always starts at address 00. In a minor test search, all instructions are inhibited except increment minor test counter (INCM). A comparison of the minor test counter contents and the minor test number stored in A-register continues until a comparison is achieved. The branch mode is then terminated and normal instruction execution follows.

b. Branch on Major Mode. A branch on major mode instruction provides for branching only to a desired minor test and assumes that the major test in the A-register is the current one. The instruction causes the test set to enter the branch mode. Following the instruction, tape data provides the minor test number which is stored in the A-register as the desired minor test. Tape search mode is entered when a comparison is made between the A-register minor test number and the minor test counter contents. The A-register is gated to the tape search logic in the branch mode. If the A-register minor test is less than the current minor test, the tape moves in a reverse direction. However, if the desired minor test is greater than the current minor test, tape search is not entered; minor test search routine is entered. The tape continues to run forward at low speed until a comparison is detected by the logic.

c. Branch on No-Go. A branch instruction can be executed if a no-go flag is set, indicating an error has been detected. After reading the branch instruction and identifying the set side of the no-go flag, the procedure for the branch and tape search function is the same as described in a above.

d. Branch on No-Go Within Major. A branch instruction can be executed if a no-go flag has been set during a major mode of operation. The procedures outlined in b above are applicable for this operation after the logic has detected a no-go in a major mode.

2-14. Computer and Control-indicator Interface Test

Logic is provided within the test set for simulating the input-output units associated with the computer. Logic is also provided for processing analog signals, and for simulating the computer when the control-indicator is being tested.

a. Analog Processing. To check the computer reception and processing of analog signals, test signals of known amplitude are generated within the test set. These signals (ac and dc) are applied to the appropriate inputchannels of the computer analog-to -digital converters, and compared with the known input. Digital-to-analog converters in the computer are then addressed to generate an analog signal. Analog signals from the computer are divided into three groups; synchro, voltage, and low-level signals. The analog control word (instructions from tape reader) enables one of these signals to be scaled within the test set, and routed back into the computer, via the analog channels previously tested. If the analog control word selects a synchro signal, that signal is routed directly back to the computer. These signals are also processed by the test set. to provide sine and cosine signals. The sine and cosine signals are applied to the computer for angle verification. All signals applied to the computer analog input channels can also be applied to the TEST position of the VOLTAGE MONJTOR switch on the SCU. This capability is controlled by the analog control word.

(1) *Computer analog channel test* (fig. 2-11). a load analog control word instruction is received. the contents of the A-register (analog control word) are loaded into the B-register. This analog control word causes ac and dc test signals to be applied to a MOS switch, and the MOS switch control to activate the appropriate MOS switch. This condition causes the selected test signal to be applied through the buffer amplifier to the computer analog input channel.

(2) *Synchro and voltage signals* (fig. 2-12). Computer synchro output signals are received by the test set and applied directly back to the computer synchro-to-digital converters, via synchro input channels. These signals are also applied to the synchro termination networks within the test set, which output the sine and

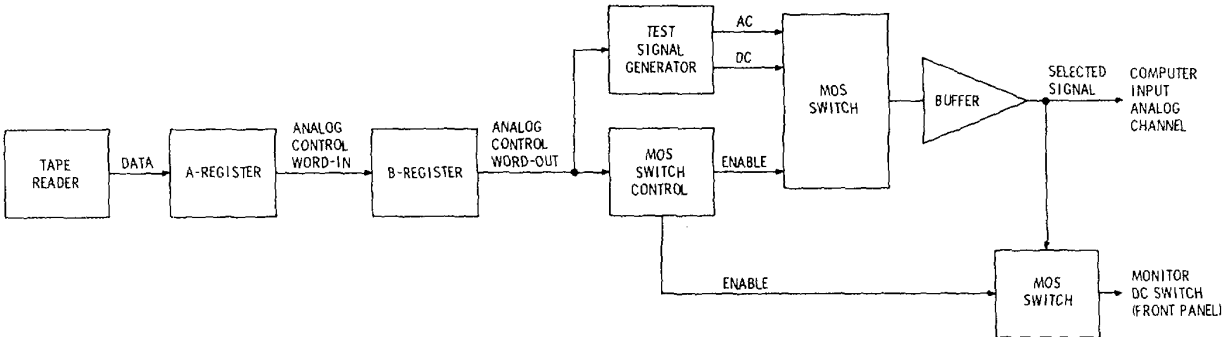


Figure 2-11. Analog processing test, data flow block diagram.

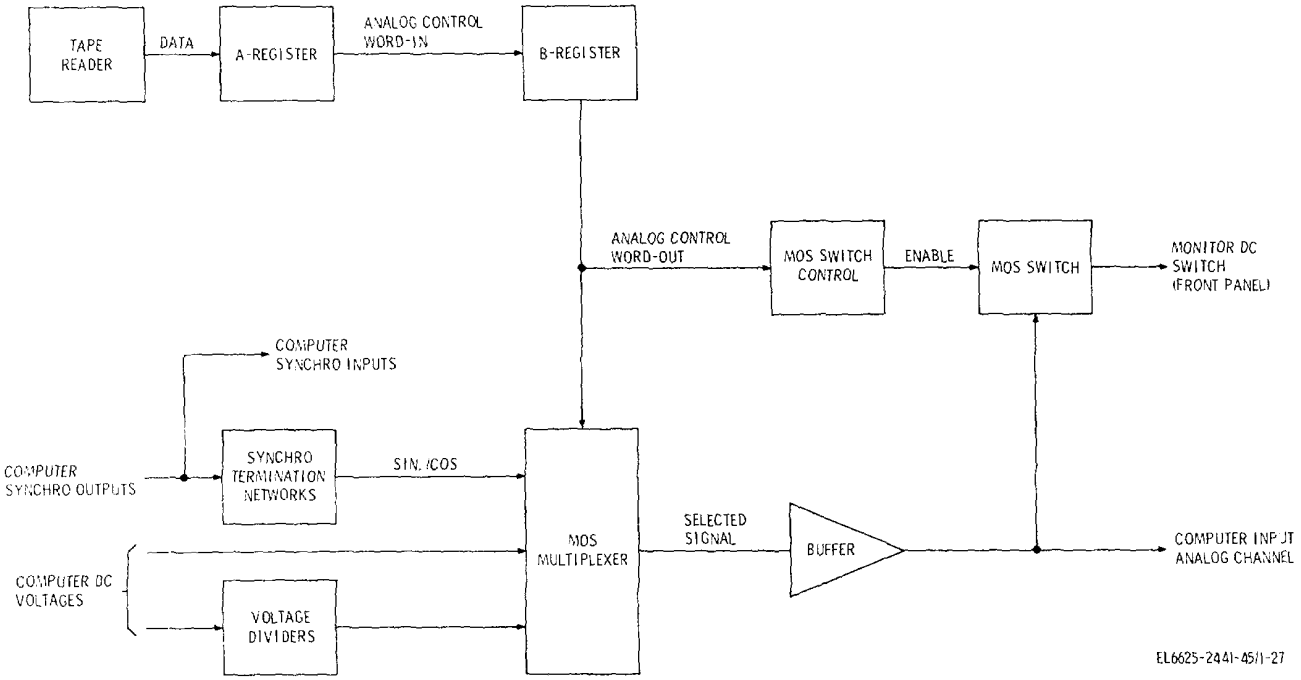


Figure 2-12. Analog processing – synchro voltage signals, data flow block diagram

cosine function of each synchro. The sine and cosine signals are applied to the MOS multiplexer, causing the signal selected by the analog control word to be applied through the buffer amplifier to the computer analog input channel. To insure the computer has provided the voltages required for a second memory unit, a voltage divider network receives the voltages and establishes a signal at a nominal level. This signal is applied to the MOS multiplexer and processed in the same manner as the synchro signals, when selected by the analog control word. Test set voltages are received and processed in the same manner. The following chart lists the synchros and voltages tested, and the analog control word construction for each synchro and voltage.

(3) Low level signals (fig. 2-13). Low level analog signals from the computer are applied to the MOS switches. Depending on the construction of the analog control word, the MOS switch control enables one of the switches, causing the selected signal to be applied to the preamplifier. The amplified signal is applied through another MOS switch (enabled by the same analog control

Synchros and voltages	Description	Analog control word														
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
True airspeed feedback	Sin	0	0	0	x	x	x	x	x	x	0	0	0	1	0	0
	Cos	0	0	0	x	x	x	x	x	x	1	0	0	1	0	0
Magnetic heading-course indicator	Sin	0	0	0	x	x	x	x	x	x	0	1	0	1	0	0
	Cos	0	0	0	x	x	x	x	x	x	1	1	0	1	0	0
Bearing minus heading	Sin	0	0	0	x	x	x	x	x	x	0	0	1	1	0	0
	Cos	0	0	0	x	x	x	x	x	x	1	0	1	1	0	0
Range to destination (units)	Sin	0	0	0	x	x	x	x	x	x	0	1	1	1	0	0
	Cos	0	0	0	x	x	x	x	x	x	1	1	1	1	0	0
Magnetic heading-BDIII	Sin	0	0	0	x	x	x	x	x	x	0	0	0	0	1	0
	Cos	0	0	0	x	x	x	x	x	x	1	0	0	0	1	0
Range to destination (tens)	Sin	0	0	0	x	x	x	x	x	x	0	1	0	0	1	0
	Cos	0	0	0	x	x	x	x	x	x	1	1	0	0	1	0
Magnetic heading-TACAN	Sin	0	0	0	x	x	x	x	x	x	0	0	1	0	1	0
	Cos	0	0	0	x	x	x	x	x	x	1	0	1	0	1	0
Range to destination (hundreds)	Sin	0	0	0	x	x	x	x	x	x	0	1	1	0	1	0
	Cos	0	0	0	x	x	x	x	x	x	1	1	1	0	1	0
Computer																
+30V		0	0	0	x	x	x	x	x	x	0	0	0	0	0	1
+30V		0	0	0	x	x	x	x	x	x	1	0	0	0	0	1
+12V		0	0	0	x	x	x	x	x	x	0	1	0	0	0	1
-6V		0	0	0	x	x	x	x	x	x	1	1	0	0	0	1
+12V		0	0	0	x	x	x	x	x	x	0	0	1	0	0	1
-6V		0	0	0	x	x	x	x	x	x	1	0	1	0	0	1
+5V		0	0	0	x	x	x	x	x	x	0	1	1	0	0	1
+5V		0	0	0	x	x	x	x	x	x	1	1	1	0	0	1
Test set																
+15V		0	1	0	0	0	0	0	0	1	x	x	x	0	0	0
26 Vac		0	0	1	0	0	0	0	0	1	x	x	x	0	0	0

word), and is processed in the same manner as the synchros and voltages. The following 'chart lists the low-level signals tested, and the analog control word construction for each signal.

b. Load Discrete Word (fig. 2-14). Data in the discrete input holding register is loaded into the computer upon receipt of a load discrete word instruction. The holding register can be

Low-level signals	Analog control word														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Drift angle error	1	0	0	1	0	0	0	0	x	x	x	x	0	0	0
Lateral steering error	1	0	0	0	1	0	0	0	x	x	x	x	0	0	0
Groundspeed error	1	0	0	0	0	1	0	0	x	x	x	x	0	0	0
Deviation	1	0	0	0	0	0	1	0	x	x	x	x	0	0	0
Azimuth cage error	1	0	0	0	0	0	0	1	x	x	x	x	0	0	0

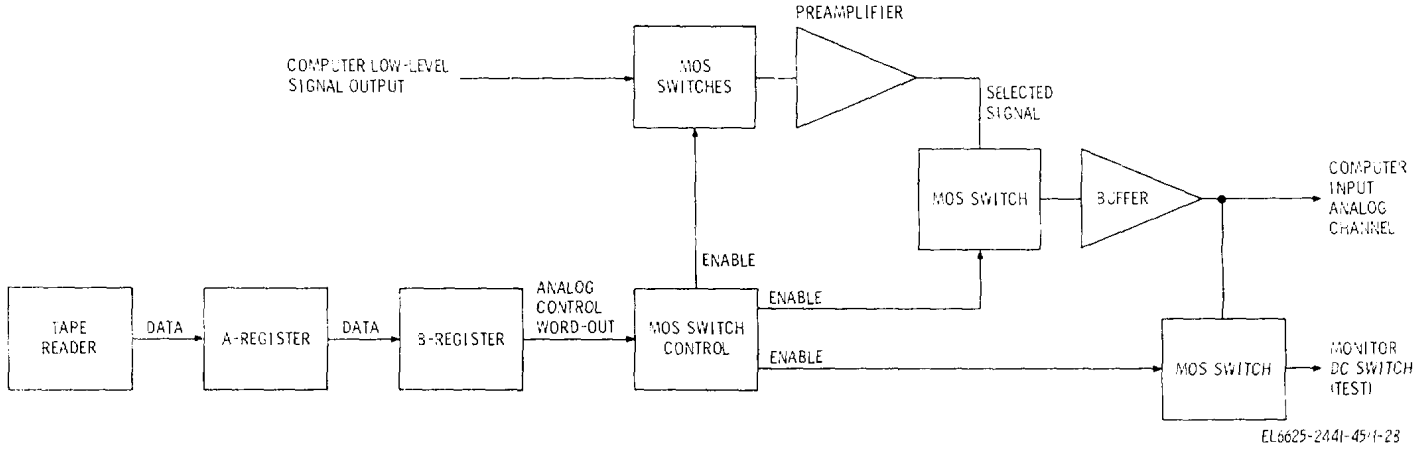


Figure 2-13. Analog processing—low level signals, data flow block diagram.

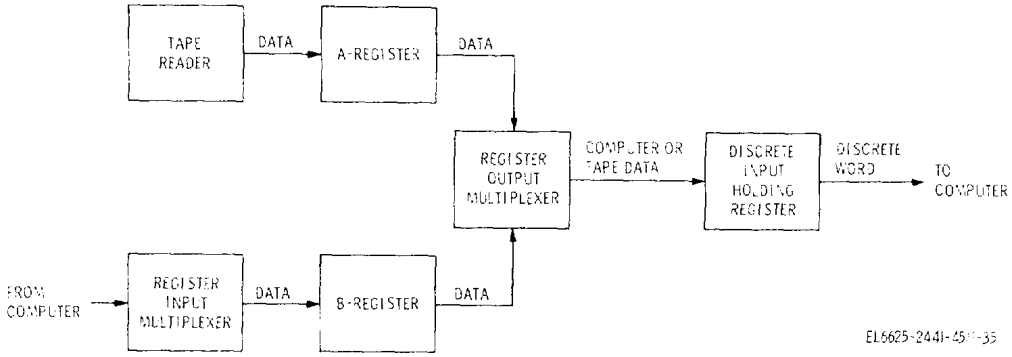


Figure 2-14. Load discrete word, data flow block diagram.

loaded with data from either the A- or B-registers, depending on the load instruction. The A-register receives data from the program tape and the B-register from the computer. Both groups of data are applied through the register output multiplexer. If the B-register is used, it is loaded by an instruction preceding the load discrete word instruction.

c. Discrete Terminations. Portions of the discrete output word (from computer) are analog signals. During a read-compare discrete output word instruction, these analog signals must be converted to digital form to be processed by the test set. This operation is performed by the discrete input termination network. The entire discrete word is then read and compared as described in paragraph 2-12.

d. Control-Indicator and TACANT Interface (fig. 2-15). Depending on the operation being performed by the computer, control indicator, or TACAN, data and data control pulses are received from the computer. Data

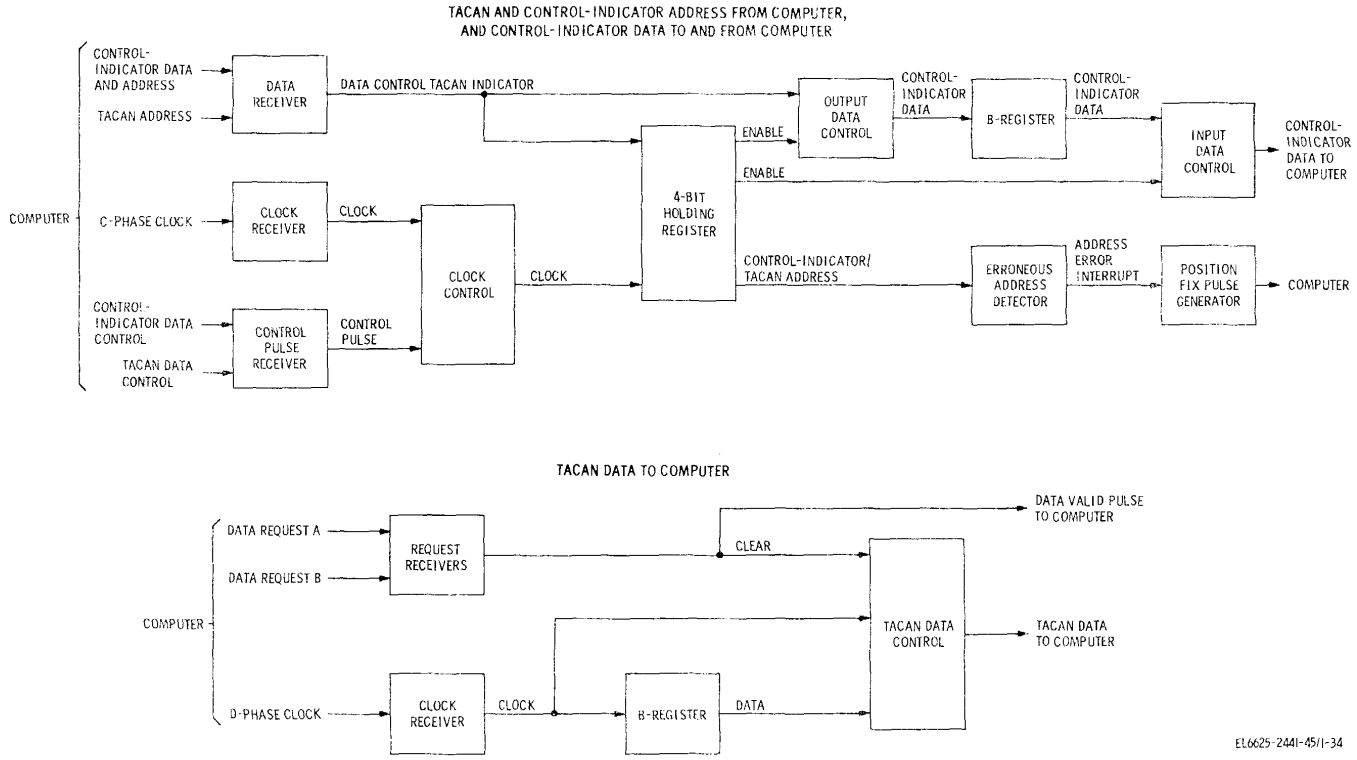


Figure 2-15. TACAN and control-indicator data processing, data flow block diagram. 2-23

is applied to the output data control logic, and the four-bit holding register. When the control pulse is high, a clock signal causes the four-bit register to be loaded (representing control-indicator or TACAN address). When the control pulse goes low, the clock signal is inhibited and the four-bit register stops shifting; the erogenous address detector decodes three bits of the register, and checks for a valid address. If the address is not valid, a posse fix signal is generated and applied to the computer, causing the computer to perform a subroutine. The fourth bit of the four-bit register is used only when processing control-indicator data, and causes the data word received from the computer to be loaded into the B-register, or the contents of the B-register to be applied to the computer (representing a control-indicator data work to computer). Logic is provided for applying TACAN data to the computer when TACAN data has been requested by the computer (fig. 2-16). Two data request signals (A and B) are generated by the computer and applied to the test set, causing a data valid pulse to be applied back to the computer. The data valid pule also clears the TACAN data control logic. The contents of the B-register ae then applied to the computer (representing a TACAN data word) at the rate of the phase D clock, also generated in the computer.

e. Control-indicator Position Fix Test (fig.2-17). Pressing the POS. -FIX push-button on the control-indicator, causes a pulse t be applied to logic to check the pulse width. A 2-MHz clock

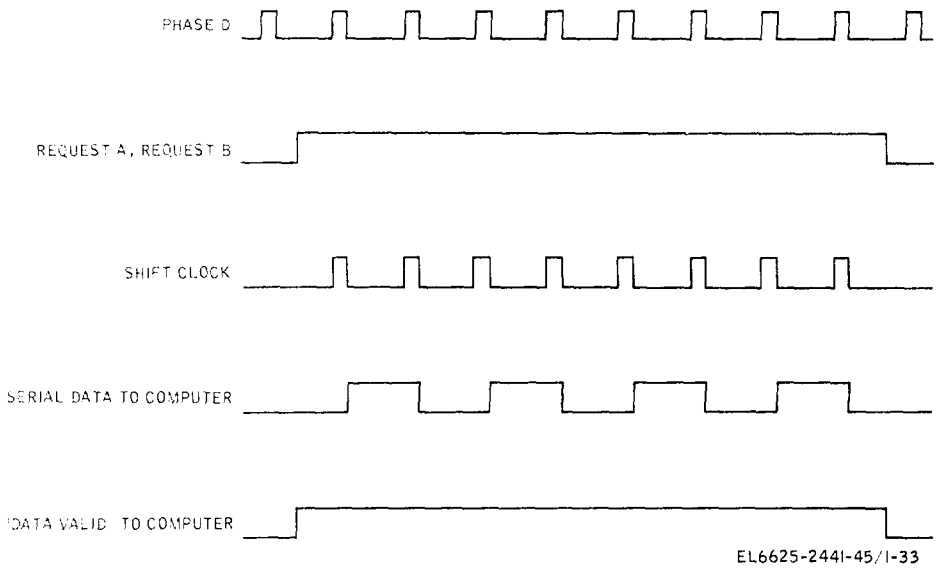


Figure 2-16. TACAN data to compare, timing diagram.

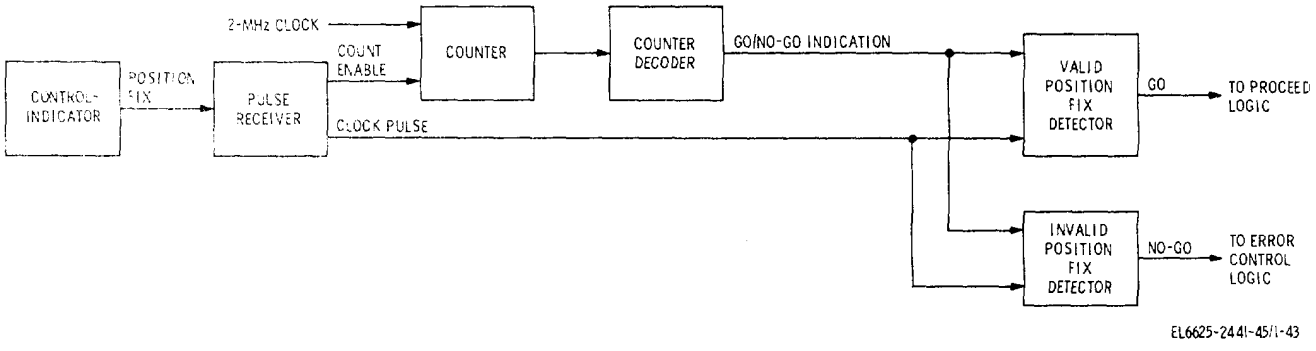


Figure 2-17. Control-indictor position fix test d flow block diagram.

signal drives a counter, which is decoded and applied to the detector logic. The position fix signal is also applied to the detectors, and depending on the state of the counter, the time period of the position fix pulse is determined. If the pulse width is less than 4 microseconds or greater than 8, an error signal is applied to the error detection logic, causing a no-go condition. If the pulse width is within the 4- to 8-microsecond range, a signal is applied to the tape proceed logic, causing the tape to drive.

f. Control-Indicator MODE Switch Test (fig. 2-18). To test the control-indicator MODE switch, an instruction causes a latch to set. This condition enables the MODE switch position drivers, and applies a ground signal to the wiper of the switch. Positions of the switch can now be applied, through the display multiplexer, to the front panel REGISTERS display indicators. The nine MSD of the REGISTERS display indicator, correspond to the nine positions of the switch. Each position of the switch causes an 8 to be displayed in its respective display.

g. Control-indicator Input Test (fig. 2-19). An instruction to load the control indicator causes the tape reader to load 32 bits of data (data word) into the A-register, and then into the control-indicator. A clock signal and a control pulse are also applied to the control indicator. The control pulse is high for the first, four bits of the data word (control-indicator address), then low for 28 bits.

h. Control-Indicator- Input-Output Test (fig. 2-20). To check the input-output capabilities of the control-indicator, an instruction causes the clock signal and control pulse to be applied to the control-indicator in the same manner as for the control-indicator input test. Four data bits (representing control-indicator address) are loaded into the A-register from the tape reader, and then shifted to the control-indicator. Depending on the address, the control-indicator either

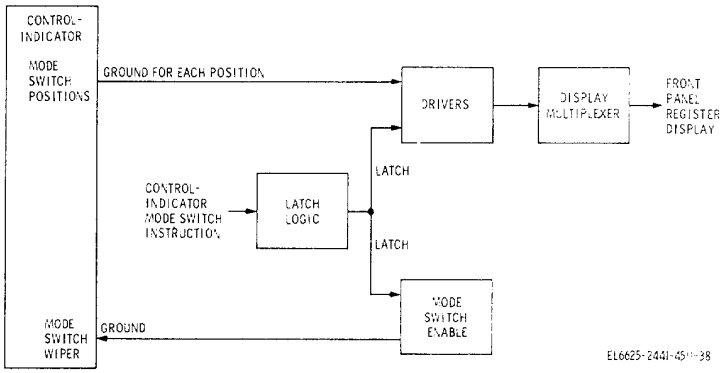


Figure 2-18. Control-indicator MODE switch test, data flow block diagram.

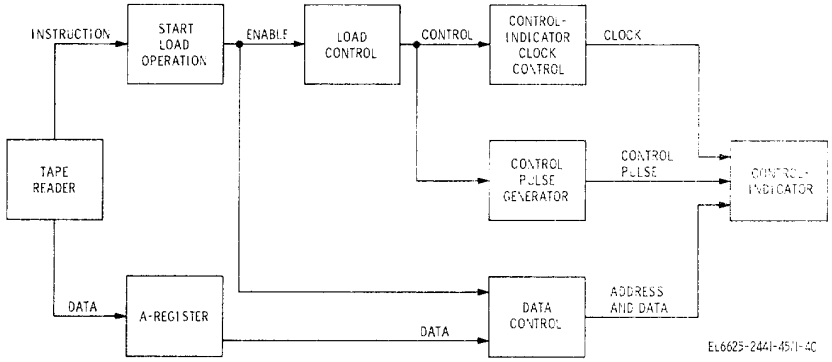


Figure 2-19. Control-indicator input test, data flow block diagram.

shifts data into the B-register, or the contents of the I;-register are shifted to the control-indicator.

i. Platform Interface Tests (fig. 2-21). Three tests are performed to check the platform interface logic. Each of the three instructions (one per test) causes a latch to set, and reset at the completion of the test. These latches set up initial conditions within the test set, for that particular test.

(1.) The first test insures that the proper incremental platform angles have been developed by iH3Ie computer. An instruction causes one of four data words (torque inputs) to be applied to the up/down counter, through the torque input control logic. The counter shifts at a 6.25-kHz rate, and counts up when the torque input is ground. After 11 milliseconds, the computer applies a signal that Stops the 6.25-kHz clock when the torque input goes high. The contents of the counter are then loaded into the B-register. An acknowledge signal is then applied to the computer, followed by the contents of the B-register. This process is repeated for tie remain i31g three data words.

(2') The second test verifies the capability of the computer to count increment velocity pulses , the test set generates four different pulse trains in two directions, off two axes. One of seven eight-bit data control words is loaded into the B-register from the computer. The computer applies a signal to reset and start the

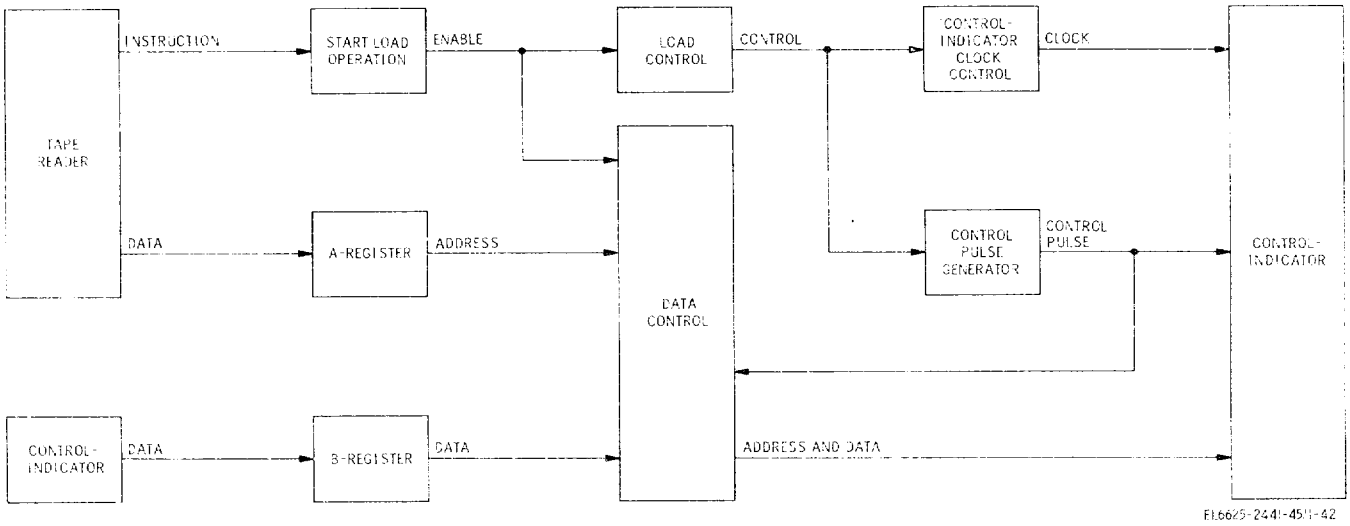


Figure 2-20. Control-indicator input-output test, data flow block diagram.

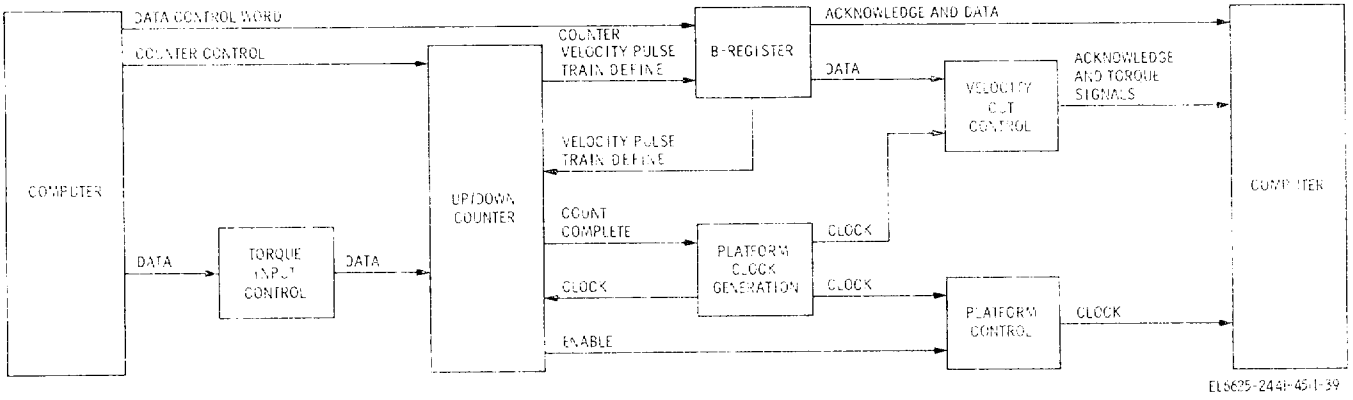


Figure 2-21. Platform interface test, data block diagram.

up/down counter, and applies the platform 100-kHz clock to the test set. The time duration of the velocity pulse train is defined by the contents of the B-register. When the up/down counter completes a count, the clock is stopped and an acknowledge signal is applied to the computer. This condition causes the computer to perform a subroutine, comparing the torque rate with time duration of the counter. This procedure is repeated for the remaining six data control words.

(3) The third test provides for a self-test of the computer interface. The computer applies torquing signals to the test set, enabling logic for receiving incremental platform angle signals. The platform clock signal is then enabled, and the up/down counter reset and started. After 1.3 seconds, the counter is loaded into the B-register, then sent to the computer for comparison with known results.

2-15. Front Panel Indicators and Error Control

(fig. 2-22)

Indicators on the test set front panel indicate the unit under test, the go/no-go status of the unit or test set, that power is applied to unit and test set, and memory fill and verify operation is being performed.

a. Setting the UNIT switch to ON enables the computer and control-indicator define logic, and causes the UNIT indicator to light. The unit being tested causes +5 V7 signal to enable the corresponding define logic. The test tape for each unit applies a signal that identifies itself, to the define logic enabled by the unit being tested, and causes the respective indicator (NCU, CIU, or SELF TEST) to light. If the wrong tape has been inserted, or a unit has not been connected to the test set, the indicators flash and the tape stops.

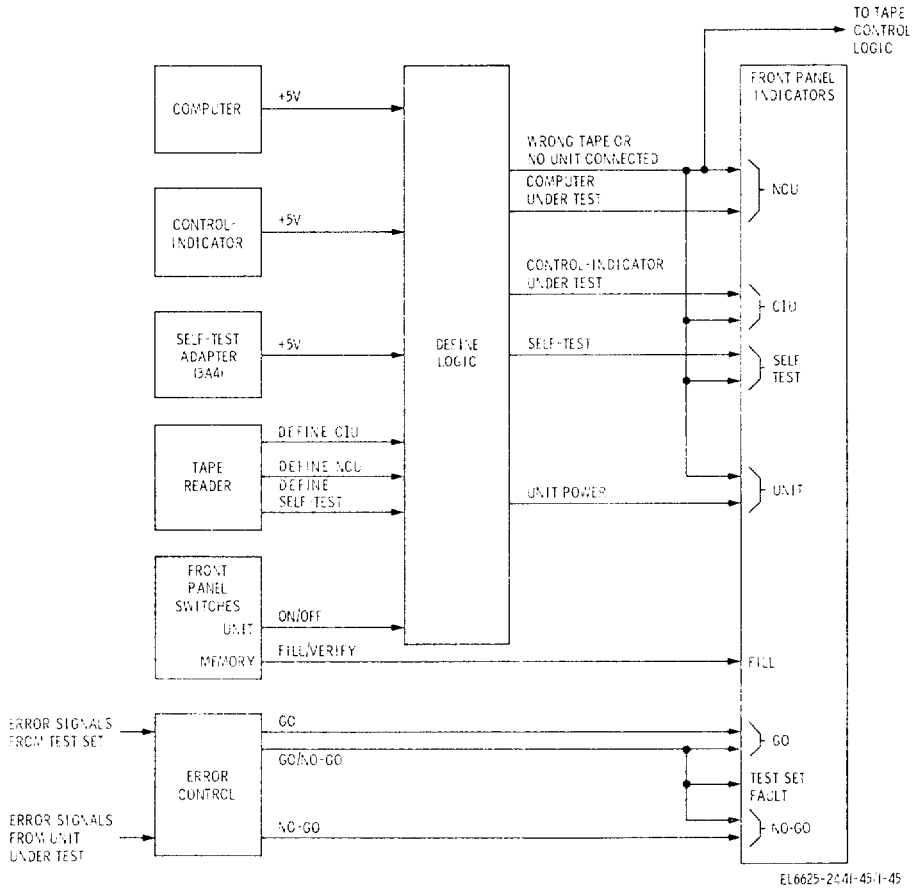


Figure 2-22. Front panel indicators and error control, data flow chart.

b. The FILL indicator lights when the memory fill/verify operation is being performed.

c. The results of the in-process test (within the test set) and error signals from the unit under test are applied to the error control logic, indicating a go or no-go condition. Error signals from the in-process tests have precedence over error signals from the unit under test. If the test S(et is in the go condition, the go and no-go logic for the unit being tested is enabled. The GO indicator is lit during testing and goes out at the end of tape; if an error has been detected, the GO indicator)., goes out and the NO GO indicator lights. In a test set failure, the GO and NO GO indicators are inhibited and the TEST SET FAULT indicator lights.

2-16. Clock Generator

The test set generates clock signals either in sync with the computer clocks, when testing the computer, or self-generates clock signals when testing the control-indicator or self-testing.

*a. Clock Generation During Computer Check*out. A 2-MHz clock signal (KPPOO) is received from the computer (fig. 2-23) and inverted by the test set logic (XKAOO1). Signal XKNAOO1 is delayed by 65 nano-seconds (XKA002) and XKAOO1 is also applied to a countdown synchronized flip-flop whose output provides a l-Miz clock signal, KKAOO5. Gated logic generates phase S and phase T negative-going 1-MlJz clocks for distribution throughout the test set.

(1) The computer 2-MHz square wave clock is checked continuously for correct phase shift limits to the 4-MHz square wave generated by the test set. Circuits provided by the test set compare the phase relationship of the two frequencies during a specified time period. If the two signals are beyond the designated limits, an error signal is generated. Figure 2-24 is a timing diagram showing the comparison period of the two frequencies. Each frequency is applied to a special coded counter. The 4-MHz test period occurs during the count of 3; the 2-Mllz test period

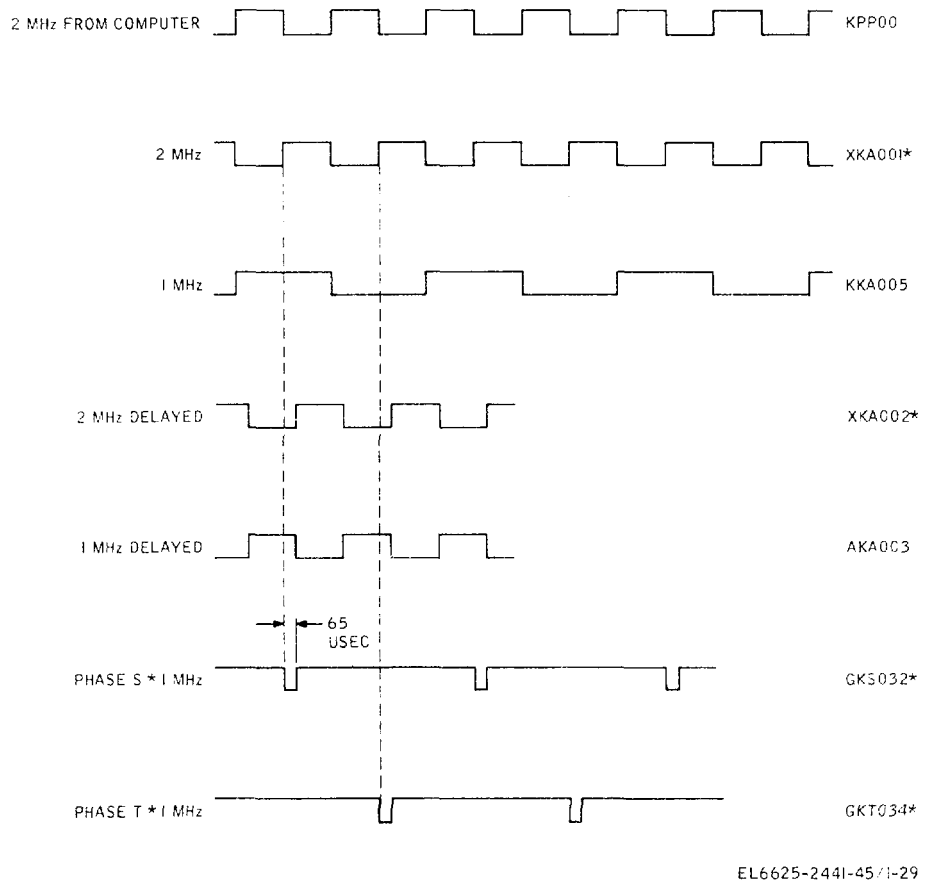


Figure 2-23. Test set clock system with computer clock running, timing diagram.

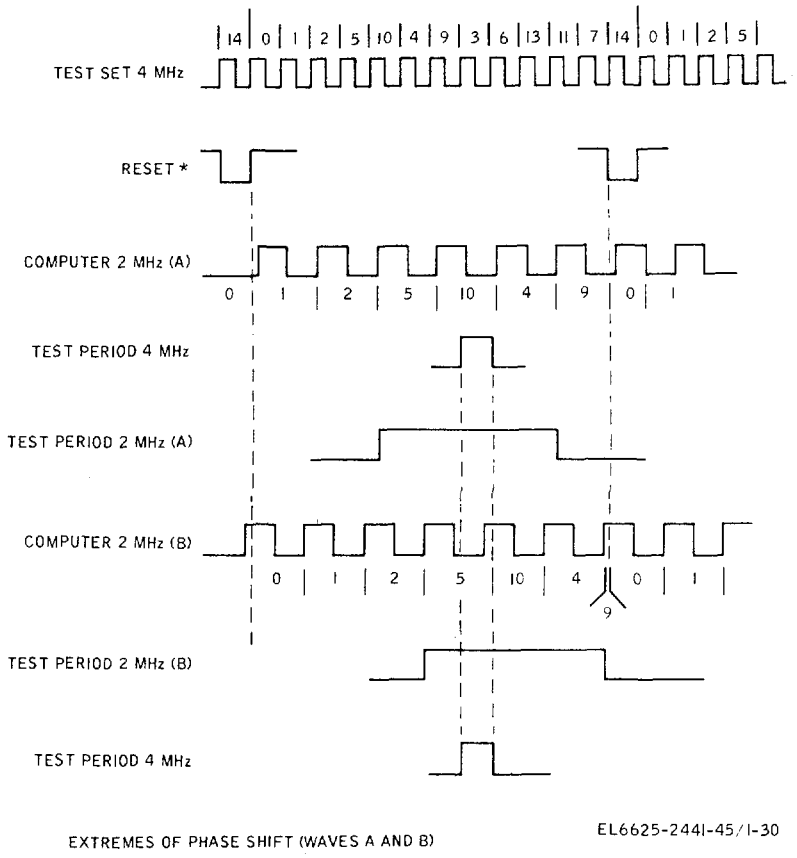


Figure 2-24. Two-MHZ-clock square wave, timing diagram.

occurs during the counts of 5, 10, and 4. The two test period signals are applied to an AND gate. If the output of the AND gate is low, the phase relationship is within limits. If the gated output is high for four consecutive comparisons, an error signal is generated indicating an out-of-phase condition.

(2) Three instructions control the computer clock. A run computer clock instruction (RCPC) causes the computer clock to be turned on for an indefinite period. The clock may be stopped by either the computer program or by an instruction from the test set tape (STCL). The computer clock can also be programmed to run for a specified number of clock periods by a run clock conditional instruction (RCNC). This instruction causes the computer clock to be turned on for N clocks (1 through 999), if a memory cycle does not occur during the last seven clocks. If a memory cycle is begun during the last seven counts of N, the clocks are stopped immediately and the memory cycle counter is cleared. When an unconditional clock run instruction is performed (RCNU), the clock runs continuously. The clock will be turned on for exactly N clocks (1 through 999).

b. Clock Generation During Self-Test and Control-Indicator Checkout. Clock pulses for self-test and control-indicator checkout are derived from the test set clock-generating circuits. A 4-MHz oscillator output applied to three countdown flip-flops (fig. 2-25) provides the 500 kHz necessary for self-test and control-indicator operation. Through logic gating, phase S and phase T clocks (0.5 MHz) are generated and distributed throughout the test set. Timing signal phase C is used for communication with the control indicator unit. To simulate computer clocks when in the self-test mode and enable the computer clock mode, signals GTTOOO* and GKAO41* are generated. GTTOOO* is connected back through the self-test adapter into QUPOOO, simulating KPPOO, 2-MHz square wave from the computer. Phase S and phase T in this mode are 1-MHz clocks.

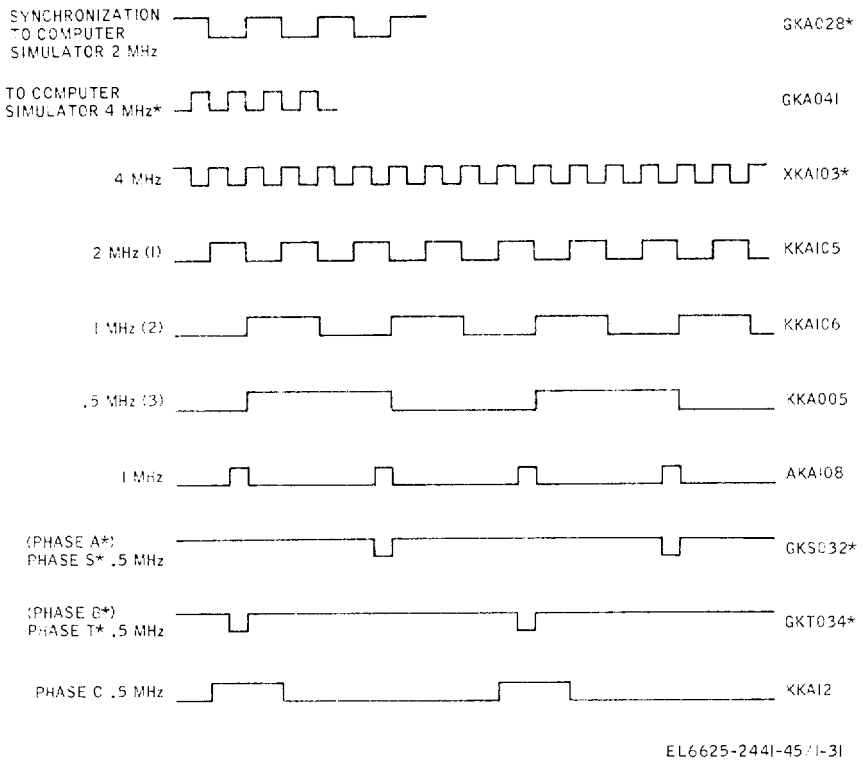


Figure 2-25. Clock generation during self- it and control-indicator checkout, timing diagram.

2-17. Power Supply 2AIPS1
(fig. 5-5)

The test set power supply is housed in the SCU. 'the following sub-paragraphs describe the power supply circuits, generation of de power supply voltages, and the power supply protective circuits.

a. Power supply control circuits. The power supply control circuits consist of transformer TI, -4.7 regulator VR1, relays K1 and K2, and power sequence switching assembly A2.

(1) The power supply is prepared for turnon when primary C-phase power is applied through connector J1-VWv' to the primary winding of transformer T1 The Output of the secondary winding of T1 is rectified by diodes CR1 and CR2 to provide +28 V auxiliary. The secondary winding center tap of T'1 is connected to power ground to provide the +28 V auxiliary ground return. The +28 V auxiliary is filtered by capacitors C6, C7 and C8 and supplied to relays K1 and K2, +4.7 V regulator VR1, power sequence switching assembly A2, negative voltage crowbar A3, positive voltage crowbar A44, and connector J1-N and Z. Regulator VR1 provides +4.7 V auxiliary to connector J1-M.

(2) The power supply is turned on in two steps. Power ground is applied to the ac power on signal line through connector J1-c to power sequence switching assembly A2, pin 2. A2 applies a ground through FL3 to relay K1 operates and closes the 115-V, 400-Hz three-phase power leads from connector J1-J, H, and G to the primary windings of A1T2. Dc voltages from rectifier assemblies A1Z1 through A1Z4 are applied to the inputs of regulators VR2, VR3, VR4, VR6, VR, 7, and VR8. The regulator control circuits are turned off by resistance divider networks connected through the contacts of dc power relay K2 to ground. The +28 V auxiliary is then applied to the dc power on signal line through connector J1-b to A2, pin 18. A2 applies a ground through F14 to relay K2. K2 operates and removes the resistance divider networks from ground, and regulators VR2, VR3, VR4, VR6, VR7, and VR8 turn on the dc voltages.

(3) When A2 receives a crowbar signal from the negative voltage crowbar A3, positive voltage crowbar A4, or +5 V crowbar A7, relay K2 is deenergized and initiates de power shutdown. A ground signal is generated which lights the appropriate indicator on the SCU test panel (fig. 2-26). When A2 receives a no-go signal from the voltage monitor A5S relay K2 is deenergized initiating dc power shutdown. A ground signal is generated which lights the OUT TOL indicator on the SCT test panel. The OVERRIDE switches (rig. 5--5) apply the override signal to A2 which causes relay f'2 to energize, removing the ground signals from the SCU test panel indicators. The OVERRIDE switches are used only during maintenance operation.

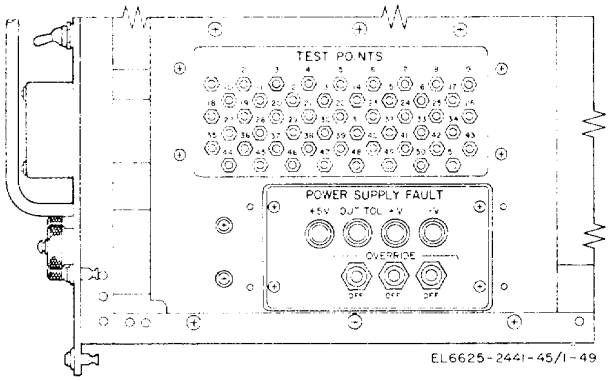


Figure 2-26. *Test panel, Signal Conditioning Unit TS -2913/ASMJ-386.*

b. Generation of -25 V, +28 V, and *±15* V. The output of the high-voltage secondary windings of transformer A1T2 is connected to rectifier assemblies AlZl and A1Z2. The secondary winding center taps are connected to ground return. The outputs of A1Z1 and A1Z2 are in parallel and provide negative and positive power supply voltages. The negative voltage is connected through LC filter (L1, C1l) to regulators VR2 and VR3. The outputs of VR2 and VR3, regulated -25 V and -15 V respectively, are connected through FL5 and FL6 to negative voltage crowbar A3, voltage monitor AS, and connector J2. The positive voltage is connected through LC filter (L2, C12) to regulators VR4 and VR6. The outputs of VR4 and VR6, regulated +28 V and +153 V respectively, are connected through FL7 and FL9 to the positive voltage crowbar A4, voltage monitor A5, and connector J2. The output of VR4 is also connected through diode A6CR4 to override the +28 V auxiliary.

c. Generation of +5 V and +4.7 V. The output of the low-voltage secondary windings of transformer A1T2 is connected to rectifier assemblies A1Z3 and A1Z4. The secondary winding center taps are connected to ground return. The outputs of AiZ3 and A1Z4 are in parallel to provide a positive power supply voltage. The positive voltage is connected through LC filter (1L3, C13) to +5 V regulator VR7 at VR7L1-6 and +4.7 V regulator VRS. The current path through VR7 is from the +22 V input through an input filter (VR7L1 pin 6 to pin 5 and capacitors VR7C1, VR7C2, and VR7C3), a power switch circuit (VR7Ql, VR7Q2, VR7R1, and VR7R2), an output inductor (VR71, 1 pins 1 and 2 to pins 3 and 4). and current-sensing resistors (VR7RCS and VR, 7R4) to the +5 V output. The output voltage of VR7 is compared with an internal reference voltage set by potentiometer VR7Ai-Ri3. While the output voltage is low, the power switch circuit is conducting (on state), current flow through the output inductor increases, and the output rises. When the output exceeds the reference level sensed by the voltage loop comparator, the level shift switch circuit causes the power switch circuit to cut off (open state). Simultaneously, the feed-back reduces the reference voltage level slightly. When the power switch circuit is in the open state, the self-induced voltage of the output inductor causes current to flow through diode VR7CR1, the output inductor, and the current-sensing resistors to the output. This current will decrease, and as it falls below the level demanded by the load, the output voltage will begin to decrease. As the output voltage drops below the reduced reference voltage level, the voltage-loop comparator circuit causes the level shift switch circuit to set the power switch circuit to the on state. The output voltage is thus regulated to an average level equal to the average level of the reference voltage. The small feedback signal applied to the reference voltage accelerates the switching speed, reducing switching losses. The output inductor and the switch timing capacitors, with the resultant output ripple, control the switching rate of the regulator. The current-loop comparator circuit causes the level shift switch circuit to set the power switch circuit to the open state when the voltage drop across the current-sensing resistors, caused by the load current, exceeds the internal reference level. When the load current has decreased, the current-loop comparator circuit causes the level shift switch circuit to set the

power switch to the on state. Since the rate of load current change is limited by the output inductor, the switching rate is set to a safe maximum value. The output of VR7, regulated +5 V, is connected through FL8, FL10, and FL11 to the +5 V crowbar A7, voltage monitor A5, +5 V bus W1 and connector J2. The output of VR8, regulated +4.7 V, is connected through FL12 to the voltage monitor AS, positive voltage crowbar A4, and connectors J1 and J2.

d. Voltage adjust controls. The voltage adjust controls (potentiometers) located in the building block voltage regulators (BBR) are listed in the following chart

e. Protective circuits. The protective circuits in the power supply comprise negative voltage crowbar A3, positive voltage crowbar A4, +5 V crowbar A7, and voltage monitor A5. The crowbar circuits monitor the regulated dc voltages and protect the test set from excessively high output voltages. If any of the power supply voltages exceed a specified limit, the crowbar connects that output to ground through silicon controlled rectifier (scr). The scr for crowbars A3 and A4 are contained within the sealed unlit and QT is the scr for crowbar A7. The output of the crowbars are applied to power sequence switching circuit A2 to light the appropriate POWER SUPPLY FAULT indicator on the SCU test panel. When the scr is operated by an over voltage condition, the resultant ground connection is sensed by the voltage monitor circuit A5. The function of the voltage monitor is to convert any loss of voltage or excessively low-voltage condition into a no-go signal. This signal 's applied to the power sequence switching circuit, deenergizing relays KT and K2, and the power supply is shut down.

Nomenclature	*Reference designators*
BBR (I)	VR4
BBR (III)	V, R6
BBR (IV)	VR2
	VR3
BBR (V)	VR1A
	VR8
Switching regulator	VR7

Regulated outputs	*Control*	*Value (ohms)*
+28 V	R14	500
+15 V	R14	500
-25 V	R14	500
-15 V		
Aux. + 4.7	VR13	500
+ 4.7 V		
+ 5.9 V	VR7A1R13	2000

2-18. Power Control and Distribution
(fig. 5-6)

Three-phase 115-Vac, 400-Hz and +28 V primary power is required to operate the test set. Power is applied to the SCU and then distributed to the LCU and units to be tested through a series of connectors and interconnecting cables.

a. Power Control. Three-phase 115 Vac is applied to SCU PRIMARY POWER circuit breaker CB4 through P'RINIARY POWER 115 Vac 400 Hz 3 PH connector Ji and RFI filter FL1. Plus 28 V is applied to NCU POWER 28 VDC circuit breaker CB2 and CIU POWER 28 VDC circuit CB3 through PRIMARY POWER 28 VDC connector J2 and RFI filter FL2.

(1) *Primary power* on. The test set is prepared for use by operating PRIMARY POWER circuit breaker CB4. Circuit breaker CB4 applies three-phase 115 Vac to power supply PS1. The C-phase line turns on SCU blowers BT, B2, and B3, and lights POWER PRIMARY indicator DS5. The A-phase line is connected to NCU POWER 115 VAC 400 Hz circuit breaker CB1. The B-phase line is connected to LOGIC CONTROL UNIT connector J5-E and through interconnecting cable, to SIGNAL CONDITIONING UNIT connector J3-E to operate LCU blowers BT and B2. Circuit breaker CB1 applies the A-phase line to NAV COMPUTER UNIT BLOWER connector J10-A and the primary of transformer T1 supplies 26 V rms, 400 Hz to the NAV COMPUTER UNIT connector J9 and to card cage assembly A3. Circuit breaker CBE also closes the circuit to NCU POWER 115 VAC 400 Hz indicator DST.

(2) *Plus 28 V* on. Operating NCU POWER 28 VDC circuit breaker CB2 applies +28 V to

NAV COMPUTER UNIT connector J9 and lights the NCU POWER 28 VDC indicator DS2. Operating CIU POWER 28 VDC circuit breaker CB3 lights the CIU POWER 28 VDC indicator DS3 and applies +28 V to LOGIC CONTROL UNIT connector J5 and through interconnecting cable, to SIGNAL CONDITIONING UNIT connector J3.

b. *Power Distribution*. Power supply PS1 is prepared for turn on by operating POWER AC switch S3. A ground is connected to the ac power on signal. POWER AC indicator DS4 and NCU POWER 115 VAC 400 Hz indicator DS1 light from +4.7 V auxiliary. POWER ELAPSED TIME mete M1 operates from +28 V auxiliary. The +28 V auxiliary is also sent to LOGIC CONTROL UNIT connector J5-X and through interconnecting cable, to SIGNAL CONDITIONING UNIT connector J3-X. Operating the LCU POWER TEST SET switch S7 applies +28 V auxiliary to operate LCU POWER ELAPSED TIME mete M1 and return the dc power on signal to SIGNAL CONDITIONING UNIT connector J3-W, and through interconnecting cable, to LOGIC CONTROL UNIT connector J5-W.
The dc power on signal turns on power supply PS1.

(1) Plus 5 V. SCU bus W3 distributes +5 V to card cage assemblies Al, A2, and A3, VOLTAGE MONITOR switch S1, LOGIC CONTROL UNIT to SIGNAL CONDITIONING UNIT connector J3. LCU bus W3 distributes +5 V to card cage assemblies Al, A2, A3, and A4, test panel A6, and TEST POINTS 88, 93 and 98.

(2) Minus 15 V. SCU PS1 supplies -15 V to card cage assembly A3 and to VOLTAGE MONITOR switch S1.

(3) Plus 4.7 V. SCU PSI supplies +4.7 V through TB1 to VOLTAGE MONITOR switch S1, to LOGIC CONTROL UNIT connector J5 and, through interconnecting cable, to SIGNAL CONDITIONING UNIT connector J3. LCU bus W4C distributes +4.7 V to card cage assemblies Al and A4 and to LAMP TEST switch S8.

(4) Plus 15 V. SCU PS1 supplies +15 V to card cage assembly A3, VOLTAGE MONITOR switch S1, LOGIC CONTROL UNIT connector J4 and, through interconnecting cable, to SIGNAL CONDITIONING UNIT connector J5. Connector J5 connects +15 V to LCU card cage assembly A2.

(5) Minus 25 V. SCU PS1 supplies -25 V to card cage assembly A3 and to VOLTAGE MONITOR switch S1.

(6) Plus 25 V. SCU PS1 supplies +25 V to VOLTAGE MONITOR switch Sl.

(7) Plus 28 V. SCU PS1 supplies +28 V to card cage assembly A3 and to VOLTAGE MONITOR switch S1.

Section III. TAPE FORMAT AND CONTROL

2-19. Self-Test Tape Operation

a. General Description. The self-test tape is run first to insure that the test set is operating properly. During self-test, the test set analyzes its own outputs, conversions and comparison techniques, and control processes. If the self-test tape completes its run without detecting a failure, the computer or control-indicator test tape is loaded. If a fault is detected while running the self-test tape, the tape stops; the test set displays inform the operator of the fault by displaying a particular number. The operator consults the troubleshooting charts for an interpretation of the displayed number.

(1) The test set contains internally mounted controls to assist maintenance personnel in manual isolation of malfunctions of the test set. Test set power and supply failures can be overridden so that the failure can be rapidly ascertained. The internal controls are inhibited when the test set is performing a unit test routine.

(2) When a test set fault is located, the faulty card is replaced with a new one.

(3) Self-test checkout by tape program incorporates two forms of testing, semiautomatic and automatic. Semiautomatic checkout verifies operation of functions which require operator

observation. This checkout is also used to expand the fault isolation capability of the test set. Areas tested in the semiautomatic checkout are instruction decodes, in-process fault detection, branching, tape format, register operation, analog/ synchro channels and control, memory verify functions, control-indicator pos fix test circuits, EOP tape control, and panel display functions.
Automatic checkout provides a thorough and detailed exercise of all areas of the tst set under various conditions of discrete inputs, outputs, and logic inputs/outputs.

b. Semiautomatic Checkout. The first portion of the tape program is the Initial confidence test. This test checks such circuits a power or reset, pull-up voltages, clock, tape data, and so forth. After each test the tape stops, and the operator checks for normal front panel indications. If the indications are normal, the START push-button switch is pressed and the operation is repeated until the final test ha been completed. If, at any time during the performance of the initial confidence check, a malfunction is detected, the operator refers to the related troubleshooting chart for recommended repair procedures. The remainder of the semiautomatic checkout is contained in major tests 1 through 19 on the program tape. These test are used to isolate faults in the test set which are not detected by the automatic portion of the self-test. Tests in this portion of the checkout are similar to those in the initial confidence test and are functionally grouped into major tests.

c. Automatic Checkout Upon completion of the confidence tests, the tape program provides an automatic check of the test set logic circuits. Automatic checks include the signal flow through discrete termination cards. All logic circuits are tested by programmed instruction signals.

d. Self-Test Instruction Initialization of various tests are controlled by the following instructions.

(1) Instruction TST1. Instruction requires the loading of up to 40 bits of self-test data into self-test registers located in the LCU and SCU. Self-test bits are assigned functions which, in general, control data paths. Following the loading of the self-test register, a number of data paths have been closed, the net effect being that some data (registers or test points) will be present at the parallel inputs of the B-register. A clock strobe is generated, loading the -register with whatever data is present and entry clearing the self-test register. The B-register is then compared with the expected results stored in the A-register through a compare instruction.

(2) Instruction TST2. A more extensive self-test is performed with this instruction. Up to 40 bits of self-test data are loaded into the self-test register. Self-test bits are assigned functions which, in general, control data paths.
Following the loading of the self-test register, a number of data paths will be closed, the net effect being that some data (registers and test points) may be present at the parallel inputs of the B-register. However, the self-test bits may also control logic not directly concerned with loading data into the B-register. Assuming that the Bregister is to be loaded, the loading takes place by a non-self-test instruction. In self-test 2 (TST2), the performance of certain regular instructions will cause data to appear at the inputs of the B-register, and will also initiate a load strobe to clock the B-register. The self-test register is then entirely cleared by the strobe. The B-register is compared with the expected results stored in the A-register by a compare instruction.
With instruction TST2, logic operations that do not require loading the B-register in parallel, may be controlled or simulated. In this case, a load strobe is not generated. Following whatever logic operation has been performed, the B-register will in general be loaded serially. The B-register is compared with the expected results by a compare instruction.

(3) Instruction TST3. The primary function of this instruction is to test the self-test register. The operand following the instruction consist of 72 bits arranged as 18 data characters. Data is loaded byte serially into the self-test register and the A-register simultaneously. After eight byte the A-register is loaded. However, shifting into the registers continue, with the least significant data being lost in the A-register. After shifting of the 10th byte, the self-test register is completely loaded. Beginning with the 11th byte, the output of the A-register and self-test register are compared, by an exclusive OR gate, bit serially. If a bit fails to compare, the TEST SET FAULT indicator lights, the tape reader stops, and the REGISTERS display shows the internal error

register by a numeric readout. The readout is then interpreted by referring to the troubleshooting charts to isolate the malfunctioning card in the self-test register.

(4) Instructions GSP3. This instruction verifies the gyro stabilized platform logic circuits located in the test set. When instruction GSP3 is used, the 100 k11z is checked, and the dynamic velocity pulse train generator is checked. During the test, the input/output complete line is checked to verify that the pulse occurs at the right time.

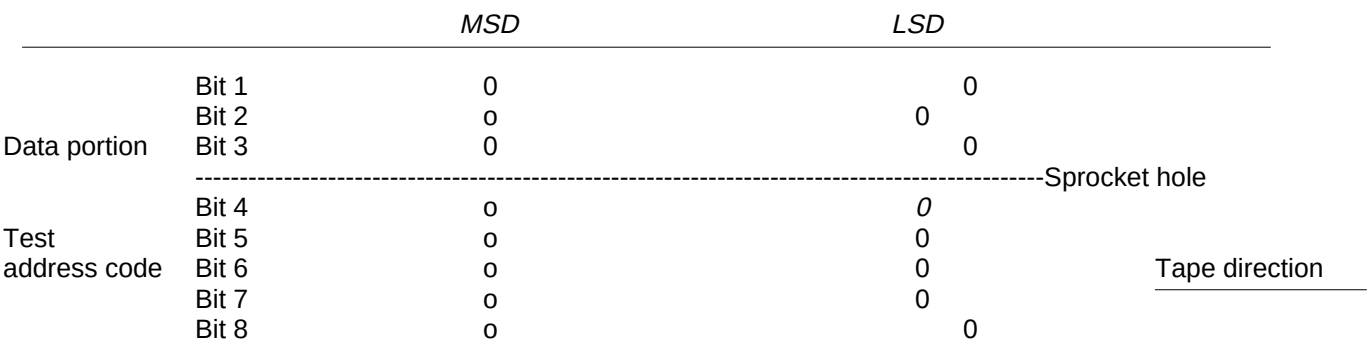
2-20. Tape Control and Processing
(fig. 5-7)

This logic provides for three functions; controlling the tape reader (TR), processing tape characters, and checking each tape character for errors. Controls *on* the front panel of internal test panel, or an instruction from the program *tape,* determine the direction and speed of the TR. The tape error detection performs various checks of' each tape character and group of characters (word) to insure the validity of the data from the TR. The tape character processing logic receives a Lest address (TA) instruction or data word, and processes the word accordingly.

a. Tape format. A tape character consists of one group of eight punched holes (bit positions) on the program tape. Tape characters are used to construct four types of program words. Bits 5 and 6 of each character define the type of word. The following chart illustrates the status of bits 5 and 6, and the number of tape characters for each program word.

Program word	*Status of bits 5 and 6*	*Number of tape characters*
Test address	5 6	2
Instruction	5- 6	2
Data	5- 6	1 to 7
End-of-data	5- 6	1

The tape is programmed to provide the words in the following sequence: test address, instruction, data, and end-of-data. Checks are performed, during running of the tape, to insure the correct tape format. Bits 1 through 4 comprise the data portion of a pure binary character; bit 7 is used for a code delete; and bit X is the parity bit used to cause odd parity within a character. If the total number of bits used in a character equals all even number (i.e., 4), bit 8 is pinched. The data portion of a character is utilized in constructing a word. The first character represents the last significant digit (LSD), and the following characters build up to the most significant digit (MSD) of the word. An illustration of the construction of a test address word follows.



b. Tape Reader Control. The TR can run forward, or reverse, at high or low speed. This capability is controlled by the TR control logic. The LCU front panel START push-button, in conjunction with the MODE switch, is used to start the tape. Depending on the position of the MODE switch (AUTO. MAJOR, or MINOR) at initialization, the TR either proceeds for-ward at low speed or begins a tape search operation. The AUTO position causes the entire test tape to be processed. The MAJOR and MINOR positions cause a tape search operation (for the selected major test) to be performed. During tape search. the TR is driven in the necessary direction and at the required speed, until the tape TA number equals the major test number selected on the front panel TEST NUMBER, /MAJOR SELECT thumbwheel (TW). That test (major) or tests (minor) are then performed. A tape search operation is also initiated upon receipt of a branch instruction from the tape (para 2-13). A sprocket strobe is generated in the TR control logic. During maintenance operations, logic is provided for controlling the TR from the internal test panel also.

(1) Auto mode. Auto mode control logic enables tape run control logic, which provides input, control signals to the TR. Pressing the START push-button, causes a proceed signal to be applied to logic enabled by the auto mode c0ontlol. The tape run control provides the necessary signals for the TR to run forward at low speed(TEST NUMBER/MAJOR SELECT) thumbwheel are inhibited during auto mode). The TR is now under control of the program tape and runs as directed.

(2) Major mode. Front panel TEST N[NII3ER/MIAJOR thumbwheel (TW) were used to manually select, the desired major test. Pressing the START push-button initiates a tape search operation. When the TA selected is higher than, the TA at which the tape is stopped, the T. will advance at high speed and overshoot the selected TA by approximately 5 inches of tape. The tape drive then reverses automatically, drives at high speed, and again overshoots the selected. TA by approximately 5 inches. The tape drive' advance-s the tape at low speed to the selected TA and he tape stops (fig. 2-27). If the T.A selected by the TW is less than the TA at which the tape is stopped, the TR will run in reverse at high speed, overshoot the selected TA by approximately 5 inches of tape, then run forward at low speed and stop at the selected TA.

Example: The test tape is stopped at TA = 40 and the selected address is TW = 50, the TR will advance at high speed and stop approximately 5 inches past TA = 50. The tape drive will reverse and rewind approximately 10 inches of test tape and stop. The tape drive will then advance at low speed until TW = TA = 50. If TA = 30 and TW = 20, the TR will run at high speed and reverse (rewind) and stop approximately 5 inches past TA = 20. The tape drive will then advance the test tape at low speed until TW = TA = 20.

The contents of the TA register represent the program tape major test number (BCD). The TW and TA numbers are compared to determine whether the TW number is less than, greater than, or equal to the TA number. If the TW number is greater than the TA number when the tape search start signal is received, the run and forward flip-flops are set (fig. 2-28). This condition causes the TR to run forward at high speed (phase 1). After receiving the next TA word, the TW and TA comparator is enabled. If the TW number is still greater, phase 1 continues. Due to the high speed of the TR, an overshoot occurs when a TW = TA (TR ready line) condition is detected. When the next TA number is received, the compare result strobe resets the forward flip-flop, causing high-speed reverse (phase 2) to be initiated. The overshoot recurs when a TW = TA condition is detected a second time (reverse run), and sets the forward and low flip-flops initiating low-speed forward (phase 3). When the TW = TA condition is detected a third time, the tape search flip-flop is reset; the TR stops.

Pressing the START push-button causes the selected major test to be performed. The TR stops at the completion of the test. Pressing the START push-button again, causes the tape search and test operation to be repeated. If a different test number has not been entered via the TW, the same major test is performed. If the tape search was initiated by a branch instruction, the tape search continues until the tape-selected minor test is located (refer to (3) below).

(3) Minor mode. With the MODE switch set to MINOR, pressing the START push-button, and then the STOP/RESET push-button, causes a tape search operation to be performed as in the major mode. At completion of the tape search operation, the first minor test (00) of the selected

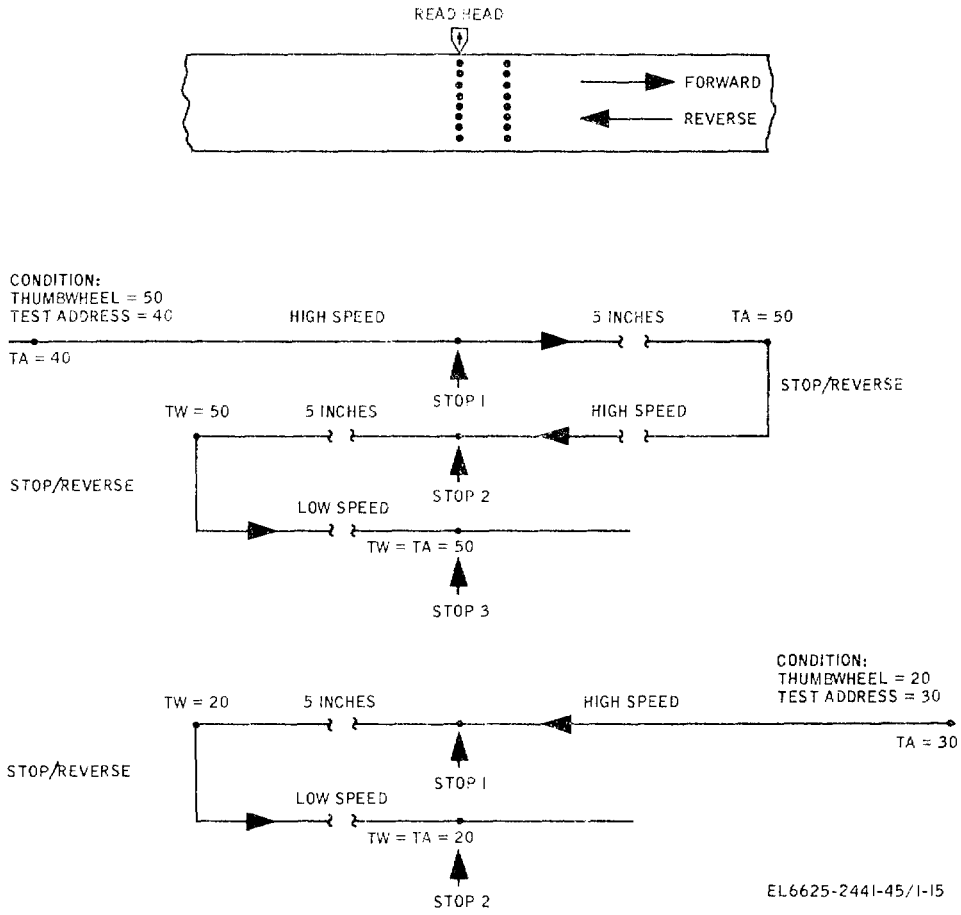


Figure 2-27. Tape direction, flow diagram.

major test (TW selected) is performed. The tape is stopped at the completion of the test, and the next minor test is initiated by pressing the START push-button. This action is continued until the last minor test has been completed. Pressing the START push-button, after completion of the last minor test, advances the tape to the next major test and at the completion of minor test 00, the tape stops.

(4) Sprocket strobe generation. Each time a sprocket hole is detected, the TR applies a signal to the tape control logic. A pulse is generated and used as a timing signal by the tape control and processing logic.

c. *Tape Error Detection.* Ii-process error checks are performed on each tape character received by the test set to insure the accuracy of each character read and transmitted by the TR. Tests performed check the horizontal and vertical parity, seventh-hole condition, format, buffer register, and tape character counter.

(1) *Horizontal parity check.* This test is performed to check whether the total number of bits used in each character is an odd number. Signals representing each bit of a character are received from the buffer logic and decoded to determine the total number of bits. If the total equals an even number, a no-go signal is applied to the error detection logic.

(2) *Vertical parity check.* An instruction to perform a vertical parity check is periodically received by the test set. This test verifies that the correct amount of bits have been processed over an extended period of time. The location of the instruction on the program tape is determined by the programmer. The instruction sets up control logic to test the state of the vertical parity register. The seven active tape bits (1, 2, 3, 4, 5, *6,* and 8) cause their respective flip-flops to toggle, when that bit position is punched. The programmer decides what additional tape characters are required to put the flip-flops in the reset state.

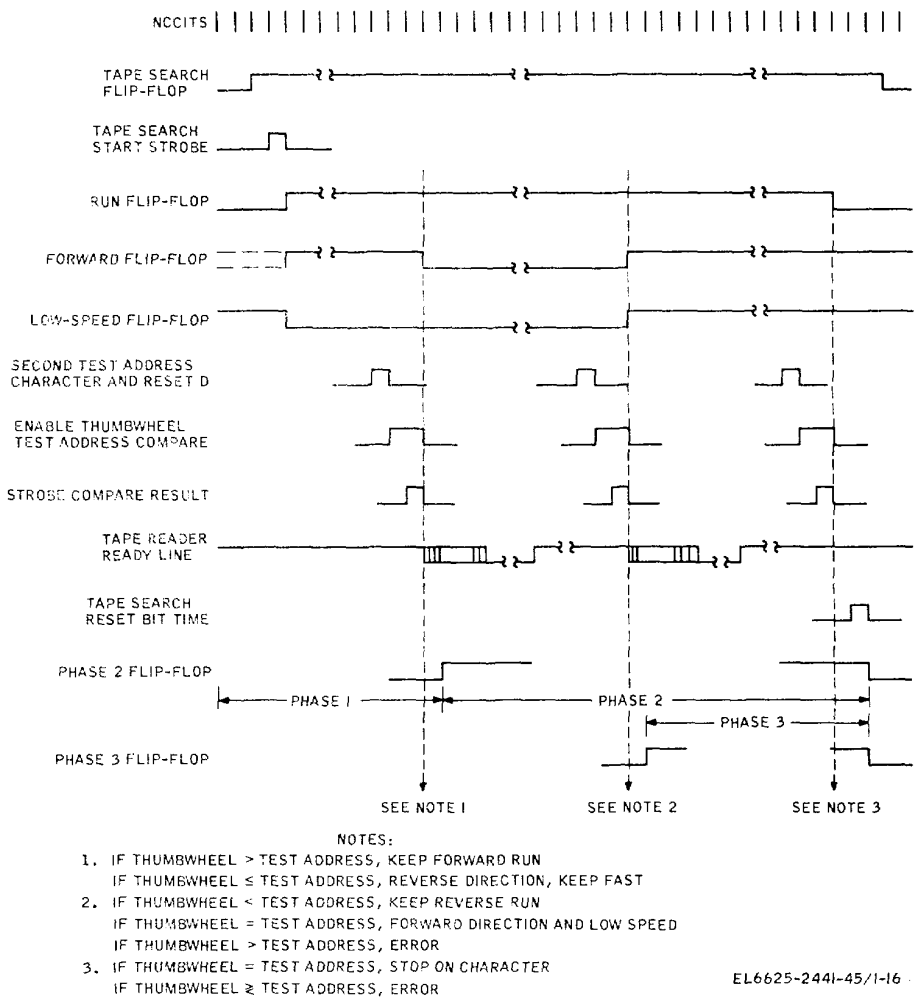


Figure 2-28. Tape search, timing diagram.

(3) Seventh-hole check. Logic is provided to detect a punched seventh-hole condition, which indicates an optional code delete.

(4) Tape format cheek. The tape format logic receives tape data (bits 5 and 6) and determines the type of word (TA, instruction, data, or end-of-data) to be processed. After the type of word has been determined, related logic in the tape processing logic is enabled. Format checks are made to insure the correct amount of characters in program words (fig. 2-29).

(5) Buffer register error check. This check is performed to determine whether the buffer register is functioning properly. Timing signals are received from the byte shift register, which causes bits 1 through 4 from the tape to be compared with the same bits as they are serially shifted out of the buffer register. For example, if the LSB loaded into buffer register is high, the first bit (LSB) shifted out is high. A comparison failure indicates a buffer register malfunction and causes the TEST SET FAULT indicator to light.

(6) Tape character counter. A tape character counter is provided to check the quantity of characters in a minor test. This counter is incremented one count by the instruction bit time (IBT) and counts to a maximum of 1, 023. Completing a 1, 023 count indicates that an error exists and causes the TEST SET FAULT indicator to light. The counter is reset at the

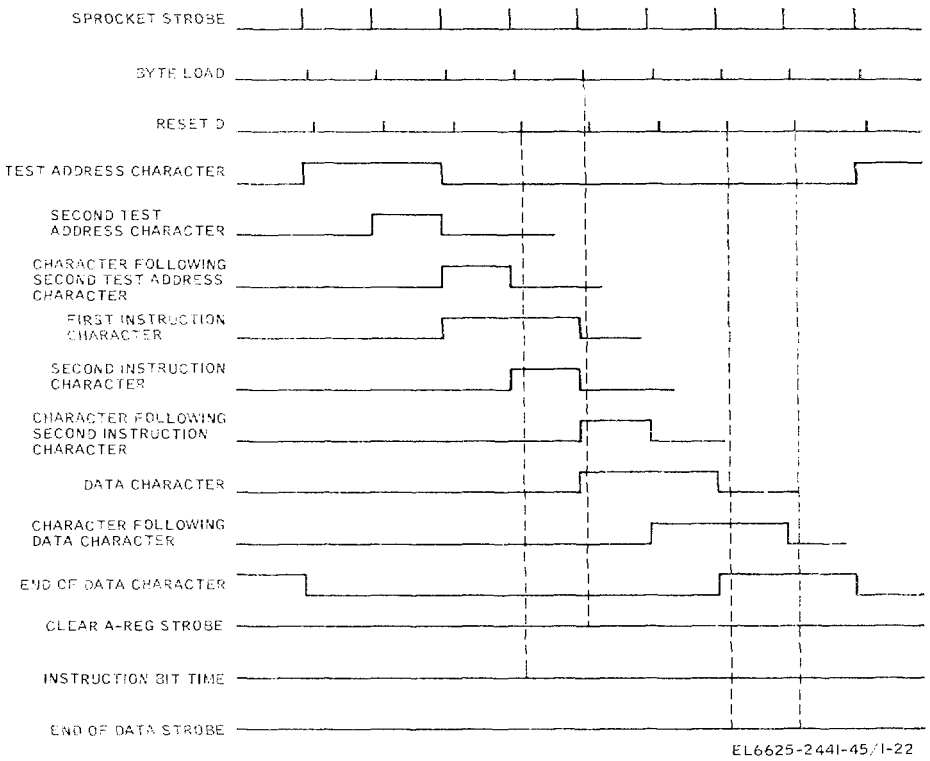


Figure 2-29. Typical tape format check, timing diagram.

beginning of each minor test by the increment minor test counter instruction.

d. Tape Character Processing. Program words are received by the buffer logic and applied to logic pertaining to that type of word. TA words are applied' trough the TA register to the TR control logic, to be used during tape search operation. TA words are also applied to the test set front panel,: displaying the major test being performed. An instruction word is applied' through 'the 'instruction' register, td the instruction decoder, minor test' counter tape character. counter, and the stop control. A data word is applied directly from the buffer logic to the A-register.

(1). Buffer logic.: The buffer logic receives parallel data from the TR. Additional logic- is provided receive data from the internal test panel, and to display that data during maintenance operations. The buffer logic applies the data to the error de6ction logic, and to the TA and instruction registers and the A-register. Depending on which register has been enabled by the tape format logic, the data is processed accordingly.

(2) Byte shift register (fig. 2-30). The byte shift register enables the sifting of the buffer, TA and interaction register. and the A-register, and controls the buffer register error check: The byte shift register contains four flip-flops (A, B, C; and D), and functions as a counter. At detection of a sprocket hole, the sprocket strobe causes the D-fib-flop to set for six phase S clock pulses. During this time, : A-, B-, and C-fib-flops set at each consecutive phase S clock pulse, then reset consecutively. The byte load pulse is generated when A-flip-flop sets, enabling the buffer register to be parallel loaded with data from the, tape. When the B-flip-flops sets, the shift four bits signal enables the buffer register to serially shift its contents into the TA or instruction registers or the A-register, and the buffer register error logic. At the sixth phase,clock pulse, the

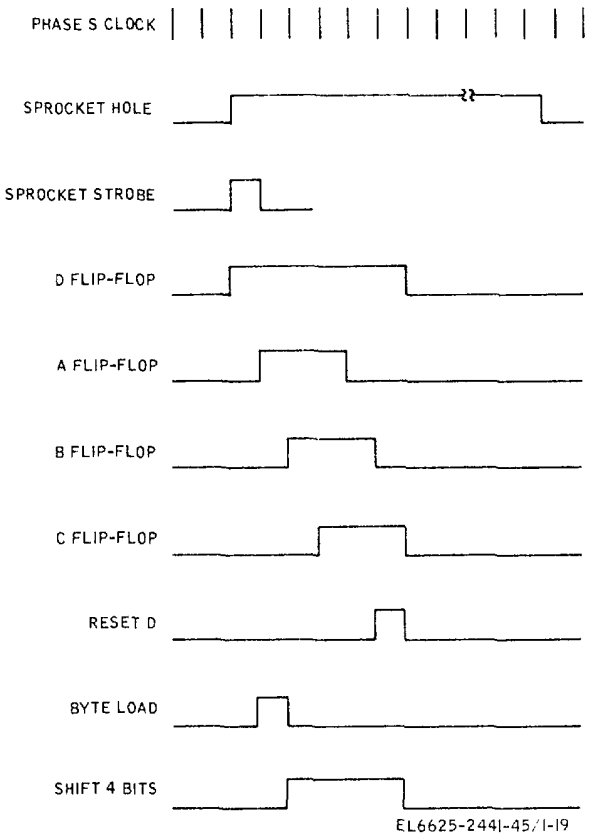


Figure 2-30. Byte shift register, timing diagram.

D-flip-flop and the shift four bits signal are reset by the reset D signal. Data cannot be loaded into the buffer register until the next sprocket hole detection (next character).

(3) TA register (fig. 2-31). Bits 5 and 6 (both true) of the TA word enable the TA register. Bits 1 through 4 of the tape character containing the LSD of the TA word, are parallel loaded into the buffer register. The buffer register serially shifts its contents to the LSD portion of the TA register, LSB first. When the second TA character is received, it is serially shifted into the MSD portion, MSB last. The contents of the TA register now comprise two BCD numbers which are converted, displayed on the front panel, and applied to the comparator logic (for tape search operation).

(4) *Instructions register* (fig. 2-32). Upon completion of a TA word processing, bits 5 (true) and 6 (false) enable the instruction register. Bits 1 through 4 of the first instruction character are parallel loaded into the buffer register, then serially shifted into the instruction register, LSB first. Bits 1 through 4 of the second character are serially shifted into the instruction register, iNSB last. The contents of the instruction register are decoded, and the instruction is processed. The following chart illustrates the octal number, code, and function of each instruction.

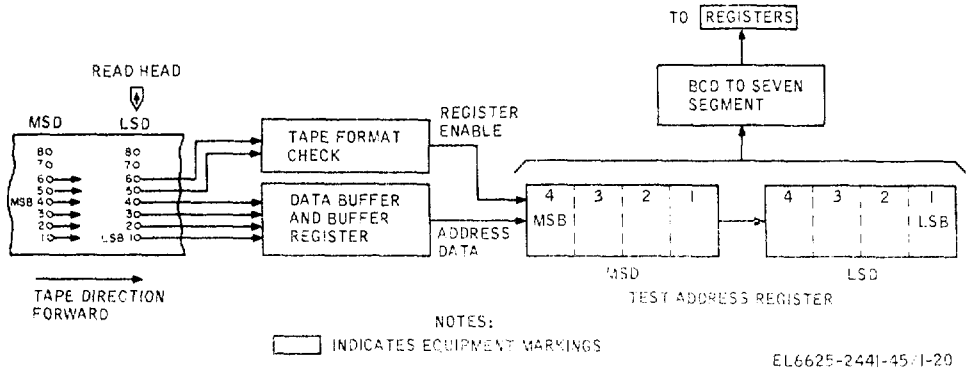


Figure 2-31. Load test address register, data *flow, block diagram.*

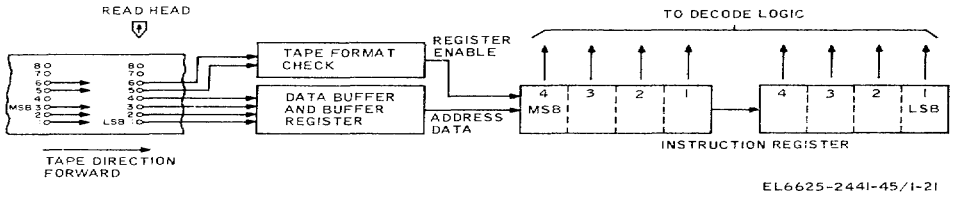


Figure 2-32. Load instruction register, data flow block diagram.

Octal no.	*Code*	*Function*
	General	
000	NOPE	Causes no test operation to occur. Used to cycle test set through instruction decode without a NCU/CIU test operation.
016	NOOP	Causes no test operation to occur. Used to cycle test set through instruction decode without a NCU/CIU test operation.
154	DNCU	Causes a latch to be set, which is AND-gated with the computer-power-on to energize the status indicator NCU. DNCU latch, with DCIU and DSTS latches, perform error checking to insure that the proper tape (computer, control-indicator, or self-test) is on the tape reader when the proper device is connected (computer, control-indicator, or self-test adapter) to the test set.
155 DCIU		Causes a latch to be set, which is AND-gated with the control-indicator-power-on to energize the status indicator CIU, Error checking as in DNCU.
156 DSTS		Causes a latch to be set, which is AND-gated with the self-test-adapter-connected to energize the status indicator SELF TEST. Error checking as in DNCU.
112 EOTF		Causes a flip-flop to be set, which inhibits any forward-run command to the tape reader. (EOTF flip-flop allows display of GO or NO GO lights at end-of-tape if MODE switch is at AUTO). Following EOTF instruction, if an auto mode, pressing STOP/RESET push-button will cause tape to search to major 00. (If START push-button is pressed, nothing will happen and the STOP/RESET push-button must be pressed twice.) If in major mode, the same operation will occur except a tape search to the thumbwheel will be initiated. When in the auto mode, the GO indicator will light at end-of-tape only if the tape ran through a TA of 00, MODE switch was left at AUTO, and the NO GO indicator did not light. If these conditions have not been met, the NO GO indicator will light at end-of-tape and auto mode.
107	EMJT	Causes tape to stop if MODE switch is at MAJOR.
177	INCM	Generates a pulse which increments the minor test counter displayed on test set LCU front panel. This pulse also resets the tape character counter to a one. This is the only instruction that is performed in branch mode.
111	STOP	Causes tape to stop; REGISTERS display is blank.
157	SDRG	Causes tape to stop; NO GO indicator lights and C-register is displayed in REGISTERS display.
	Test	
013	LDAB	Causes the transfer of 32 bits of data from A- to B-register after reading the end-of-data character. A-register remains unchanged. If one or more data characters follow the second instruction character, the A-register is cleared and then loaded with whatever data comes from tape, prior to the end-of-data character. This instruction causes four MSB of the B-register to biz ')3Jdod with a hex-A (1010), following the shift.

Octal no.	*Code*	*Function*
003	CMAB	Causes the comparison (logical-exclusive OR) of 32 bits of A- and B-register s to be loaded into the C-register after reading the end-of-data character. A- and B-registers remain unchanged. If a data character follows the second instruction character, the A-register is entirely cleared and then loaded with whatever data comes from tape, prior to the end-of-data character. If any bit fails to compare, the no-go flag is set. No-go flag was reset at start of instruction. The four MSB of A-register must be loaded from the tape with a hex-A (91010) to insure the A register is not programmed to saturate. Prior to this instruction, the four MSB of B-register will have been loaded with a hex-A (1010) by various instructions, to insure that B-register is not saturated. Four MSB of C-register should always be 0 after this instruction.
012	AANC	Causes the logical AND of 32 bits of A- and C-registers to be loaded into B- and C-.registers after reading the end-of-data character. A-register remains unchained. If a data character follows the second instruction character, the A-register is entirely cleared and then loaded with whatever data comes from tape, prior to the end-of-data character. If any true bit is loaded in C-register, the no-fla5 is set. No-go flag was reset at start of instruction. This instruction causes four .ISB of the B-register to be loaded with hex-A (1010), following AND.
	Branch	
022	UNBR	Causes test set to enter tape search mode and branch mode following The end-of-data character. Data loaded into A-register consists of major and minor numbers to which a branch is desired. If the major test number in A-register Is greater than the current major test number, tape reader runs forward. If less, tape reader runs in reverse direction. During tape search, tape runs at high speed- When a correct camper of the current major test number and the desired major test number occurs, tape search mode is terminated. Test set remains in branch mode and runs at low spread, ignoring all instructions but INCM, increment minor counter. unit a correct minor test compare occurs. Then branch mode is terminated and normal instruction execution returns. Branch mode may be terminated by pressing STOP/RESET push-button.
023	BRMJ	Causes test set to enter branch mode following end-of-data character In addition, tape search mode (reverse) is entered simultaneously if the desired minor test is less than or equals the current minor test. (See UNBR for tape search operation.) Only the desired minor test need be loaded into A-register, since the current major test number is in the major test register. If the desired minor test is greater than the current minor test, tape search is not entered, the tape continuing to run at low speed (forward) until the desired minor test is located, then branch mode is terminated and normal instruction execution returns.
024	BRNO	Causes test set to enter tape search mode and branch mode following , end-of-data character if the no-go flag is set. See UNBR for further operation. 'he data loaded into A-register following this instruction will he loaded as "long data" If the n0o-e flag is not set, and as "short data" if the no-go flea is set.
025	BNMIJ	Causes test set to enter branch mode 'following and-of-data character if the n0-go flag is set. See BRMJ for further operation. The data loaded into A-register followin g this instruction will be loaded as "long data" if the no-go flag is not set, and as "short data" if the no-go flag is set.
	Computer interface	
120	GINT	Causes either one or both interrupt request flip-flops to be se', according, so ant' byte of data loaded into the A-register. The request remains until the interrupt at '<niwledgc. signal is received from the computer.
117	RSET	Causes the generation of a computer reset signal. If the computer clock i1, on, the reset signal will last long enough for the computer to begin a reset cycle If the computer clock is off, (i.e., single clock mode), the computer reset signal will remain computer clock is tuned on for least one clock.

Octal no.	*Code*	*Function*
115	RCPC	Causes the computer clock to be turned on for an indefinite period of time. Clock may be stopped by either computer program or test set program control.
11	4RCNC	Causes the computer clock to be turned on for N (001 to 999) clocks conditionally. If, during the last nine counts of N, a memory cycle is begun, the clocks are stopped immediately.
113	RCNU	Causes the computer clock to be turned on for exactly N (001 to 999) clocks. If, during the last nine counts of N, a memory cycle is begun, the memory inhibit signal is activated for the duration of the remaining clocks.
116	STCL	Causes computer clock to stop immediately after the second instruction character is read.
	Input/ output interface	
010	DEIP	Operates on the assumption that prior to the occurrence of end-of-data character, the computer program has performed DEIP instruction. With this condition met, the end-of-data character initiates the serial shift of the 28 low-order bits of the A-register to the EB, It is assumed that the 28 bits were loaded from tape previous to the end-of-data character; however, it is not a requirement. A-register remains unchanged.
004	RMBA	Causes the computer MB register (via NAD lines) to be read in parallel into the A-register, right justified, following the end-of-data character.
	CIU interface	
001	CIU	Requires 32 bits of data to be loaded into A-register from tape. Following the end-of-data character, serial shift of the A-register to the control-indicator is initiated.
002	CIU2	Requires four bits of data, address information, to be loaded into A-register from tape. The four address bits are shifted to the control-indicator following the end-of-data character. After the fourth bit is transmitted, the B-register is shifted for 28 bit-times, open ended. The control-indicator either receives or sends 28 bits of information, depending upon whether the fourth address bit is a 0 or a 1, respectively. This instruction causes the B-register to be loaded with a hex-A (1010) in the four MSB, following the shift.
130	CIU3	Causes a latch to be set which supplies a ground signal to the control-indicator MODE switch wiper. Position of the MODE switch is now displayed in the REGISTERS display. The nine right-most digits correspond to the nine positions of the MODE switch. Active display condition will be an eight; inactive, either a blank or zero. This instruction will normally be followed by a stop instruction.
	Platform interface	
035	GSP1	Verifies that the proper incremental platform angles are developed on tray 4 of the computer.
036	GSP2	Determines the capability of tray 4 to count incremental velocity pulses.
037	GSP3	Checks the operation of the self-test features that enable the AV registers to count torquing pulses.
	Flags	
026	SIOC	Sets I/O complete
027	RIOC	Resets I/O complete
030	SSIO	Sets serial I/O control
031	RSIO	Resets serial I/O control

Octal no.	*Code*	*Function*
032	SSID	Sets serial input data
033	RSID	Resets serial input data
122	SINM	Sets inhibit memory control
123	RINM	Resets inhibit memory control
131	SINP	Sets inhibit proceed
132	RINP	Resets exhibit proceed
i 33	SCWM	Sets clear-write memory
1:3-1	RC	Resets clear-write memory
135	SIIC	Sets inhibit increment CP
136	RIIC	Resets inhibit increment CP
137	SINC	Sets initiate instruction cycle
140	RINC	Resets initiate instruction cycle
141	SICP	Sets increment CP
142	RICP	Resets increment CP
	Read-Compare	
160	RCAA	
161	RCAA	
162	RCAQ	
172	RCCA	
166	RCCE	
167	RCCI	
171	RCCM	Sets a latch immediately (any instruction) Control logic waits until a data character is programmed after the instruction. The A-register is then cleared and loaded with tape data.
173	RCEA	If a data character is not programmed, A-register remains unchanged. Following the
170	RCEA	end-of-data character, the desired computer register is parallel loaded into the B-register and
	RCEB	compared with the contents of the A-register, the result being loaded in C-register. If any bit
175	RCFM	fails to compare, the no-go flag is set. The no-go flag was reset at the beginning of Destruction.
175I	TCFM	These instructions cause B-register to be loaded with a hex-A (1010) at the tune of the read. To achieve a true compare, A-register should be loaded with a hex-A (1010) in the four MSI'
165	RCMA	
1633	RCMB	
164	RCCP	
017	RCPJ	
174	RCXM	
125	RCW1	

Octal no.	Code	Function
126	RCW2	
127	RCW3	
176	RCEX	(Refer to pace 2-414)
020	RCDW	
124	RCM1	
021	RCM2	
007	Load LACW	Causes data loaded in the A-register to be transferred to B-register. The B-register is then gated to analog channel control logic, permitting the testing of computer analog channels. If data characters are not programmed, the A-register data is not transferred to the B-register and B-register is not Gated to analog channel control logic.
014	LQJD	Causes three bits of data loaded in 'he A-register to be transferred to a holding register, which applies address information to the three QJDXX lines The holding register will be cleared after three phase C clocks, which may be under program control when this instruction is performed
144	LDCAX	Causes a clear and load operation to be performed on the specified computer register. Data is loaded in parallel.
145	LDCE	
146	LDCI	
147	LDCM	
143	LDCP	
151	LDMB	
152	LXMB	Causes a clear and load operation to be performed on the computer MB register, via the XMBXX lines. Data is loaded in parallel.
034	LDSI	Causes data in A-register to be loaded into the discrete input holding register Signals from the holding register supply levels to the computer which simulate all of the system discrete.
100	Memory MFIL	Sets up control logic to fill or verify a block of memory (up to 1, 024 words). First operand loaded into the A-register is the starting CP address, which is loaded into the computer CP register following the first end-of-data character. Simultaneously, the computer CM register is loaded with count S, in preparation for a memory cycle. The following operands, loaded into the A-register from tape, are memory data. Memory fill operation will be described prior to memory verify. During memory fill, A-register data is loaded in parallel into the MB register. A clear-write memory cycle is initiated to write the data into the location specified by the CP register. The CP register is then incremented one count, another operand enters the A-register from tape and is loaded into he NIB register. and another memory cycle is initiated. Similar operations continue until a SMFL instruction is performed. During memory verify, following the loading of the A--register, a read-restore memory cycle is initiated which transfers memory data into the NIB register The MB register is then loaded into the B-register and compared (logical-exclusive OR) to A-register data. Following the compare, a second read-restore is initiated This is to verify the first restore operation. The MB register is again loaded into the B-register and a second compare is made. If the compare fails, the no-go flag is set and the tape stops. The current value of CP register will be in the REGISTERS display. If the STOP/RESET push-button is pressed, the display will show the C-register, which contains the result of' the compare. If a failure does not occur, the CP register is incremented one count, another operand enters the A-register, two read-restore-and-compare cycles are performed. Similar operations continue until a SMFL instruction is performed.

Octal no.	Code	Function
110	HMFL	Same as MFIL, however, tape runs at high speed. Used for loading large blocks of data.
101	SMFL	Causes either a memory fill or memory verify mode to be terminated immediately. Tape reader continues to run, but shift to low speed.
102	SLMA	Causes first operand (memory address) loaded into the A-register to be loaded into the CP register, following the first end-of-data character. Simultaneously, the CM register is loaded‘ with count 8 in preparation for a memory cycle. A second operand may follow the first end-of-data character. Following the second end-of-data character, the A-register is loaded in parallel into the MB register and a clear-write memory cycle is initiated to write the data into the location specified by the CP register.
153	SLMC	Causes first operand (memory address) loaded into the A-register to be loaded into the C-register ,following the first end-of data character. Simultaneously, the CM register is loaded with count 8 in preparation for a memory cycle. A second end-of data character, which must follow the first, causes the C-register to be loaded in parallel into the MB register, and a clear-write memory cycle to be initiated to write the data into the location specified by the CP register.
104	SREM	Causes operand (memory address) loaded into the A-register to be loaded into CP register, following the end-of-data character. Simultaneously, the CM register is loaded with count 8 in preparation for a memory cycle. After the CP and CM registers have been initialized, a read-restore memory cycle is initiated to read memory data from the location specified by CP register into the MB register.
105	LVWC	Causes first operand (memory address) loaded into the A-register to be loaded into the CP register, following the first end-of-data character. simultaneously, the CM register is loaded with count 8 in preparation for a memory cycle. The second operand must be programmed an alternating 1-0 pattern. Following the second end-of-data character, the tape reader is stopped and the A-register loaded in parallel into the MB register. A de-write memory cycle is initiated to write the data into the location specified by the CP register. The CP register is then incremented one count, A-register is shifted right (end around) one bit, and another clear-write memory cycle is initiated. similar operations continue until the 10 low-order bit of the CP register are saturated, signifying that a 1,024-word block of memory has been loaded. Verification of the loaded data now begins. The CP register has been cleared. A read-restore memory cycle is Initiated to read the data from the location specified by the CP register into the MB register. The MB register is then loaded into B-register and compared (logical-exclusive OR) to data remaining in A-register. A second read-restore cycle is initiated, to check the first restore, and is then followed by a compare. If any comparison fail, the no-go flag is set and remains set. Following the two compares, the CP register is incremented one count and A-register is shifted right (end around) one bit. Similar operations continue until the 10 low-order bits of the CP register are saturated, signifying that a 1,024-word block has been verified. The tape reader is restarted, and the program checks, via a branch (BRNO or BNMJ), whether the no-go flag was set.
106	MVET	Causes tape reader to go into tape search mode for major test address 00. Within this major test and subsequent major tests, it is assumed there are MFIL instructions. However, the MVET instruction causes the MFIL instruction to operate in memory verify, rather than memory fill mode. After the MVET instruction is read a second time, an automatic tape rewind is performed.
	Test	
005	TST1	Requires the loading of up to 40 bits of self-test data into a self-test register located in the LCU and SCU. Self-test bits are assigned functions which in general control data paths. Following the loading of the self-test register, a number of data paths have been closed, the net effect being that some data (registers or test point) will be present at the parallel input of the B-register. A clock strobe is produced, loading the B-register with whatever data was present, and clearing the self-test register. The B-register may now be compared with the expected result, via the CMAB instruction.

Octal no.	*Code*	*Function*
006	TST2	Requires the loading of up to 40 bits of self-test data into a self-test register located in the LCU and SCU. Self-test bits are assigned functions which in general control data paths. Following the loading of the self-test register, a number of data paths have been closed, the net effect being that some data (registers or test points) may be present at the parallel inputs of the B-register. The self-test bits, in self-test mode 2, may also control logic not directly concerned with loading data into the B-register. Assuming, first, that the B-register is to be loaded, the loading takes place by a non-self-test instruction being performed. In self-test mode 2, the performance of certain register instructions will cause data to appear at the inputs of the B-register, and will also initiate a load strobe to clock the B-register. The self-test register will be cleared by the strobe. The B-register may now be compared with the expected result, via the CMAB instruction. Self-test mode 2 may also control or simulate logic operations that do not require the B-register being loaded in parallel. In this case, a load strobe is not generated. Following whatever logic operation is performed, the B-register will in general be loaded serially. The B-register may now be compared with the expected result, via the CMAB instruction.
103	TST3	Causes the self-test of the self-test register. The operand following the instruction will consist of 72 bits, arranged as 18 data characters. The data will be loaded byte se rially into the self-test register and the A-register simultaneously. After eight bytes (data characters), the A-register is loaded. Shifting continues, however, with the least significant data being lost. At the completion of the 10th byte, the self-test register is loaded. Beginning with the 11th byte, the output of the A-register and self-test register are compared (logical-exclusive OR) bit serially. If any bit fails to compare, the TEST SET FAULT indicator lights, the tape reader sops, and the REGISTERS display shows the internal error register. The display can be interpreted by referring to TM 11-6625-2441-12, and should indicate that the error is in the self-test register.
121	EVPC	Sets up control logic to test the state of the vertical party register, following the end-of-data character. Each of the seven active tape channels (1, 2, 3, 4, 5, 6, 8) cause its respective flip-flop, in the vertical parity register, to toggle each time the channel is in the t rue state. The tape assembler program keeps track of the parity of each channel. When an EVPC instruction is programmed, the assembler decides what additional tape character, either data or end-of-data, is required to cause the vertical parity register to reach the 0000000 state following the end-of-data character. The register is checked, and if not all O's, the TEST SET FAULT indicator lights, the tape stops, and the REGISTERS display shows the internal error register. The display should indicate that a vertical parity error exists.

(5) Data word A data word, consisting of 1 to 28 bits, is applied directly to the A-register to be processed per the preceding instruction. At the end of the data word, an end-of-data pulse is generated and the instruction is processed.

(6) Minor test counter. This counter provides the number of the minor test for display. The counter is incremented one count by an increment minor test counter instruction, and resets at the beginning of a major test.

2-21. Program Listing

The program listing, appendix B, is a graphic presentation of the self-test program tape. Correlation between the test set TEST NUMBER MAJOR MINOR indicator and the listing will provide information such as test description, test

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Scope

General support maintenance includes troubleshooting and removal and replacement procedure for the test set. Troubleshooting procedure include charts for troubleshooting and resistance measurements. Removal and replacement procedures are for discrete components an' assemblies of the test set. In the removal an(replacement procedures, when full reference designations are used in paragraph headings, references to the same item within that paragraph will be abbreviated.

3-2. Test Equipment, Tools, and Materials Required

a. Test Equipment. The following chart lists all test equipment essential for troubleshooting the test set.

Item	*Manufacturer and part no.*	*Use*
Voltmeter (DVM)	Non Linear Systems Model X-2	Verifying predetermined voltage measurements.
Oscilloscope AN/USM-281A (with Plug-In Units PL--1186/USM-281A and PL-1187/USM-281A).		Displaying test signal waveforms; measuring frequency and voltage.
Tape Reader AN/USA-34.		Transferring information from the diagnostic and test tapes to the test set.
Multimeter AN/USM-223.		Checking voltages, continuity. and resistance during trouble-shooting.

b. *Tools.* The following tools are essential for maintenance of the test set.

Item	*Manufacturer and part no.*	*Use*
Too] kits TK-100/G, TK-105/G, and TK-90/G.	.....	Providing tools for general use.
Crimping tool.	Daniels MH750	Attaching wire to replacement pins for Bendix and Hughes type connectors.
Termi-Point service tool.	AMP 69535	Attaching wires to AIP type connector pins using clips.

Item	Manufacturer and part no.	Use
Mandrel.	AMP 69545-1	Used with Term-Point service tool to accommodate 2n-gage wire_ and AMP 67042-2 clips.
Extractor-locator tool.	AMP 69357-5.	Removing clips from damaged AMP type connector pins, re-locating clips and wares still attached to connector pins.
Pull test tool.	AMP 69358-6.	Inspecting Term-Point Terminations.
Removal tools.	Bendix 11-8675-16, 11 -867 5 -20, 11-8675-22, 11 -8675-24	Removing damaged pins from Bendix type connectors.
Insertion tools	Bendix 11-8674-16,) 11 -8674 -20, 11-8674 -222, 11 -8674 -24	Inserting replacement pins in Bendix type connectors.
Contact locator heads.	Bendix 11-8673-4, . 11-8673-6, > 11-8673-7)	Used in conjunction with Bendix removal and insertion tools (installed in crimping tool M3H750).
Torque wrench.	Torque Controls, Inc. Kit 2.	Torquing of hardware.
Insertion tool,	Hughes TW0221TOOO.	Inserting replacement pins in Hughes type connectors.
Removal tool. T.	Hughes Hughes type connectors.	Removing damaged pins from
wire stripper.	GGG-S-793A.	Stripping insulation from wires.
Wire stripper. Model 100.	K. Miller	Trimming wire, for use wit]h ' termi-Point service tool.
Heat gun.	Master Appliance HG-751J.	Shrinking heat-shrinkable sleevin4.

c. materials. The following materials are essential for maintenance of the test set.

Item	FSN	Use
Cleaning compound.	7930-395-9542.	Cleaning solder connections.
Lint-free cloth.	8305-170-5062.	Cleaning equipment.
Camel's hair brush (commercial).		Cleaning solder connections.
Acetone (0-A-51D).		Cleaning mechanical parts.
Insulation sleeving, electrical, heat-shrinkable (MIL-I-23053).		Providing electrical isolation between connector pins; supporting small-gage wires.

Item	*FSN*	*Use*
Sealant, grade C (Loctite, MIL-S-22473).		Locking (liquid used in lieu of mechanical locking device).
Perchloroethylene (commercial).		Cleaning electrical parts.
Freon (PCA).		Removing residue left by other cleaning compounds

SECTION II. TROUBLESHOOTING

3-3. Troubleshooting Procedures

Troubleshooting the test set at general support maintenance is a continuation of the organizational maintenance troubleshooting procedures contained in TM 11-6625-2441-12. Since all plugging modules, indicator lamps, and switch knobs are replaced at organizational maintenance, the general support maintenance troubleshooting chart isolates malfunctions to discrete components and cables. The sequence numbers in the troubleshooting chart are keyed to the sequence numbers in the daily preventive maintenance checks and services chart in TM 11-6625-2441-12. The Corrective action column lists discrete components which could cause the trouble indication. In all tests, the possibility of intermittent troubles should not be overlooked. If this type of trouble is present, it may be made to appear by tapping or jarring the equipment. Make a close inspection of the wiring and connections in the units of the test set. Continuity and resistance measurements, referenced to the wire and circuit lists in appendix C, volume 2 and various figures in chapter 5, should be used to locate faulty wiring and connections. Upon completion of repairs, perform the self-test procedures in TM 11-6625-2441-12. The self test program listing may be used as an aid in following the operation of the self-test tape.

3-4. Troubleshooting Chart

Step no.	Trouble symptom	Procedure trouble	Corrective action
3	Switch does not work smoothly	Faulty switch	Replace switch (para 3-7, 3-8, 3-18, 3-29, 3-32, 3-33, or 3-35)
4	Trouble symptoms are as follows:		
	a. SCU blowers not operating.	a. Probable troubles are as follows: (1) Faulty blower 2AlBl, B2, or B3. (2) Faulty capacitor 2A1 C1, C3, or C4. (3) Faulty hybrid 2A1HY2 (4) Faulty circuit breaker 2A1CB4.	a. Corrective actions are as follows: (1) Replace blower 2AlBl, B2, or B3 (para 3-14 and 3-15). (2) Replace capacitor 2AlCl, C3, or C4 (para 3-16) (3) Higher level of maintenance. (4) Replace circuit breaker 2A1CB4 (para 3-13).
	b. LCU blowers not operating.	b. Probable troubles are as follows: (1) Faulty blower 1A1B1 or B2.or	b. Corrective actions are as follows: (1) Replace blower lAlBl B2 (para 3-38).

Step no.	Trouble symptom	Procedure trouble	Corrective action
		(2) Faulty capacitor 1A1 C1 or C2.	(2) Replace capacitor lAlC1 or C2 (para 3-39).
		(3) Faulty hybrid 2A1HY1	.(3) Higher level of maintenance.
		(4) Faulty circuit breaker 2A1CB4.	(4) Replace circuit breaker 2A1CB4 (para 3-13).
	c. POWER PRIMARY indicator does not light	c. Faulty indicator assembly .2AIDS5 or capacitor	c. Replace indicator assembly 2A1C2.2AlDS5 (para 3-6) or capacitor 2A1C2 (para 3-16)
	d. POWER AC indicator dose not light	d. Probable troubles are as .follows: (1) Faulty indicator assembly 2AlDS4.bly	d. Corrective actions are as follows: (1) Replace indicator assem- 2AlDS4 (para 3-6).
		(2) Faulty POWER AC switch 2A1S3	(2) Replace switch 2A1S3 .(para 3-18).
5	Trouble symptoms are as follows:		
	a. POWER TEST SET indicator does not light.	a. Probable troubles are as follows: (1) Faulty indicator assembly 1A1A5DS11.bly	a. Corrective actions are as follows: (1) Replace indicator assem- 1A1A5DS11.
		(2) Faulty TEST SET switch 1A1A5S7.	(2) Replace switch lAlA5S7 (para 3-32).
	b. TEST NUMBER indicator does not display MAJOR 00 MINOR 00 and REGISTERS display is not blank	b. Probable troubles are as follows: (1) Faulty TEST NUMBER .indicator assembly(s) 1A1A5DS8A through 1A1A5DS8D.	b. Corrective actions are as follows: (1) Replace indicator assembly(s) lAlA5DSSA through 1A1A5DS8D (para 3-30).
		(2) Faulty REGISTERS display indicator assembly(s) 1A1A5DS7A through 1AlA5DS7L.	(2) Replace indicator assembly(s) 1AIA5DS7A through l1AA5DS7L (para 3-30).
	c. Tape drives off reel in forward direction.	c. Faulty START switch 1A1A5S2	c. Replace switch lAlA5S2 (para 3-29).
	d. Tape drives off reel in reverse direction.	d. Faulty component board 2A1A4.2A1A4	d. Replace component board (para 3-17).
	e. Tape drives in forward or reverse direction and stops.	e. Faulty component board 2A1A4.2A1A4	e. Replace component board (para 3-17).
6	Any or all SCU indicators do not light.	Probable troubles are as follows:	Corrective actions are as follows:
		(1) Faulty LAMP TEST switch 2A1S2.	(1) Replace switch 2A1S2 (para 3-8).
		(2) Faulty SCU indicator assembly(s).assembly(s)	-(2) Replace SCU indicator (para 3-6).
		(3) Faulty component board 2A1A4.2A1A4	(3) Replace component board (para 3-17).

Step no.	Trouble symptom	Procedure trouble	Corrective action
7	Trouble symptoms are as follows:		
	a. Any or all LCU indicators do not light.	a. Probable troubles are as follows: (1) Faulty LAMP TEST switch 1A1A5S8. (2) Faulty LCU indicator assembly(s).assembly(s)	a. Corrective actions are as follows: (1) Replace switch lAlA5S8 (para 3-29). (2) Replace LCU indicator (para 3-28).
	b. REGISTERS display does not indicate all 8's.	b. Faulty REGISTERS display indicator assembly(s) 1A1A5DS7A through 1A1A5DS7L.	b. Replace indicator assembly(s) 1A1A5DS7A through 1A1A5DS7L (para 3-30).
	c. REGISTERS display is blank and TEST NUMBER indicator displays MAJOR 00 MINOR 00.	c. Faulty component board 2A1A4.2A1A4	c. Replace component board (para 3-17).
8	Any or all voltages not present	Faulty VOLTAGE MONITOR or not as specified.	Replace switch 2A1Sl (para switch 2A1S1.3-37).
9	Trouble symptoms are as follows:		
	a NCU POWER 115 VAC, 400 Hz indicator does not	a. Faulty NCU POWER 115 VAC, 400 Hz circuit breaker light.	a. Replace circuit breaker 2AICB1 (para 3-13). 2AlCB1.
	b. Oscilloscope indication not as specified or not present (73.6 (±7.4)V p-p).	b. Probable troubles are as follows: (1) Faulty SCU NCU POWER 115 VAC, 400 Hz circuit2AlCB1 breaker 2A1CB1. (2) Faulty VOLTAGE MONITOR switch 2A1S1. (3) Faulty transformer 2AlTl. 2A1T1	b. Corrective actions are as follows: (1) Replace circuit breaker (para 3-13). (2) Replace switch 2A1S1 (para 3-7). (3) Replace transformer (para 3-20).
	c. NCU POWER 28 VDC indicator does not light.	c. Faulty NCU POWER 28 VDC circuit breaker 2A1CB2.2A1CB2	c. Replace circuit breaker (para 3-13).
	d. DVM indication not and. specified .switch	d. Faulty VOLTAGE MONITOR 2AlS1	d. Replace switch 2A1Sl .(para 3-7).
10	Trouble symptoms are as follows:		
	a. CIU POWER 28 VDC indicator does not light.	a. Probable troubles are as follows: (1) Faulty component board 2A1A4.2A1A4 (2) Faulty CIU POWER 28 VDC circuit breaker2A1CB3 2A1CB3.	a. Corrective actions are as follows: (1) Replace component board (para 3-17). (2) Replace circuit breaker (para 3-13).
	b. DVM indication not as specified.	b. Faulty VOLTAGE MONITOR switch 2AlSl.	b. Replace switch 2AIS1 (para 3-7).

Step no.	Trouble symptom	Procedure trouble	Corrective action
11	Trouble symptoms are as follows:		
	a. Tape does not drive	a. Probable troubles are as follows: (1) If replacement of card 1A1A3A (25, 29) did not correct trouble, probable trouble is faulty oscillator 1A1Y1	a. Corrective actions are as follows: (1) Replace oscillator 1A1Y1 (para 3-40),
		(2) If replacement of card 1A1A1A (8, 16, 17) did not correct trouble, probable trouble is faulty STOP/RESET push-button switch 1 A1 A5S3.	(2) Replace switch iAlA5S3 (para 3-29).
		(3) If replacement of card 1A1A2A (23, 24, 25) did not correct trouble, probable trouble is LCU/ SCU cables.	(3) Check continuity (para 3-5, fig. 5-8 or 5-9) and replace faulty cable or connector (para 3-41 through 3-47)).
		(4) If replacement. of card 1A1A1A (6, 16, 18, 19, 20, 22) did not correct trouble, probable trouble is START push-button switch 2A1A5S2.	(4) Replace switch 2A1A5S2 (para 3-29).
	b. TEST NUMBER minor indicator steps correctly but REGISTERS display is not as specified.	b. Faulty SCUILCU cables.	b. Check continuity (para 3-5, fig. 5-8 or 5 -9) and replace faulty cable or connector (para 3-41 through 3-47).
	c. TEST NUMBER indicator and REGISTERS display step correctly but when tape stops, indications are not as specified.	c. Faulty TEST NUIBER indicator assembly lAlA5DS8C or D.	c. Replace indicator assembly 1A1A5DS8C or D (para 3-30).
14	TEST NUMBER indication not as specified.	Faulty TEST NUMBER indicator assembly lAlA5DS8C or D.	Replace indicator assembly lAlA5DSSC or D (para 3-30).
16	Tape does not drive.	Faulty STOP/RESET switch	Replace switch 1A1A5S3 (para

3-5. Adapter, Self Test MS-8586/ ASM-386 3A4, Continuity and Resistance Measurements (fig. 3-1 and 5-8)

Refer to figure 3-1 for location and reference designations of the self-test adapter resistor come ponents. Use the test equipment specified if paragraph 3-2 for measurement of resistive loads The following chart lists the resistors and values.

Resistor	*Value (ohms)*
R1	200
A1R2	300
A1 R3	100
A1R4	1, 000
A1R5	47, 000
A1R6	4, 000
A1R7	4, 000
A1R8	2, 000

Resistor	value (ohms)		
		AIR12	2,000
		AIR13	680
AiR8	2,000	AIR14	300
AIR9	2,000	AIR15	2,490
AiR10	2,000	AIR16	2,490
AIR11	2,000	AIR17	100

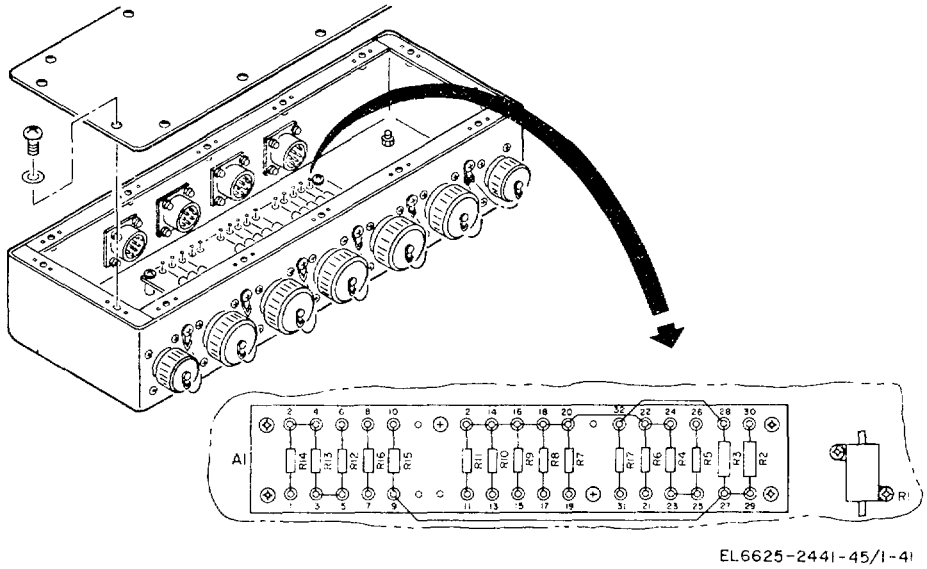


Figure 3-1. Adapter, Self Test MXI-8586/ASMf-386, resistor location diagram.

Section III. REMOVAL AND REPLACEMENT

3-6. Removal and Replacement of Indicators 2AIDSI through 2AIDS9

(fig. 3-2)

The following removal and replacement procedures apply to DS1 through DS5 (front panel) and DS6 through DS9 (test panel).

a. Removal

(1) Loosen 12 stud nuts (1) that secure chassis assembly (2) to combination case.

NOTE

Card cages 2AlAl and 2A1A2 are connected mechanically. Captive screws on both card cages must be loosened and card cages opened together

(2) Loosen required number of captive screws (3) that secure card cage(s) (4) to chassis assembly (2) and swing card cage(s) open.

(3) Tag and unsolder wires from terminals of faulty indicator.

(4) Remove nut (5) and lockwasher (6); remove indicator (7) and 0-ring (8) from front panel (9) or test panel (62).

b. Replacement

(1) Attach 0-ring (8) and indicator (7) to front panel (9) or test panel (62) with lockwasher (6) and nut (5).

(2) Solder tagged wires to proper terminals of replacement indicator.

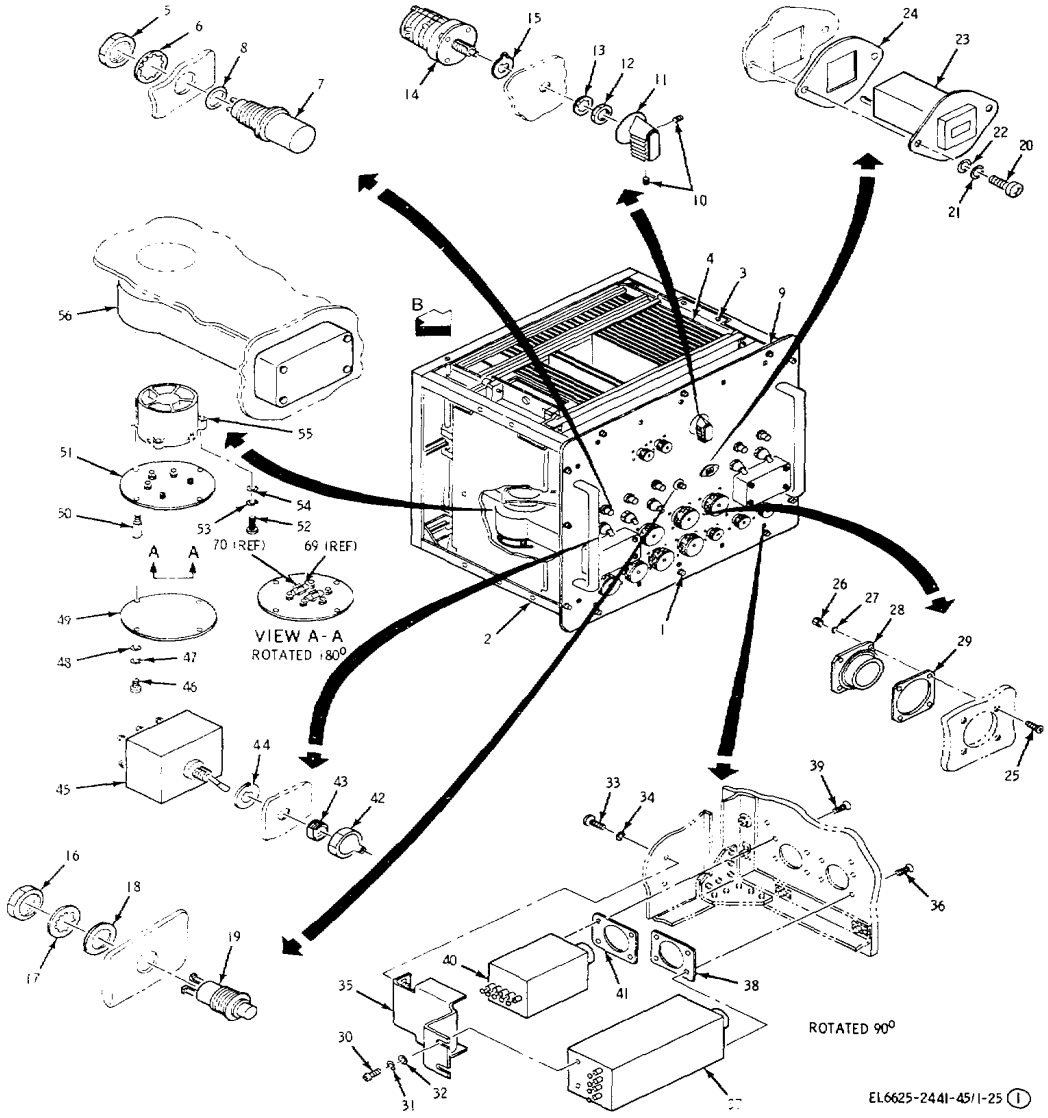


*Figure 3-20 (**1**). Signal Conditioning Unit TS-2913/ASM-386, exploded view (part 1 of 3)*

1	Stud nut (12)	20	Screw (4)	38	Emi gasket
2	Chassis assembly	21	Lockwasher (4)	39	Screw (4)
3	Captive screw (6)	22	flatwasher (4)	40	Filter 2A1J1
4	Card cage (3)	23	Elapsed-time meter (2; 2A1M1, lAIA5Ml)	41	Emi gasket
5	Nut (9)			42	Boot (4)
6	Lockwasher (9)	24	Emi gasket (2)	43	Boot adapter (4)
7	Indicator (9, 2AIDS1 through	25	Screw (40)	44	Keywasher (4)
2	AIDS9	26	Nut (40)	45	Circuit breaker (4, 2AlCB1 through
8	0-ring (9)	27	Nut (40)		2A1CB4)
9	Front panel	28	Connectors (10, 2A1J3 through	46	Screw (4
10	Setscrew (2)		2A1J2)	47	Lockwasher
11	Knob	29	Emi gasket (10)	48	flatwasher (4)
12	Nut	30	Nt (2	49	Protection plate
13	Lockwasher	31	Lockwasher (2)	50	Spacer (4)
14	Switch 2A1S1	32	Flatwasher (2)	51	Air inlet duct cover
15	Keywasher	33	Screw (2)	52	Screw (3)
16	Nut	34	Flatwasher (2)	53	Lockwasher (3)
17	Lockwasher	35	Filter support bracket	54	flatwasher (3)
18	Flatwasher	36	Screw (4)	55	Blower 2A1Br
19	Switch 2A1S2	37	Filter 2A1J2	56	Air inlet duct

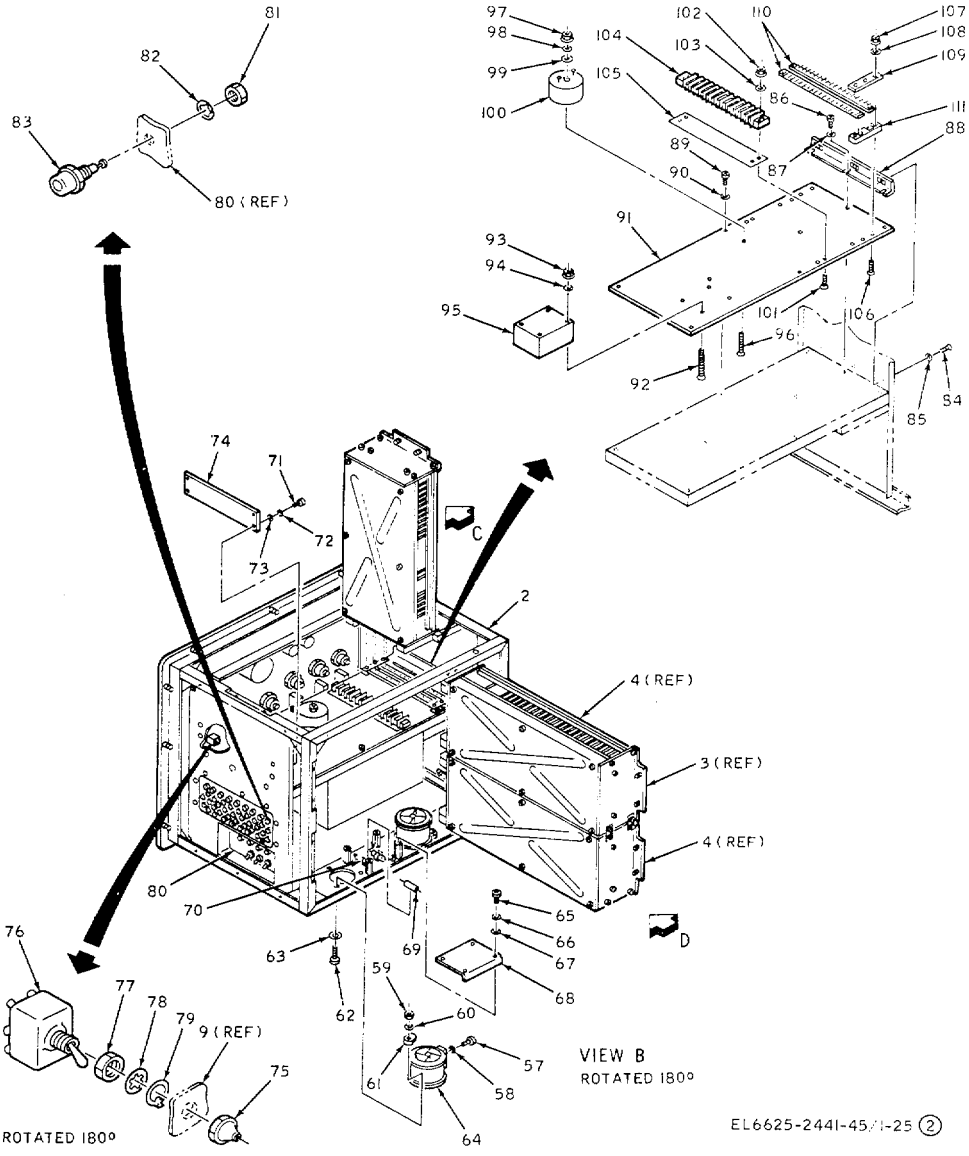
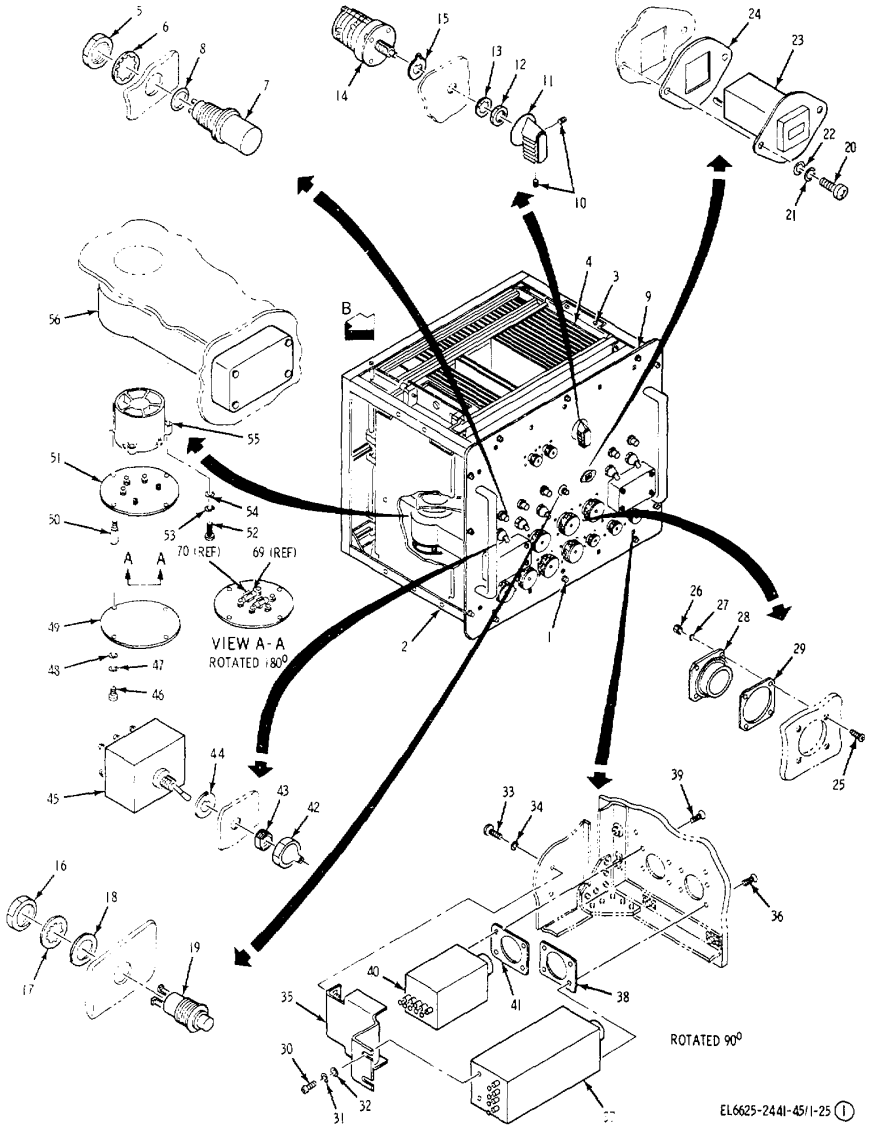


*Figure 3-2 **(2)**. Signal Conditioning Unit TS-2913/ASM-386, exploded view (part 2 of 3)*

57 Screw (6)
58 Flatwasher (6)
59 Nut (6)
60 Flatwasher (6)
61 Cleat (6)
62 Screw (6)
63 Flatwasher (6)
64 Blower (2, 2A1B2 and
2A 1B3)
65 Screw (4)
66 Lockwasher (4)
67 Flatwasher (4)
68 Cover
69 Capacitor (4, 2AlCl through
2A 1C4)
70 Clip (4)
71 Screw (4)
72 Lockwasher (4)
73 Flatwasher (4)
74 Component board 2A1A4
75 Boot (4)
76 Switch (4, 2A1S3 through
2A1S6)
77 Nut (4)
78 Lockwasher (4)
79 Keywasher (4)
80 Test panel
81 Nut (51)
82 Lockwasher (51)
83 Test point connector (51, 2AlJ13 through
2A1J63)
84 Screw (6)
85 Flatwasher (6)
86 Screw (6)
87 Flatwasher (6)
88 Angle bracket (2)
89 Screw (4)
90 Flatwasher (4)
91 Plate
92 Screw (4)
93 Locknut (4)
94 Flatwasher (4)
95 Transformer 2AlTl
96 Screw
97 Locknut
98 Lockwasher
99 Flatwasher
100 Reactor 2AlLl
101 Screw (4)
102 Locknut (4)
103 Flatwasher (4)
104 Terminal board 2A1TB1
105 Marker strip
106 Screw (6)
107 Locknut (6)
108 Flatwasher (6)
109 Bus bar retainer (2)
110 Bus bar (2, 2A1W2, and
2A1W3)
111 Bus bar bracket (2)



Signal (3) Signal Conditioning- Unit TS-2913/ASM-386, exploded view (part 3 of 3)

112	Connector retaining screw (14)
113	Connector (14, 2AtP1 through 2A1P6, and AlPI through I AlP8)
114	Screw (28)
	ll5 Nut i28)
116	Lockwasher ' 28 I
117	Flatwasher (2'8)
118	Card cage connectors (11)
119	Screw (42)
120	Flatwasher (-12)
121	Spacer (42)
122	Cover (7)
123	Standoff (11)
124	Screw (91)
125	Lockwasher (91)
126	Flatwasher (91)
127	Bushing (91)
128	Connector plate assembly (7)
129	Spacer (7) 1A2A4)
130	Spacer (14)
131	Spacer (28)
132	Pin (2)
133	Hinge, pin t2)
134	Nylon shim washers (4 maximum)
135	Card cage 2A1S 3
136	Screw (12)
137	Lockwasher (12)
138	Flatwasher (12)
139	Bushing (12)
140	Ground strap (6)
141	Screw (18)
142	Flatwasher (IS)
14:3	Connecting plate (9)
144	Pin (12)
145	Hinge pin (6)
146	Nvlon shim washers (24 maximum)
147	Card cage (6, 2A] Al, 2AIA2 lAlAl through

(3) Secure card cage(s) (4) to chassis assembly (2) with captive screws (3).

(4) Slide chassis assembly (2) into combination case and tighten 12 stud nuts.

3-7. Removal and Replacement of Switch 2AISl
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cage open.

(2) Tag and unsolder wires from terminals of switch S1.

(3) Loosen two setscrews (10) that secure knob (11) to switch S1.

(4) Remove nut (12) and lockwasher (13); remove switch S1 (14) and keywasher (15) from front panel (9).

b. Replacement

(1) Attach keywasher (15) and switch S1 (14) to front panel (9) with lockwasher (13) and nut (12).

(2) Solder tagged wires to proper terminals of switch S1.

(3) Secure knob (11) to switch S1 with two setscrews (10).

(4) Refer to paragraph 3-6b(3) and (4) to secure card cage to chassis assembly and install chassis assembly in combination case.

3-8. Removal and Replacement of Switch 2AIS2
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cage open.

(2) Tag and unsolder wires from terminals of switch S2.

(3) Remove nut (16), lockwasher (17), and flatwasher (18); remove switch S2 (19) from front panel (9).

b. Replacement

(1) Attach switch S2 (19) to front panel (9) with flatwasher (18), lockwasher (17), and nut (16).

(2) Solder tagged wires to proper terminals of switch S2.

(3) Refer to paragraph 3-6b(3) and (4) to secure card cage to chassis assembly and install chassis assembly in combination case.

3-9. Removal and Replacement of Elapsed-Time Meters 2AIM1 and 1AIA5MI

a. Removal

(1) Remove two screws (20), lockwashers (21), and flatwashers (22); carefully remove elapsed-time meter (23) and emi gasket (24) from front panel.

(2) Tag and unsolder wires from elapsed- time meter terminals.

b. Replacement

(1) Solder tagged wires to proper elapsed- time meter terminals.

(2) Attach emi gasket (24) and elapsed-time meter (23) to front panel using two flatwashers (22), lockwashers (21), and screws (2).

3-10 . Removal and Replacement of Front Panel Connectors 2A1J3 through 2AlJ12
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and remove wires from faulty connector.

(3) Remove four screws (25), nuts (26), and flatwashers (27); remove connector (28) and emi gasket (29) from front panel.

b. Replacement

(1) Attach emi gasket (29) and connector (28) to front panel using four flatwashers (27), nuts (26). and screws (25).

(2) Install tagged wires in connector.

(3) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-11. Removal and Replacement of Filter 2A1J2
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Remove two nuts (30), lockwashers (32), flatwashers (32), screws (33), and flatwashers (34); remove filter support bracket (35).

(3) Tag and unsolder wires from filter J2 terminals.

(4) Remove four screws (36); remove filter J2 (37) and emi gasket (38) from front panel.

b. Replacement

(1) Attach emi gasket (38) and filter J2 (37) to front panel using four screws (36).

(2) Solder tagged wires to filter J2 terminals.

(3) Mount filter support bracket (35) using two flatwashers (34), screws (33, flatwashers (32), lockwashers (31), and nuts (30).

(4) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-12. Removal and Replacement of Filter 2A1J1
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Remove two nuts (30), lockwashers (32), flatwashers (32), screws (33). and flatwashers (34); remove filter support bracket (35).

(3) Tag and unsolder wires from filter J1 terminals.

(4) Remove four screws (39); remove filter J1 (40) and emi gasket (41) from front panel.

b. Replacement

(1) Attach emi gasket (41) and filter J1 (40) to front panel using four screws (39).

(2) Solder tagged wires to filter J1 terminals.

(3) Mount filter support bracket (35) using two flatwashers (34), screws (33), flatwashers (32). lockwashers (31), and nuts (30).

(4) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-13. Removal and Replacement of Circuit Breakers 2A1CB1 through 2A1CB4
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3--6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and unsolder wires from terminals of faulty circuit breaker.

(3) Remove boot (42) and boot adapter (43); remove keywasher (44) and circuit breaker (45) from front panel (9).

b. Replacement

(1) Attach keywasher (44) and circuit breaker (45) to front panel (9) with boot adapter (43) and boot (42).

(2) Solder tagged wires to proper terminals of replacement circuit breaker.

(3) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-14 . Removal and Replacement of Blower 2A1B1
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) to remove chassis assembly from combination case; carefully place chassis assembly upside down on work- bench.

(2) Remove four screws (46), lockwashers (47), and flatwashers (48); remove protection plate (49).

(3) Remove four spacers (50); remove air inlet duct cover (51).

(4) Tag and unsolder wires from terminals of blower Bl.

(5) Remove three screws (52), lockwashers (53), and flatwashers (54); remove blower Bl (55) from air inlet duct (56).

b. Replacement

(1) Attach blower BI (55) to air inlet duct (56) with three flatwashers (54), lockwashers (53), and screws (52).

(2) Solder tagged wires to proper terminals of blower Bl.

(3) Secure air inlet duct cover (51) to air inlet duct (56) with four spacers (50).

(4) Attach protection plate (49) to spacers (50) with four flatwashers (48), lockwashers (47), and screws (46).

(5) Refer to paragraph 3-6b(4) to install chassis assembly in combination case.

3-15 . Removal and Replacement of Blower 2A1B2 and 2A1B3
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag wires attached to terminals of faulty blower; remove three screws (57) and flatwashers (58) and remove wires from faulty blower.

(3) Remove three nuts (59), flatwashers (60), cleats (61), screws (62), and flatwashers (63); remove blower (64).

b. Replacement

(1) Attach blower (64) to chassis assembly (2) with three flatwashers (63), screws (62), cleats (61), flatwashers (60), and nuts (59).

(2) Attach tagged wires to proper terminals of replacement blower with three flatwashers (58) and screws (57).

(3) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-16. Removal and Replacement of Capacitors 2AlC1 through 2A1C4
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) to remove chassis assembly from combination case.

(2) Proceed as follows to remove capacitors C3 and C4:

(a) Refer to paragraph 3-6a(2) to swing card cages open from chassis assembly.

(b) Remove four screws (65), lockwashers (66), and flatwashers (67); remove capacitor cover (68).

(

c) Unsolder leads of faulty capacitor (69) and remove from clip (70).

(3) Proceed as follows to remove capacitors Cl and C2:

(a) Carefully place chassis assembly (2) upside down on workbench.

(b) Perform procedure in paragraph 3-14a(2).

(c) Unsolder leads of faulty capacitor (69) and remove from clip (70).

b. Replacement

(1) Proceed as follows to replace capacitors C1 and C2:

(a) Place capacitor (69) in clip (70) and solder leads to terminals.

(b) Perform procedure in paragraph 3-14b(4).

(c) Place chassis assembly (2) right side up on workbench.

(2) Proceed as follows to replace capacitors C3 and C4:

(a) Place capacitor (69) in clip (70) and solder leads to terminals.

(b) Attach capacitor cover (68) to chassis assembly (2) with four flatwashers (67), lock- washers (66), and screws (65).

(c) Refer to paragraph 3-6b(3) to secure card cages to chassis assembly.

(3) Refer to paragraph 3-6b(4) to install chassis assembly in combination case.

3-17. Removal and Replacement of Component Board 2A1A4
(fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) above to remove chassis assembly from combination case and swing card cages open.

(2) Tag and unsolder wires attached to component board A4.

(3) Remove four screws (71), lockwashers (72), and flatwashers (73); remove component board A4 (74).

b. Replacement

(1) Attach component board A4 (74) to chassis assembly (2) with four flatwashers (73), lockwashers (72), and screws (71).

(2) Solder tagged wires to proper terminals of component board A4.

(3) Refer to paragraph 3-6b(3) and (4) to secure card cages to assembly and install chassis assembly in combination case.

3-18. Removal and Replacement of Switches 2A1S3 through 2A1S6
(fig. 3-2)

The following removal and replacement procedures apply to toggle switches S3 (front panel) and S4 through S6 (test panel).

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and unsolder wires attached to terminals of faulty switch.

(3) Remove boot (75); remove switch (76), nut (77), lockwasher (78), and keywasher (79) from test panel (SO) or front panel (9).

b. Replacement

(1) Attach keywasher (79), lockwasher (78), nut (77) and switch (76) to test panel (80) or front panel (9) with boot (75); tighten nut (77).

(2) Solder tagged wires to proper terminals of replacement switch,

(3) Refer to paragraph 3-66(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-19 . Removal and Replacement of Test Point Connectors 2A1J13 through 2A1J63 (fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cage open.

(2) Unsolder wire(s) from test point connector terminal.

(3) Remove nut (81) and lockwasher (82); remove test point connector (83) from TEST POINT panel.

b. Replacement

(1) Attach test point connector (83) to TEST POINT panel using lockwasher (82) and nut (81).

(2) Solder wire(s) to test point connector terminal.

(3) Refer to paragraph 3-6b(3) and (4) to secure card cage to chassis assembly and install chassis assembly in combination case.

3-20. Removal and Replacement of Transformer 2A1T1 (fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and unsolder wires from transformer T1 terminals.

(3) Remove six screws (84), flatwashers (85), screws (86), and flatwashers (87); remove two angle brackets (88).

(4) Remove four screws (89) and flat- washers (90); carefully lift plate (91) from heat exchanger.

(5) Remove four screws (92), locknuts (93), and flatwashers (94); remove transformer T1 (95) from plate (91).

b. Replacement

(1) Attach transformer T1 (95) to plate (91) using four flatwashers (94), locknuts (93), and screws (92).

(2) Attach plate (91) to heat exchanger using four flatwashers (90) and screws (89).

(3) Install two angle brackets (88) using six flatwashers (87), screws (86), flatwashers (85), and screws (84).

(4) Solder tagged wires to transformer T1 terminals.

(5) Refer to paragraphs 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-21 . Removal and Replacement of Reactor 2AIL1 (fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and unsolder wires from reactor L1 terminals.

(3) Remove six screws (84), flatwashers (85), screws (86), and flatwashers (87): remove two angle brackets (88).

(4) Remove four screws (89) and flat- washers (90); carefully lift plate (91) from heat exchanger.

(5) Remove screw (96), locknut (97), lock- washer (98), and flatwasher (99); remove reactor L1 (100) from plate (91).

b. Replacement

(1) Attach reactor LI (100) to plate (91) using flatwasher (99), lockwasher (98), locknut (97), and screw (96).

(2) Attach plate (91) to heat exchanger using four flatwashers (90) and screws (89).

(3) Install two angle brackets (88) using six flatwashers (87) screws (86), flatwashers (85), and screws (84)

(4) Solder -tagged wires to reactor L1 terminals.

(5) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly : combination case.

3-22 . Removal and Replacement of Terminal Board 2A]TBI (fig. 3-2)

a. *Removal*

(1) Refer to paragraph 3-6a(l) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and remove wires from terminal board TB1. Note position of jumper strips before removing them.

(3) Remove six screws (84), flatwashers (85) screws (86), and flatwashers (87), remove two angle brackets (88)

(4) Remove four screws (89) and flatwashers (90)carefully lift plate (91) from heat exchanger.

(5) Remove four screws (101), locknuts (1.02) and flatwashers (103); remove terminal board TB1 (104)and marker strip (105) from plate (91)

b. Replacement

(1) Attach marker strip (105) and terminal board TB1 (104) to plate (91) using four flatwashers (103), locknuts (102), and screws (101).

(2) Attach plate (91) to heat exchanger using four flatwashers (90) and screws (89).

(3) Install two angle brackets (88) using six flatwashers (87), screws (86), flatwashers (85), and screws (84).

(4) Install jumper strips in positions noted before removal and attach tagged wires to terminal board TB1.

(5) Refer to paragraph 3-6b(3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-23. Removal and Replacement of Bus Bars 2A1W2 and 2AIW3 (fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) and (2) to remove chassis assembly from combination case and swing card cages open.

(2) Tag and remove wires from bus bars W2 and W3.

(3) Remove six screws (84), flatwashers (85), screws (86), flatwashers (87); remove two angle brackets (88).

(4) Remove four screws (89) and flatwashers (90); remove plate (91).

(5) Remove six screws (106), locknuts (107), and flatwashers (108); remove two bus bar retainers (109), bus bars W2 and W3 (110), and two bus bar brackets (111).

b. Replacement

(1) Attach two bus bar brackets (111), bus bars W2 and W3 (110), and two bus bar retainers (109) using six flatwashers (108), locknuts (107), and screws (106).

(2) Attach plate (91) to heat exchanger using four flatwashers (90) and screws (89).

(3) Install two angle brackets (88) using six flatwashers (87), screws (86), flatwashers (85), and screws (84).

(4) Attach tagged wires to bus bars W2 and W3.

(5) Refer to paragraph 3-6b('3) and (4) to secure card cages to chassis assembly and install chassis assembly in combination case.

3-24. Removal and Replacement of Card Cage Connectors (fig. 3-2)

The following removal and replacement procedure applies to connectors J1 and J2 of all card cages in the SCU and LCU. It is assumed in this procedure that access to the card cage has been made.

a. Removal

(1) Remove circuit cards from card cage (TM 11-6626-2441-12).

(2) Loosen two connector retaining screws (112) and carefully disconnect two mating connectors (113).

(3) Tag and remove wires and contacts from damaged connector. (Refer to paragraph 3-47 for proper contact removal tool.)

(4) Remove two screws (114), nuts (115), lockwashers (116), and flatwashers (117); remove connector (1 18).

b. Replacement

(1) Attach connector (118) to card cage using two flatwashers (117), lockwashers (116), nuts (115), and screws (114).

(2) Insert tagged wires and contacts in connector. (Refer to paragraph 3-2ce for proper insertion tool.)

(3) Connect two connectors (113) and tighten two connector retaining screws (112).

(4) Install circuit cards (TM 11-66252441-12).

(5) Install chassis assembly in combination case.

3-25. Removal and Replacement of Connector Plate (fig. 3-2)

The following removal and replacement procedure applies to the connector plate of all SCU and LCU card cages. It is assumed in this procedure that access to the card cage has been made.

a. Removal

(1) Remove all circuit cards from card cage with damaged connector plate (TM 11-6625-2441-12).

(2) Loosen two or four captive screws (3) and swing card cage(s) out.

(3) Remove six screws (119) and flatwashers (120); remove six spacers (121) and cover 1122).

(4) Tag and remove wires from standoffs E1 and W1 (123).

(5) Loosen two connector retaining screws (112) and disconnect two connectors (113).

(6) Remove four screws (114), nuts !115;), lockwashers (116), and flat. washers (117); remove connectors JI and J2 (118). Do not remove wires and contacts from connectors.

(7) Remove 13 screws (124). lockwashers (125), flatwashers (126), and bushings (127); remove connector plate assembly (128), spacer (129), two spacers (130), and four spacers (131).

b. Replacement

(1) Attach four spacers (131), two spacers (13O), spacer (129), and connector plate assembly (128) to card cage frame using 13 bushings (127), flatwashers (126), lockwashers (125), and screws (124).

(2) Install connectors JI and J2 (118) using four flatwashers (117), lockwashers (116), nuts (115), and screws (114).

(3) Connect two connectors (113) and tighten two connector retaining screws (112).

(4) Route tagged wires through grommet in card cage and attach to standoffs W1 and E1 (123).

(5) Attach cover (122) to card cage using six spacers (121), flatwashers (120), and screws (119).

(6) Swing card cage(s) back to normal position; secure to chassis assembly by tightening captive screws (3).

(7) install chassis assembly in combination

3-26. Removal and Replacement of Card Cage 2A1A3 (fig. 3-2)

a. Removal

(1) Refer to paragraph 3-6a(1) to remove chassis assembly from combination case.

(2) Remove circuit cards (TM 11-6625-2441-12).

(3) Loosen two connector retaining screws (112) and carefully disconnect two connectors (113).

(4) Loosen ,two captive screws (3) and swing card cage A3 (135) open.

(5) Remove six screws (119) and flatwashers (121)): remove, sax spacers (121) and cover (122).

(6) Tag and remove Wires from standoffs E1 and W1 (123)

(7) Drive two pins (132) from hinge posts; remove two hinge pins (133),nylon. shim washers (132), and card cage A3 (135).

NOTE

Nylon shim washers are used to reduce the end play of card cage hinge assemblies. Assemblies may have one. two, or no nylon shims installed. When removing a card cage, note the quantity and the position of the shims relative to the card (age: install shims in the same quantity and in the same position when replacing the card cage.

b. Replacement

(1) Remove six screws (119) and flatwashers (120): remove six spacers (121) and (-over (122) from replacement card cage.

(2) Attach card cage A'l3 (135) to chassis assembly with nylon shim washer(s) (134, in the same position and quantity noted in removal), two hinge pins (133), and two pins (132).

(3) Connect two connectors (113) to J1 and J2 (118) and tighten two connector retaining screws (112).

(4) Route tagged wires through grommet in card cage and attach to standoffs WI and E1 (123).

(5) Attach cover (122) to card cage using six spacers (121), flatwashers (120), and screws (119).

(6) Secure card cage to chassis assembly using two captive screws (3).

(7) Install circuit cards (TM 11-6625-2441-12).

(8) Refer to paragraph 3-6b(4) to install chassis assembly in combination case.

3-27. Removal and Replacement of Card Cages 2A1A1, 2A1A2, and 1A1A1 through 1A1A4 (fig. 3-2)

The following removal and replacement procedures are applicable to card cages in both the LCU and SCU. It shall be assumed that the chassis assembly has been removed from the combination case. When removing card cage 1A1A3 or 1A1A4 from the LCU, it is necessary to swing the card cage assembly away from the chassis assembly (TM 11-6625-2441-12).

a. Removal. Steps (2) through (5) below apply to the card cage to be replaced and the adjacent card cage. Steps (7) through (9) apply to the card cage being replaced only.

(1) Remove circuit cards from damaged card cage (TM 11-6625-2441-12).

(2) Looser four captive screws (3) and swing card cages clear.

(3) Remove 12 screws (119) and flatwashers (120); remove 12 spacers (121) and two covers (122).

(4) Remove four screws (136), lockwashers (137), flatwashers (138), and bushings (139); remove two ground straps (140).

(5) Remove six screws (141) and flatwashers (142); remove three connecting plates (143). (One connecting plate is located on the connector end of the card cage, the other two on the opposite end.)

(6) Swing good card cage into normal position and secure using captive screw (3).

(7) Tag and remove wires from standoffs E1 and W1 (123).

(8) Loosen two connector retaining screws (112) and disconnect two connectors (113).

(9) Remove two pins (144) and remove hinge pin (145), nylon shim washer(s) (146), and card cage (147).

NOTE

Nylon shim washers are used to reduce the end play of card cage hinge assemblies. Assemblies may have one, two, or no nylon shims installed. When removing a card cage, note the quantity and the position of the shims relative to the card cage; install shims in the same quantity and in the same position when replacing the card cage.

b. Replacement

(1) Remove six screws (119) and flatwashers (120); remove six spacers (121) and cover (122) from replacement card cage.

(2) Attach card cage (147) to chassis assembly hinge posts with nylon shim washer(s) (146, in the same position and quantity noted in removal), hinge pin (145), and two pins (144).

(3) Connect two connectors (113) to mating card cage connectors and tighten two connector retaining screws (112).

(4) Attach tagged wires to standoffs W1 and El (123). Route wires through grommet in card cage.

(5) Loosen captive screw (3) and swing card cage out and align with replacement card cage. (Refer to a(6) above.)

(6) Connect the two card cages using three connecting plates (143), six flatwashers (142), and screws (141).

(7) Attach two ground straps (140) to card cages using four bushings (139), flatwashers (138), lockwashers (137), and screws (136). To attach the ground strap, it will be necessary to remove the required hardware from the replacement card cage.

(8) Install two covers (122) using 12 spacers (121), flatwashers (120), and screws (119).

(9) Swing card cages into proper position and secure using four captive screws (3).

(10) Install circuit cards in card cage (TM 11-6625-2441-12).

(11) Refer to the appropriate paragraph and install the chassis assembly in the combination case.

3-28. Removal and Replacement of indicators 1A1A5DS] through 1A1A5DS6 and 1AIA5DS9 (fig. 3-3)

a. Removal

(1) Loosen 12 stud nuts (1) that secure chassis assembly (2) to combination case and remove chassis assembly from combination case.

(2) Loosen seven captive screws that secure the two halves of the chassis assembly and swing chassis assembly open.

(3) Tag and unsolder wires attached to terminals of faulty indicator.

(4) Remove two screws (3) that secure legend plateholder (4), legend plate (5), and gasket (6) to front panel lAIA5 (7).

(5) Remove two screws(8), washers (9), and mounting bushings E1 that secure indicator base and spacer (11) to back of front panel.

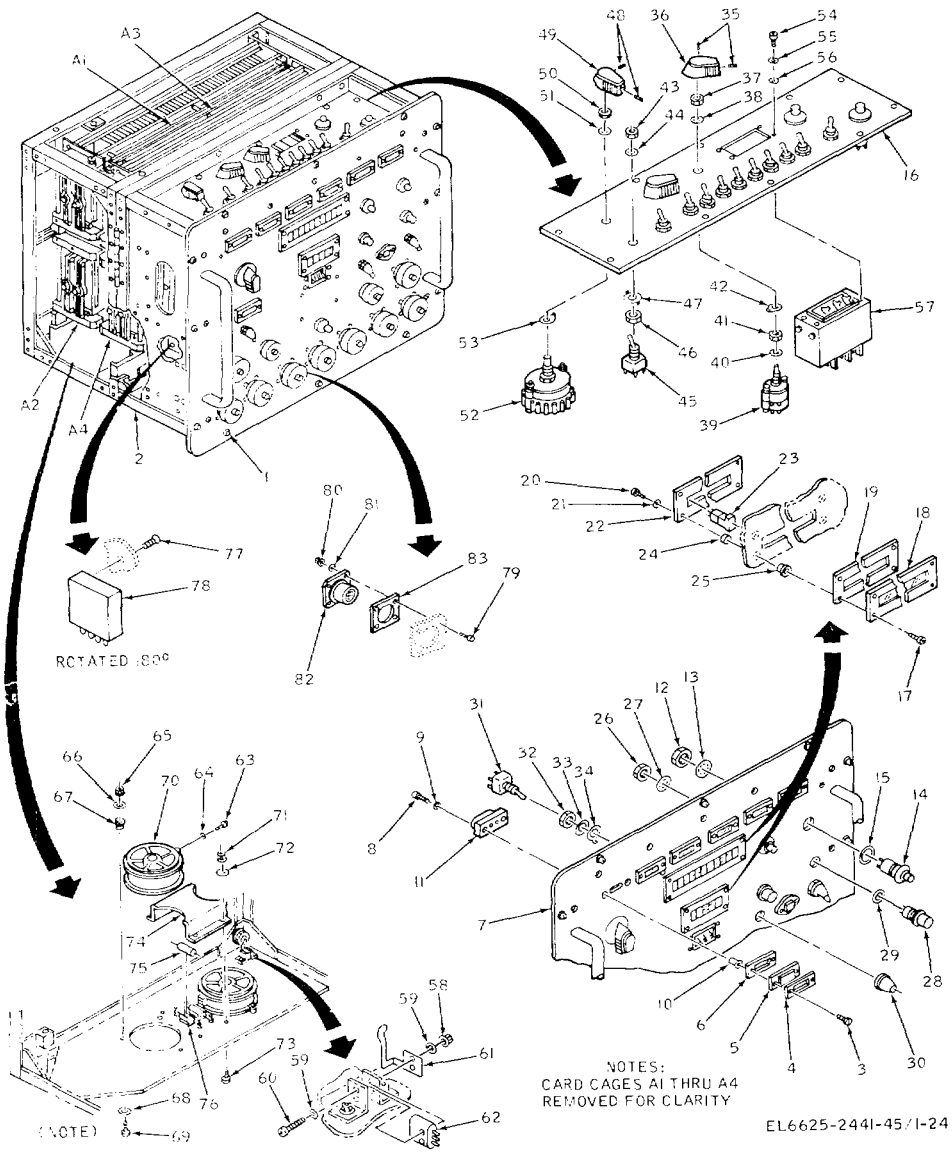


Figure 3-3. Logic Control Unit TS-2912/ASM-386 exploded view

1 Stud nut (12)
2 Chassis assembly
3 Screw (14)
4 Legend plateholder (7)
5 Legend plate (7)
6 Gasket (7)
7 Front panel 1AIA5
8 Screw (14)
9 Washer (14)
10 Mounting bushing (14)
11 Indicator base and spacer (7)
12 Nut (5)
13 Lockwasher (5)
14 Switch (5; 1AIA5S2, 1ATA5S3, lAIA6S5, 1A1A6S6, lAIA5S8)
15 Seal (5)
16 Test panel 1AIA6
17 Screw (8)
18 Bezel and neutral density filter assembly (2)
19 Gasket (2)
20 Screw (8)
21 Washer (8)
22 Mounting strip (2)
23 Lamp assembly (15)
24 Spacer (8)
25 Mounting collar (8)
26 Nut (2)
27 Lockwasher (2)
28 Indicator (2, lAlA5DSlU and 1A1A5DS11)
29 0-ring (2)
30 Boot (3)
31 Switch (3; 1AIA5S4, 1AIA5S6, lAIA5S7)
32 Nut (3)
33 Lockwasher (3)

34 Keywasher (3)
35 Setscrew (6)
36 Knob (3)
37 Nut (3)
38 Lockwasher (3)
39 Switch (3; IAiA5S1, lAlA6S2, IA1A6S3)
40 0-ring (3)
41 Nut (3)
42 Keywasher (3)
43 Nut (11)
441 Loc.'-washer (11)
45 Switch (11, lAlA6S7 through 1AIA6SI7)
16 Nut (11)
47 Keywasher (i1)
48 Setscrew (2)
49 Knob
50 Nut
81 Lockwasher
52 Switch I AlA6S1
53 Keywasher
54 Screw (8)
55 Lockwasher (8)
56 Washer (8)
57 Thumbwheel switch (2, lAlA6S4 and 1AIA5S5)
58 Nut (2)
59 Washer (4)
60 Screw (2)
61 Actuator
62 Panel lockout switch lAlS1
63 Screw (6)
64 Washer (6)
65 Nut (6)
66 Washer (6)
67 Cleat (6)
68 Washer (6)
69 Screw (6)
70 Blower (2, 1A1B1 and 1A1B2)
71 Nut (4)
72 Washer (4)
73 Screw (4)
74 Capacitor cover
75 Capacitor (2, 1A1C1 and 1A1C2)
76 Clip (2)
77 Screw (2)
78 Oscillator 1A1Y1
79 Screw (44)
80 Nut (44)
81 Flatwasher (44)
82 Connector(11, 1A1J1 through 1A1J11)
83 Emi gasket (11)

b. Replacement

(1) Attach indicator base and spacer (11 to back of front panel 1A1A5 (7) using two mounting bushings (10), washers (9), and screw (8).

(2) Solder tagged wires to proper terminals of replacement indicator.

(3) Attach gasket (6), legend plate (5) and legend plateholder (4) to front panel 1A1A5 (7) with two screws (3).

(4) Close two halves of chassis assembly and tighten seven captive screws.

(5) Slide chassis assembly (2) into combination case and tighten 12 stud nuts (1).

3-29. Removal and Replacement of Switches 1A1A5S2, 1A1A5S3, 1A1A.5S8, 1A1A6S5' and 1A1A6S6 (fig. 3-3)

The following removal and replacement procedures apply to front panel switches S2, S3' and S8 and test panel switches S5 and S6.

a. Removal

(1) Refer to paragraph 3-2½'i(1) and (2 to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires from faulty switch terminals.

(3) Remove nut (12) and lockwasher (13) that secure switch (14) and seal (15) to front panel 1A1A5 (7) or test panel 1A1A6 (16); remove switch and seal.

b. Replacement

(1) Place seal (15) and switch (14) in front panel 1A1A5 (7) or test panel 1A1A6 (16) and secure with lockwasher (13) and nut (12).

(2) Solder tagged wires to proper terminals of replacement switch.

(3) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-30. Removal and Replacement of Digital Display Indicators 1A1A5DS7 and 1A1A5DS8 (fig. 3-3)

a. Removal

(1) Refer to 3-28a(1) and (2) to re-move chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires from faulty digital display indicator lamp assembly.

(3) Remove four screws (17); remove bezel and neutral density filter assembly (18) and gasket (19) from front panel lAlA5 (7).

(4) Remove four screws (20) and washers (22-1); remove mounting strip (22) and lamp assembly (23) and four spacer (24) and mounting collars, from front panel 1A1A5 (7).

b Replacement

(1) Secure four mounting collars (25) and spacers (24) and lamp assembly (23) and mounting strip (22) to rear of front panel 1A1A5 (7) with four washers (21) and screws 20).

(2) Secure gasket (19) and bezel and neutral density filter assembly (18) to front panel 1A1A5 (7) with four screws (17).

(3) Solder tagged wires to proper terminals o-f replacement digital display indicator.

(4) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-31. Removal and Replacement of Indicators 1A1A5DS10 and 1A1A5DS11 (fig. 3-3)

a. Removal

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to terminals of faulty indicator.

(3) Remove nut (26) and lockwasher (27); remove indicator (28) and 0-rirg (29) from front panel 1A1A5 (7).

b. Replacement

(1) Replace 0-ring (29) and indicator (28) on front panel 1A1A5 (7) using lockwasher (27) and nut (26).

(2) Solder tagged wires to proper terminals of replacement indicator.

(3) Refer to3--28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-32. Removal and Replacement of in-witches 1A1A5S4, 1A1A556, and lAIASS7 (fig. 3-3)

a. Removal

(1) Refer to 328a (1) and (2), to remove chassis assembly, from combination case and to open chassis assembly.

(2) Tag and unsolder wires from terminals of faulty switch.

(3) Remove boot (30), remove switch (31), nut (32). lockwasher (33), and keywasher (34) from front panel 1A1A15 (7)

b. Replacement

(1) Attach keywasher (31,), ¶ (33), nut (32) and switch (31) to front panel 1A1A5 (7) using boot (30); tighten nut (32).

(2) Solder tagged wires to proper terminals of replacement switch.

(3) Refer to 3--28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-33. Removal and Replacement of Switches 1A1A5S1, 1A1A6S2, and 1A1A6S3 (fig. 3-3)

The following removal and for placement procedure applies to front panel switch S1 and test panel switches S2 and S3.

a. Removal

(1) Refer to 3—28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to terminals of faulty switch.

(3) Loosen two setscrews {35) that secure knob (36) to switch.

(4) Remove nut (37) and lockwasher (38); remove switch (39), 0-ring (40), nut (41), and keywasher (42) from front panel lAlA5 (7) or test panel lAlA6 (16).

b. Replacement

(1) Attach keywasher (42), nut (41), 0ring (40), and switch (39) to front panel lAlA5 (7) or test panel 1A1A6 (16) with lockwasher (38) and nut (37).

(2) Solder tagged wires to proper terminals of replacement switch.

(3) Secure knob (36) to switch with two setscrews (35).

(4) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-34. Removal and Replacement of Switches 1AIA6S7 through 1A'IA6S17 (fig. 3-3)

a. Removal

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to terminals of faulty switch.

(3) Remove nut (43) and lockwasher (44); remove switch (45), nut (46), and keywasher (47) from test panel 1A1A6 (16).

b. Replacement

(1) Attach keywasher (47), nut (46), and switch (4.5; to, test panel t.'iA6 (16) with lockwasher (44) and nut (43).

(2) Solder tagged wires to proper terminals of replacement switch.

(3) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-35. Removal and Replacement of Switch 1A1A6S1 (fig. 3 -3)

a. Removal

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to terminals of switch S1.

(3) Loosen two setscrews (48) that secure knob (49) to switch S1.

(4) Remove nut (50) and lockwasher (51); remove switch SI (52) and keywasher (53) from test panel lAlA6 (16).

b. Replacement

(1) Attach keywasher (53) and switch SI (52) to test panel lAlA6 (16) with lockwasher (51) and nut (50).

(2) Solder tagged wires to proper terminals of switch S1.

(3) Secure knob (49) to switch SI with two setscrews (48).

(4) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-36. Removal and Replacement of Thumbwheel Switches 1A1A6S4 and 1A1A5S5 (fig. 3-3)

The following removal and replacement procedure applies to test panel thumbwheel switch S4 and front panel thumbwheel switch S5.

a. Removal

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to terminals of faulty thumbwheel switch.

(3) Remove four screws (54), lockwashers (55), and washers (56); remove thumbwheel switch (57).

b. Replacement

(1) Attach thumbwheel switch (57) to panel with four washers (56), lockwashers (55) and screws (54).

(2) Solder tagged wires to proper terminals of replacement thumbwheel switch.

(3) Refer to 3--28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-37. Removal and Replacement of Panel Lockout Switch 1A1S1 (fig. 3-3)

a. Removal (1) Refer to 3-28a(1) to remove chassis assembly from combination case.

(2) Loosen two captive screws that secure card cage 1A1A.,2 to rear half of chassis assembly and swing card cage 1AlA2 clear of blower interlock switch.

(3) Tag and unsolder wires attached to blower interlock switch SI.

(4) Remove two nuts (58), four washers (59), and two screws (60); remove actuator (61) and blower interlock switch S (62).

b. Replacement

(1) Attach blower interlock switch SI (62) and actuator (61) to rear half of chassis assembly (2) with two screws (60), four washers (59), and two nuts (58).

(2) Solder tagged wires to proper terminals of blower interlock switch S1.

(3) Swing card cage 1A1A2 into position on rear half of chassis assembly (2) and tighten two captive screws.

(4) Refer to 3-28b(5) to install chassis assembly in combination case.

3-38. Removal and Replacement of Blower 1A1B1 and 1A1B2 (fig. 3-3)

a. Removal (1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Loosen eight captive screws that secure card cages 1A1A1 through 1AIA4 to rear half of chassis assembly (2) and swing the four card cages clear of the rear half of the chassis assembly.

(3) Tag wires attached to faulty blower terminals; remove three screws (63) and washers (64) and wires.

(4) Remove three nuts (65), washers (66), cleats (67), washers (68), and screws (69); remove blower (70) from chassis assembly (2).

b. Replacement

(1) Secure blower (70) to chassis assembly (2) with three screws (69), washers (68), cleats (67), washers (66), and nuts (65).

(2) Attach wires to proper terminals of replacement blower and secure with three washer (64) and screws (63).

(3) Swing card cages 1A1A1 through lAlA4 into position on rear half of chassis assembly (2) and tighten eight captive screws.

(4) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-39. and Replacement of Capacitors 1A1Cl and 1A1C2 (fig. 3-3)

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Loosen eight captive screws that secure card cages 1A1A1 through 1A1A4 to

rear half of chassis assembly (2) and swing card cages clear of rear half of chassis assembly.

(3) Remove four nuts (71), washers (72), and screws (73); remove capacitor cover (74) from chassis assembly (2).

(4) Unsolder leads of capacitor (75) and remove from clip (76).

b. Replacement

(1) Place capacitor (75) in clip (76) and solder capacitor leads to standoff terminals.

(2) Attach capacitor cover (74) to chassis assembly (2) with four screws (73), washers (72), and nuts (71).

(3) Swing card cages lAlAl through lAlA4 into position on rear half of chassis assembly and tighten eight captive screws.

(4) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-40. Removal and Replacement of Oscillator 1A1Y1 (fig. 33)

a. Removal

(1) Refer to 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and unsolder wires attached to leads of oscillator Y1.

(3) Remove two screws (77); remove oscillator Y1 (78) from chassis assembly (2).

b. Replacement

(1) Attach oscillator Y1 (78) to chassis assembly (2) with two screws (77).

(2) Solder tagged wires to proper terminals of oscillator Y1.

(3) Refer to 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-41. Removal and Replacement of Connectors 1A1J1 through 1A1J1 (fig. 3-3)

a. Removal

(1) Refer to paragraph 3-28a(1) and (2) to remove chassis assembly from combination case and to open chassis assembly.

(2) Tag and remove wires and contacts of connector.

(3) Remove four screws (79), nuts (80), and flatwashers (81); remove connector (82) and emi gasket (83).

b. Replacement

(1) Attach emi gasket (83) and connector (82) to front panel using four flatwashers (81), nuts (80), and screws (79).

(2) Insert tagged wires into connector.

(3) Refer to paragraph 3-28b(4) and (5) to secure chassis assembly halves and install chassis assembly in combination case.

3-42. Removal and Replacement of Connectors 3A4-2J1 through 3A4-2J8, 3A4-2Jl5, 3A4-2J16, and 3A4-3J1 (fig. 3-4)

a. Removal

(1) Remove 14 screws (1) and flatwashers (2); remove cover (3) from chassis (4).

(2) Tag and remove wires from connector.

(3) Remove four screws (5), locknuts (6), and flatwashers (7) remove connector (8) and emi gasket (9)

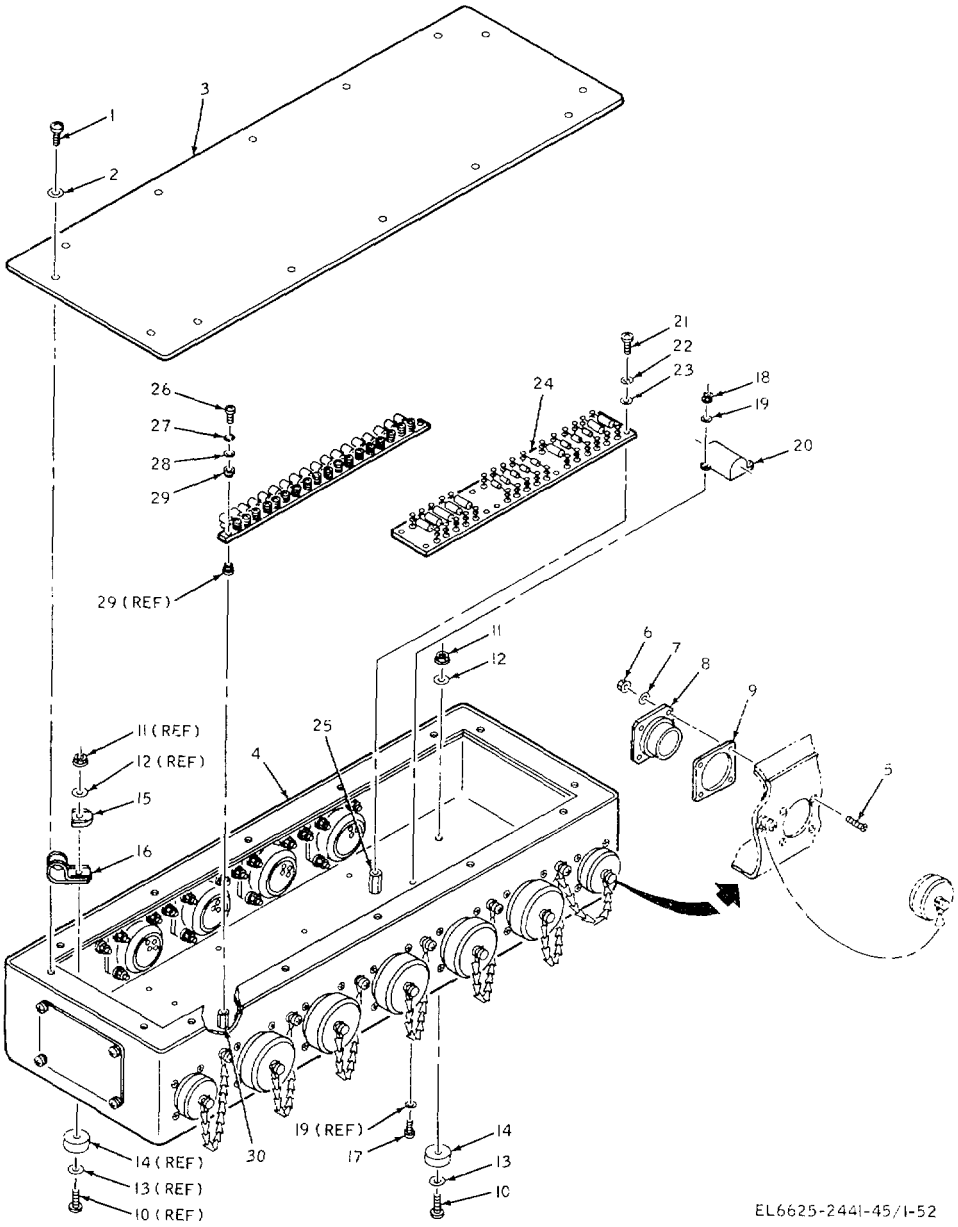


Figure 3-4. Adapter, Self-Test MX-8586/ASll-386 exploded view.

1 Screw (14)
2 Flatwasher (14)
'3 Cover
4 Chassis
5 Screw (44)
6 Locknut (44)
7 Flatwasher (44)
8 Connector (11; 3A4-2J1 through 3A4-2J8, 3A4-2J15, 3A4-2J16, 3A4-3J1)
9 Emi gasket (11)
10 Screw (4)
11 Nut (4)
12 Flatwasher (4)
13 Flatwasher t4)
l1t Bumper (4)
15 D-washer (3)
16 Cable clamp (3)
17 Screw (2)
18 Locknut (2)
19 Flatwasher (4)
20 Resistor 3A4R1
21 Screw (4)
22 Lockwasher (4)
23 Flatwasher (4)
24 Component board SA4Al
25 Standoff (4)
26 Screw, (2)
27 Lockwasher (2)
28 Flatwasher (2)
29 Shoulder washer (4)
30 Bus bar 3A4IWi
31 Spacer (2)

b. Replacement

(1) Attach emi gasket (9) and connector (8) to chassis (4) using four flatwashers (7), locknuts (6). and screws (5).

(2) Attach tagged wires to connector.

(3) Attach cover (3) to chassis (4) using 14 flatwashers (2; and screws (1).

3-43. Removal and Replacement of Bumpers and Cable Clamps (fig 3-4)

Hardware used to attach the four bumpers to the self-test adapter also secure the three cable clamps.

a. Removal

(1) Remove 14 screws (1) and flatwashers (2); remove cover (3) from chassis (4).

(2) Remove four screws (10), nuts (11), flatwashers (12), and flatwashers (13); remove four bumpers (14), three D-washers (15), and three cable clamps (16) from chassis (4).

b. Replacement

(1) Attach three cable clamps (16), three D-washers (1). and four bumpers (14) to chassis (4) using four flatwashers (13), flatwashers (12), nuts (11) and screws (10).

(2) Attach -over (3) to chassis (4) using 14 flatwashers (2) and screws (1).

3-44. Removal and Replacement of Resistor 3A4R1 (fig. 3-4)

a. Removal

(1) Remove 14 screws (1) and flatwashers (2); remove cover (3) from chassis (4).

(2) Unsolder wires from resistor R1 terminals.

(3) Remove two screws (17), two locknuts (18), and four flatwashers (19); remove resistor R1 (20) from chassis (4).

b. Replacement

(1) Attach resistor R1 (20) to chassis (4) using four flatwashers (19), two locknuts (18), and two screws (17).

(2) Solder wires to resistor RI terminals.

(3) Attach cover (3) to chassis (4) using 14 flatwashers (2) and screws (1) 3-45. Removal and Replacement of Component Board 3A4A1 (fig. 3-4)

3-45. a. Removal

(1) Remove 14 screws (1) and washers (2); remove cover (3) from chassis (4).

(2) Tag and unsolder wires from component board A1 terminals.

(3) Remove four screws (21), lockwashers (22), and flatwashers (23); remove component board Al (24) from four standoffs t25).

b. Replacement

(1) Attach component board Al (24) to four standoffs (25) using four flatwashers 123), lockwashers (22), and screws (21).

(2) Solder tagged wires to component board Al terminals.

(3) Attach cover (3) to chassis (4) using 14 flatwashers (2) and screws (1).

3-46. Removal and Replacement of Bus Bar 3A4W1 (fig. 3-4)

a. Removal

(1) Remove 14 screws (1) and flatwashers (2); remove cover (3) from chassis (4).

(2) ;and remove wires from bus bar W1

(3) Remove two screws (26), two lockwashers(27), two flatwashers (28), and four shoulder washers (29); remove bus bar W1 (30) from two standoffs (31).

b. Replacement

(1) Attach bus bar W1 (30) to two standoffs (31) using four shoulder washers (29). two flatwashers (28), two lockwashers (27), and two screws (26).

(2) Attach tagged wires to bus bar W1

(3) Attach cover (3) to chassis (4) using 14 flatwashers (2) and screws (1).

3-47. Connector Repair and Replacement (fig. 3-5, 3-6, and 5-9)

The procedures in this paragraph are for test set connectors that are not military standard connectors. These procedures may also b)e used for connector repair. The following chart lists the recommended contact removal and insertion tool and contact locator head for each connector. The contact locator heads listed are used with the MH750 crimping tool. Equivalent tools may be substituted for the tools listed.

CAUTION

The proper tool is determined by the contact size. Do not use the wrong tool.

NOTE

Removal and replacement procedures are the same for both connector pins and sockets.

connector	Contact removal tool (manufacturer	Contact inspection tool (manufacturer)	contact locator head (Daniels)
1A1A1A31J1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J2	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J2	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P9
1A1A1A31J2	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A1A31J2	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A5P1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1A6P1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1J4	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P6
1A1J5	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P6
1A1J112	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1J113	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P1	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P2	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P3	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P4	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P5	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6
1A1P6	TWO22RT000 (Hughes)	TWO22IT000 (Hughes)	P6

Connector	Contact removal tool (manufacturer)	Contact insertion tool (manufacturer)	Contact locator head (Daniels)
1A1P7	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
1A1P8	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A1A31J1	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A1A31J2	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A2A31J1	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A2A31J2	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A3A31J1	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1A3A31J2	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1J3	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P14
2A1J4	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P14
2A1P1	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1P2	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1P3	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1P4	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1P5	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
2A1P6	TW022RT000 (Hughes)	TW022IT000 (Hughes)	P6
3W9P1	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P15
3W9P2	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P15
3W10P1	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P15
3W10P2	11-8794-24 (Bendix)	11-8795-24 (Bendix)	P15

a. The following procedure is applicable to special purpose cable assembly nonmilitary standard connectors. Figure 3-5 illustrates a typical configuration of this type connector. Figure 3-6 illustrates the configuration of banana tip plug 2W6P2. Use standard maintenance practices when replacing connector 2W6P2.

(1) Removal of bayonet coupling connectors

(a) Remove two cable clamp screws and unscrew cable clamp.

(b) Unscrew connector backshell and slide clear of connector shell.

(c) Tag connector contacts; using proper contact removal tool, carefully remove contacts (pins or sockets) by pushing out of connector insert from contact side of connector.

(2) Replacement of bayonet coupling connector

(a) Using proper contact insertion tool, carefully push contact into connector until contact is felt to snap into place. Use nylon plugs provided with connectors to fill all unused connector contact holes.

(b) Screw backshell on connector shell. Use caution when tightening backshell to prevent strain on contacts and wires.

(c) Screw cable clamp on backshell and secure with two cable clamp screws.

b. The following procedures are applicable to LCU and SCU harness connectors and their mating connectors. The tools listed in chart above are to be used for both pins and sockets.

(1) Tag each wire; using proper contact removal tool, carefully but firmly push contacts through connector from connector face.

(2) When replacing card cage connectors, refer to paragraph 3-24 for removal and replacement procedures
.

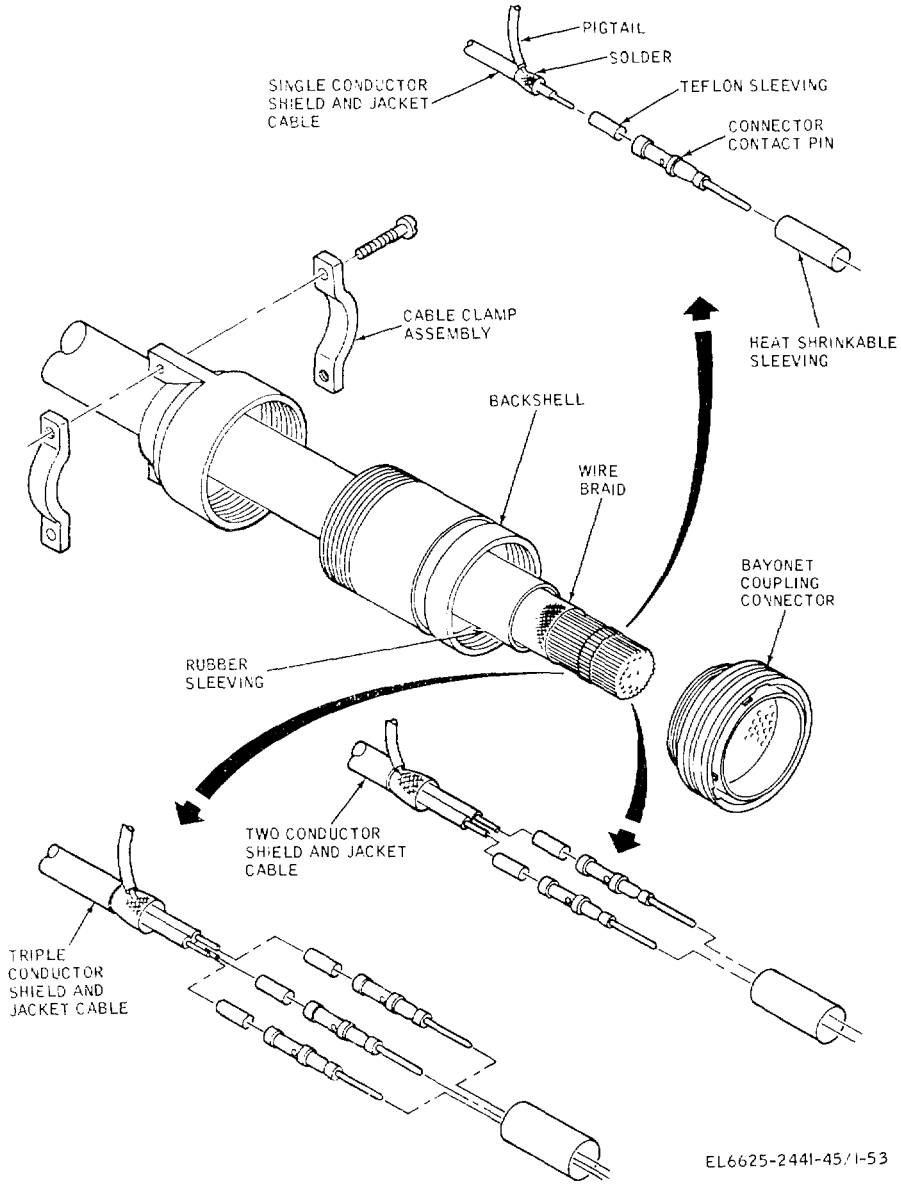


Figure 3-5. Special propose electrical cable assembly, typical shielded cable configuration and connector removal diagram.

(3) Grip tagged contact and wire with proper contact insertion tool and push firmly but carefully until contact is felt to snap into place.

c. The following procedures are applicable to connectors utilizing Termi-Point connections.

(1) Loading Termi--Point service tool (fig.3-7)

(a) Remove spring clip from reel holder spindle.

(b) Place reel of clips on spindle with label side out and replace reel holder spindle spring clip.

(c) Pivot clip train protector down and feed clip train onto clip track.

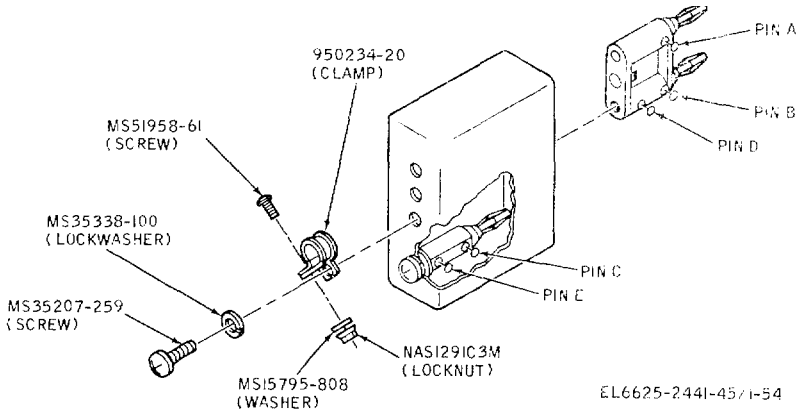


Figure 3-6. Connector 2W6P2, configuration diagram

(d) Using A-end of multipurpose tool, slide feed clip train along clip guide track until clip train stops at feed pawl.

(e) Using B-end of multipurpose tool, depress feed pawl and advance clip train until feed pawl engages the space between the first and second clips.

(f) Pivot clip train protector up and snap into place.

(2) Removing clips and wires (fig. 3-8)

(a) Hold extractor-locator tool perpendicular to connector and hook lip of extractor end of tool as shown. If replacing pin, remove all clips and wires. If repairing wiring harness, remove the clip and wire to be replaced.

(b) Twist tool clockwise to remove clip and wire. If replacing one or two clips, use locator end of tool to reposition remaining clips on connector pin.

(3) Preparation for use (fig. 3-9)

(a) Set clip position control to proper position.

(b) Use K. Miller model 100 wire stripper to cut wire to ensure wire end is not flattened. Do not strip wire.

(c) Insert unstripped wire into hole between resizer and mandrel, and push wire until it bottoms.

(d) Squeeze tool handle and release to ready clip and wire e for application to connector pin.

(4) Application (fig. 3-10)

CAUTION

If excessive resistance is encountered during application, do not exert excessive pressure; pin damage will occur.' Remove tool and begin application procedure again.

(a) Position Termi-Point tool so connector pin fits into exposed clip.

(b) Align tool vertically and horizontally and rest alignment foot on surrounding pins.

(c) Apply light pressure on tool until clip reaches preset position on post. Insure that pressure is straight toward connector pin.

(d) Remove tool, release handle and reset tool by pushing clip train protector fully forward.

(e) Depress insulation ejector to remove insulation from tool.

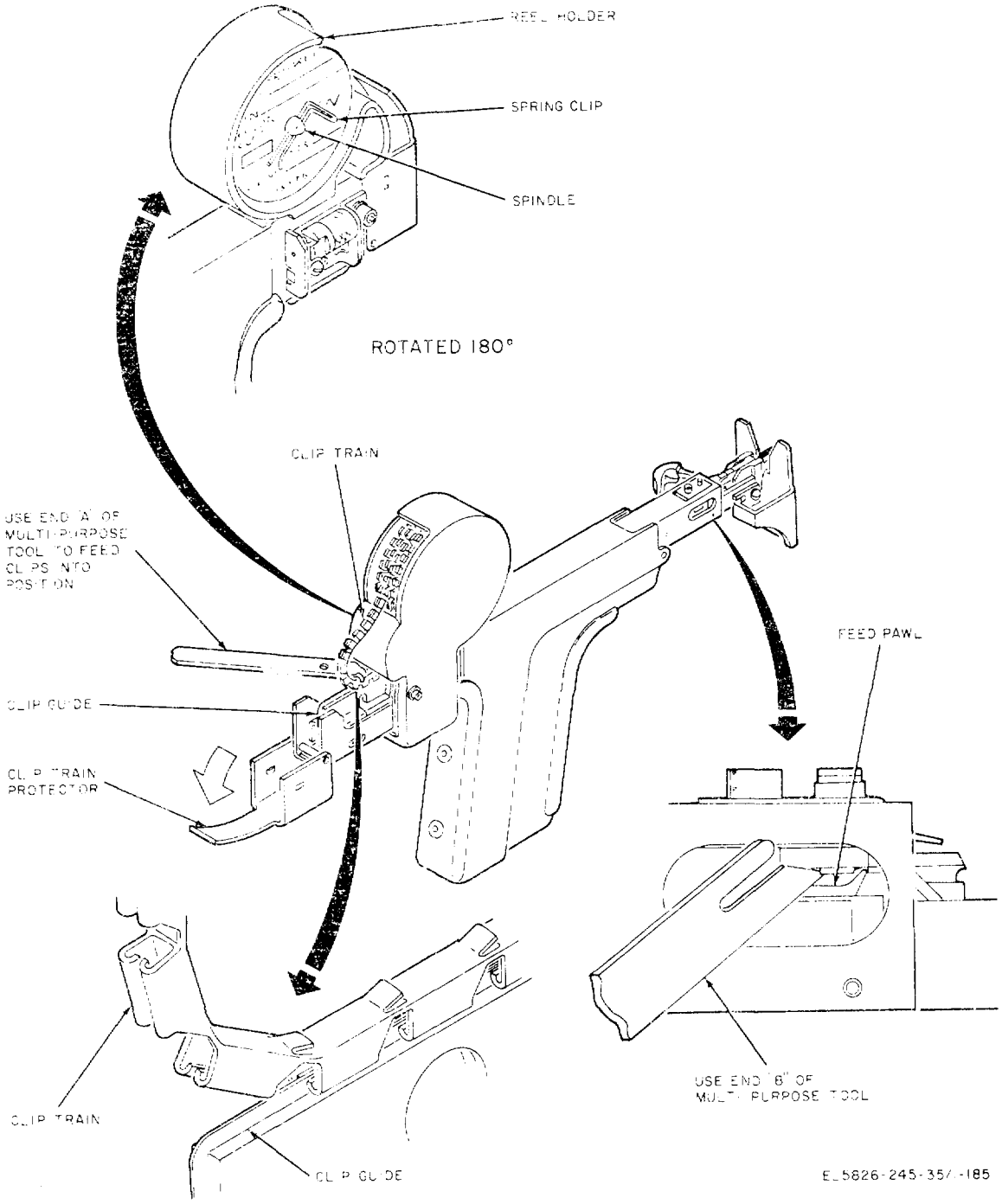


Figure 3-7. Termi-Point service tool loading.

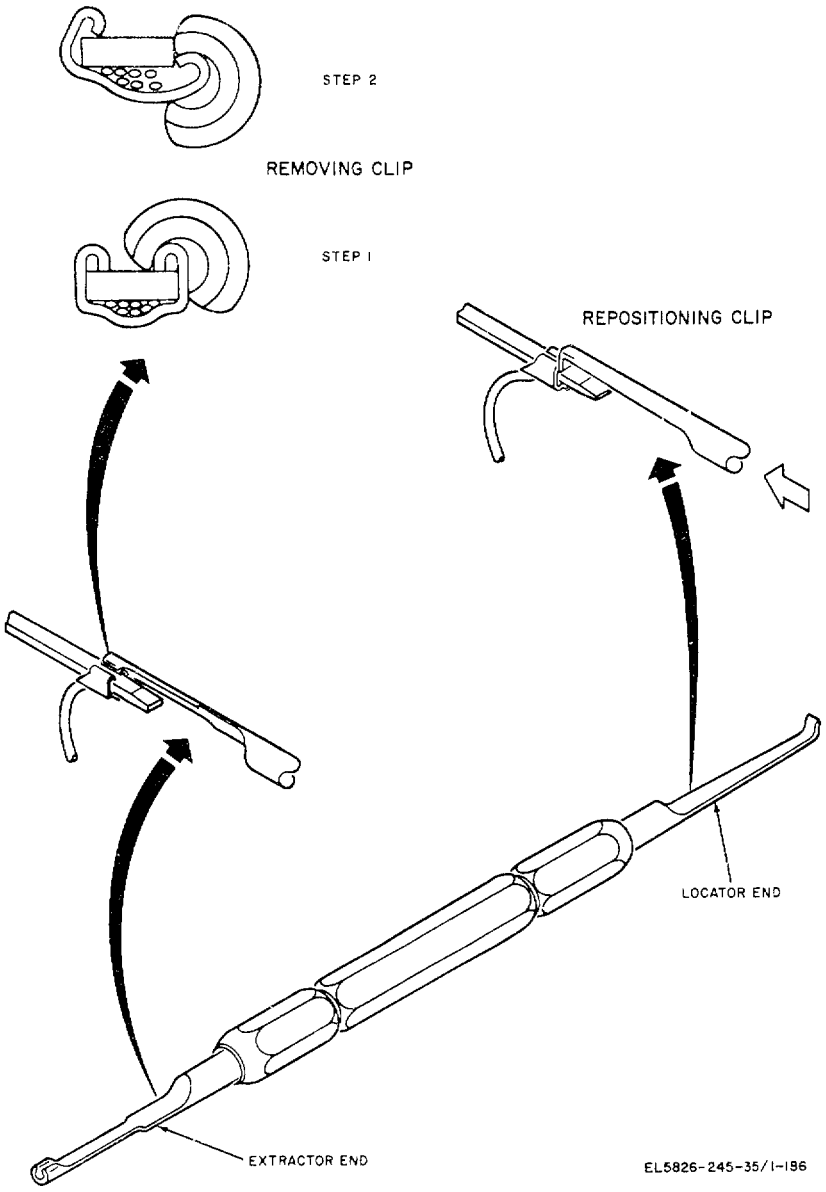


Figure 3-8. Extractor-locator tool.

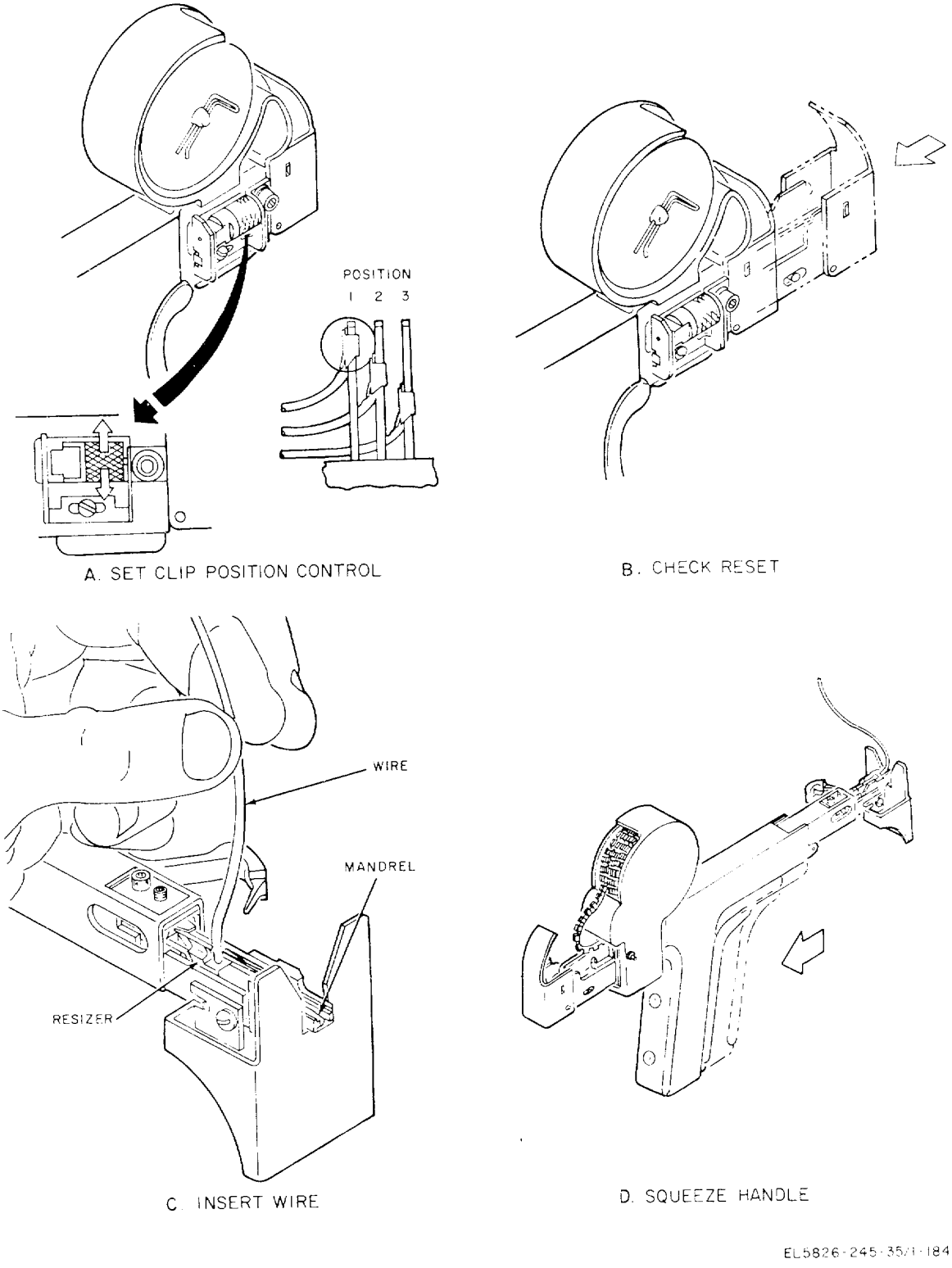


Figure 3-9. Preparing Termi-Point service tool for use.

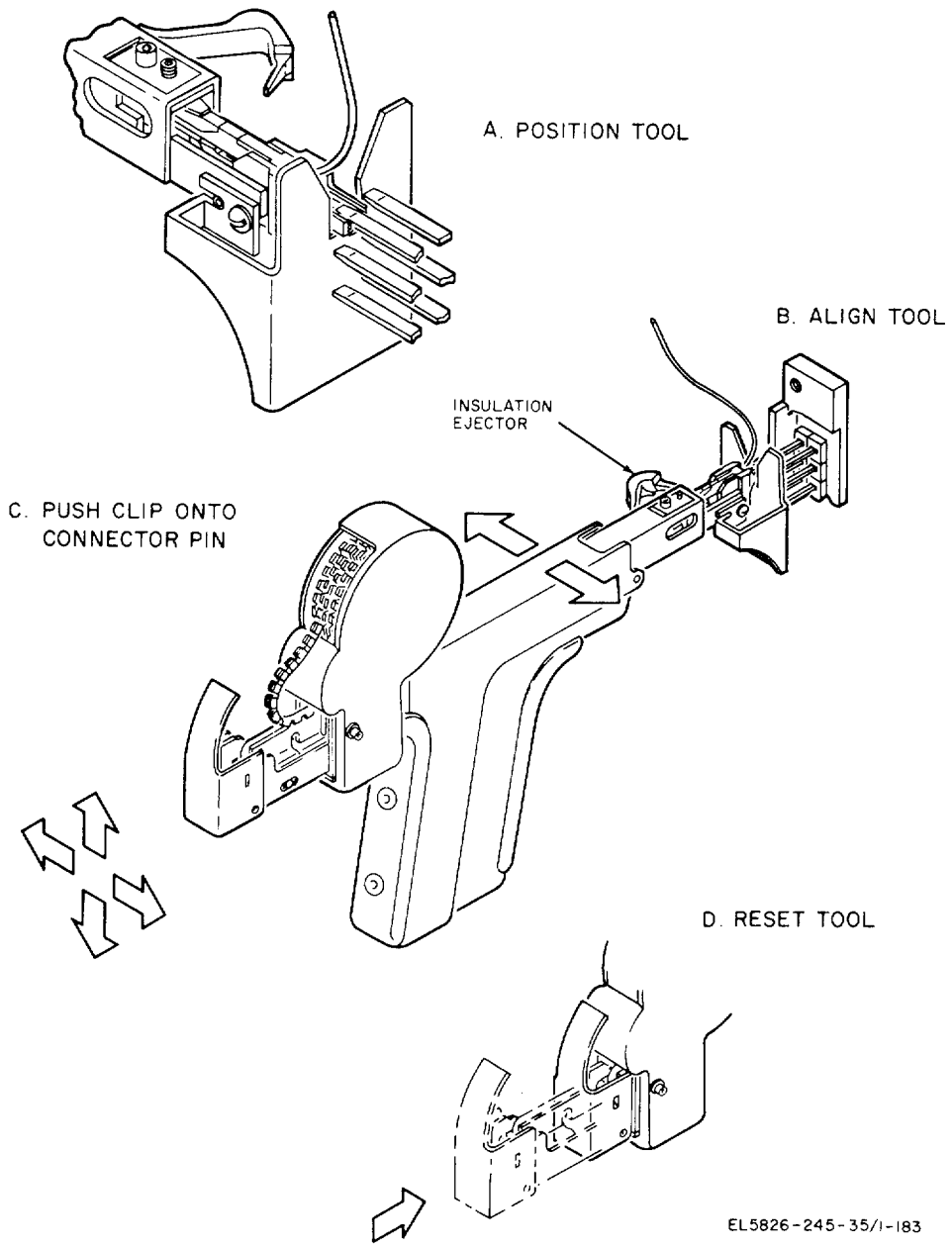


Figure 3-10. Applying clop to connector pin.

CHAPTER 4

DEPOT MAINTENANCE

Section I. GENERAL

4-1. Scope of Depot Maintenance

Depot maintenance consists of testing, adjusting, and troubleshooting power supply 2AlPS1, rebuilding special purpose electrical cable assemblies, and complete overhaul of the test set. Procedures in this chapter also provide instructions for removal and replacement of discrete components and modules of power supply 2AlPS1. The procedures in this chapter combined with those in chapter 3 of this manual provide instructions for rebuilding the test set.

4-2. Tools, Test Equipment, and Materials Required

Tools, test equipment, and materials required, in addition to those listed in TM 11-6625-2441-12 and chapter 3 of this manual, are listed below.

a. Tools. The only additional tool required for depot maintenance is a precision oven, FSN 6640-531-4358, which provides controlled heat for curing epoxy adhesive.

b. Test Equipment. The following chart lists the test equipment required for depot maintenance.

Item	*Part no. and manufacturer*	*Use*
Test fixture, NCCITS power supply	TE 209316 (Litton)	Provides connections for excitation, variable and fixed loads, and test points for testing and adjusting power supply 2AlPS1
Power supply, dual dc	TW 5005 (Power Design)	Provides fixed +28 V excitation and variable test voltages for testing and adjusting power supply 2AIPS1

c. Materials. The following chart lists the materials required for depot maintenance.

Material	*FSN, federal specification or military specification*	*Use*
Adhesive, epoxy, resin, metal-to-metal structural bonding	MIL-A-8623, Type I	Bonds metal to metal

Material	*FSN, federal specification or military specification*	*Use*
Insulating and sealing compound, electrical	MIL-I-8660	Provides additional heat conduction for power diodes and transistors
Capacitor, electrolytic, tantalum, solid (56 µF, 15 V)	MIL-C-39003	Provides filtering for filtered +4.7 V during power supply test

Section II. TROUBLESHOOTING

4-3. General

Troubleshooting at depot maintenance consists of performing a close visual inspection of the equipment received from lower levels of maintenance and performing the procedures contained in this section. It shall be assumed that the items of equipment received at depot maintenance contain faulty components or modules. When performing the procedures in this section, care should be taken to prevent further damage to the equipment.

4-4. Power Supply 2AIPS1 Fault Isolation

Isolation to faulty discrete components or modules in the power supply is performed in two basic operations: a visual inspection and a functional test. Before performing the functional test, perform a careful visual inspection to locate any broken or burned components or wires. Replace faulty components or modules; removal and replacement procedures are located in paragraphs 4-9 through 4-37. If faulty wires, components, or modules are not found during the visual inspection, perform the procedures in paragraph 4-5.

WARNING

The power supply contains voltages which may cause DEATH or SERIOUS INJURY. Be careful when taking readings or making adjustments in the power supply.

CAUTION

Some of the power supply adjustments are very close to exposed terminals and pins. Use extreme care when making adjustments to prevent damage to the power supply.

4-5. Power Supply 2AIPS1 Test Procedure

a. Preliminary Test Procedures

(1) Insure that all primary power to the NCCITS power supply test fixture (test fixture) is off.

(2) Set test fixture switches and controls in as follows:

Switch or control	*Position or*
115 VAC switch	OFF
AUX AC switch	OFF
AC POWER switch	OFF
AUX 28V switch	OFF
+5V LOAD switch	NOM

Switch or control	Position or setting
-15V LOAD switch	NOM
-25V LOAD switch	NOM
AUX 4.7V LOAD switch	RATED
+28V LOAD switch	RATED
FILTERED 4.7V LOAD switch	NOM
RI control (multimeter connected between AUX 4.7 VDC test jack and EXT 28V RTN input jack)	Adjust R I for 9.4 (± 0.5) ohms
R17 (multimeter connected between FILTERED 4.7 VDC test jack and EXT 28V RTN input jack)	Adjust R17 for 10.0 (, 0.5) ohms
R19 (multimeter connected between +28 VDC test jack and EXT 28V RTN input jack)	Adjust R19 for 93 (, 2) ohms
INTLK INPUT switch	OFF
AUX 4.7V LOAD switch	NOM
+28V LOAD switch	NOM

(3) Connect power supply and test fixture

(4) Turn on all external test equipment and

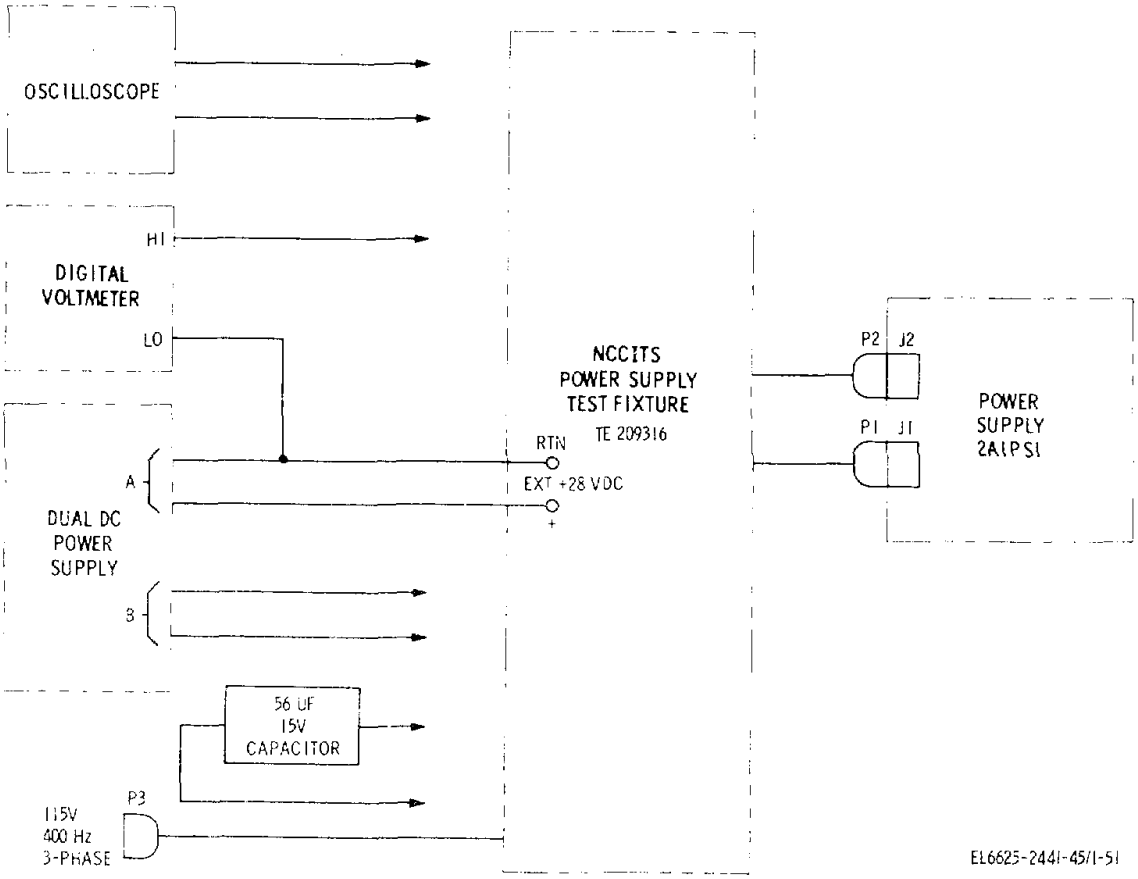


Figure 4-1. Power Supply 2A1PS1, Test Setup.

b. Test Procedures. Perform tests in the test procedure chart in the order listed. The Item column identifies the individual test to be performed. The Procedure column provides the step-by-step procedures and normal indication for each test. The Reference column locates the fault isolation and troubleshooting procedures that are to be performed when tests result in abnormal indications.

NOTE

Unless otherwise specified, all controls, indicators, and jacks are located on the test fixture.

c. Test procedure chart.

Sequence no.	***Item***	***Procedure***	***Reference***
1	Power supply turnon	Apply primary power to power supply under test as follows: a Set dual dc power supply A output to +24.0 (±2.0) V b. Set 115 VAC switch to ON c. Simultaneously set AC POWER and AUX AC switches to ON d. Observe the PS FAULT, VM NO-GO, +VCB, -VCB, and +5 VDC CB indicators are out e. Connect DVM to the following test jacks and observe indication of 0 (+O.5) Vdc: (1) FILTERED 4.7 VDC (2) +28 VDC (3) +5 VDC (4) +15 VDC (5) -15 VDC (6) -25 VDC	Paragraph 4-7
2	Auxiliary +4.7 V check	Connect digital voltmeter (DVM) and oscilloscope (scope) inputs to AUX 4.7 VDC test jack. Observe the following: a DVM indicates +4.7 (+O.3) V b. Ripple indication on scope less than 100 mV p-p	If voltage is out of tolerance refer to paragraph 4-39a. If voltage cannot be adjusted and/or ripple level is excessive, refer to paragraph 4-7.
3	Auxiliary +28 V check	Connect DVM and scope inputs to AUX 28V test jack. Observe the following: a. DVM indicates +28 (+2, -8) V b. Ripple indication on scope less than 2000 mV p-p	Paragraph 4-7

Sequence no.	Item	Procedure	Reference
4	Preparation for dc power on	a. Connect 56-,uF, 15-V capacitor checks + terminal to FILTERED 4.7 VDC test jack and - terminal to EXT 28V RTN test jack b. Set AUX 28V switch to ON	
5	+28V	Connect DVM and scope inputs to +28 VDC test jack and observe the following: ripple level is excessive refer a. DVM indicates +28.00 (+0.05, to paragraph 4-7. -0.06) V b. Ripple indication on scope less than 300 mV p-p	If voltage is out of tolerance refer to paragraph 4-39a If voltage cannot be adjusted and/or
6	+15V check	Connect DVM and scope inputs to +15 VDC test jack and observe the following: ripple level is excessive, refer a. DVM indicates +15.00 (±0.03)V to paragraph 4-7. b. Ripple indication on scope less than 250 mV p-p.	If voltage is out of tolerance refer to paragraph 4-39a. If voltage cannot be adjusted and/or
7	+5 V check	Connect DVM and scope inputs to +5 VDC test jack and observe the following: ripple level is excessive, refer a. DVM indicates +5.00 (+O.01)V to paragraph 4-7. b. Ripple indication on scope less than 100 mV p-p.	If voltage is out of tolerance, refer to paragraph 4-39a. If voltage cannot be adjusted and/or
8	Filtered +4.7 V	Connect DVM and scope inputs to FILTERED 4.7 VDC test jack and observe the following: ripple level is excessive, refer a. DVM indicates +4.70 (O.O1)V to paragraph 4-7 b. Ripple indication on scope less than 100 mV p-p.	If voltage is out of tolerance, refer to paragraph 4-39a. If voltage cannot be adjusted and/or
9	-15 V check	Connect DVM and scope inputs to -15 VDC test jack and observe the following: a DVM indicates -15.00 (±0.0) V b. Ripple indication on scope less than 250 mV p-p.	If voltage is out of tolerance, refer to paragraph 4-39a. If voltage cannot be adjusted and/or ripple level is excessive, refer to paragraph 4--7.
10	-25 V check	Connect DVM and scope inputs to -25 VDC test jack and observe the following: a DVM indicates -25.00 (+0.05) V to paragraph 4-7. b. Ripple indication on scope less than 250 mV p-p.	If voltage is out of tolerance, refer to paragraph 4-39a. If voltage cannot be adjusted and/or ripple level is excessive, refer

Sequence no.	Item	Procedure	Reference
		Note: If PS FAULT indicator lights, set AUX AC switch to OFF and back to ON.	
11	Rated load checks	Set the following load switches to RATED a -25V LOAD b. -15V LOAD c. +15V LOAD d +5V LOAD e +28V LOAD f FILTERED 4,7V LOAD	None
12	+28 V check	Connect DVM and scope inputs to +28 VDC test jack and observe the following: a. DVM indicates +28 00 (±0.28) V7 b Ripple indication on scope less than 300 mV p-p	Paragraph 4-7
13	+15 V check	Connect DVM and scope inputs to F15 VDC test jack and observe the following: a DVM indicates +15.00 (±015) V b Ripple indication on scope less than 250 mV p-p	Paragraph 4-7
14	+5 V check	Connect DVM and scope inputs to filter 2AlPS1FLIO and observe the following: a. DVMI indicates +5.00 (±0.15) V b Ripple indication on scope less than 100 mV p-p	Paragraph -l-7
15	Filtered ±4.7 V check	Connect DVM and scope inputs to filter 2AlPS1FLl2 and observe the following: a DVM indicates +4.70 (±0.14) V b Ripple indication oi scope I less than 100 mV p-p	Paragraph 4-7

16	-15 V check	Connect DVM and scope inputs to -15 VDC test jack and observe the following: a. DVM indicates -15.00 (±0.15) V b. Ripple indication on scope less than 250 mV p-p	Paragraph 4-7
17	-25 V check	Connect DVM and scope inputs to -25 VDC test jacks and observe the following: a. DVM indicates -25.00 (±0.25) V b. Ripple indications on scope less than 250 m V p-p	Paragraph 4-7
18	Voltage monitor circuit	Set all load switches to NOM Caution: When performing the checks in sequence no. 19 and 21, it is necessary to connect power supply outputs to the EXT 28V RTN test jack (ground). To prevent serious damage to the power supply, do not hold connection for more than 0.5 seconds.	None
19	Positive voltage monitor	Momentarily jumper +28 VDC no-go check input jack and observe the following: a. PS FAULT and VM NO-GO indicators light b. All power supply output voltages, except auxiliary +4.7 V and auxiliary +28 V, indicate 0 Vdc maximum	Paragraph 4-7 test jack to EXT 28V RTN
20	Power supply reset	Set AUX AC switch to OFF and back to on and observe that PS FAULT and VM NO-GO indicators go out.	Paragraph 4-7
21	Negative voltage monitor	Momentarily jumper -25 VDC no-go check test jack to EXT 28V RTN input jack and observe the following: a. PS FAULT and VM NO-GO indicators light	Paragraph 4-7

Sequence no.	Item	Procedure	Reference
		b. All power supply output voltages, except auxiliary +4.7 V and auxiliary +28 V, indicate 0 Vdc maximum	
22	Preparation for power supply interlock check	Set AUX 28V, AC POWER, and AUX AC switches to OFF. Set AUX AC switch back to ON	None
23	Power supply interlock output check	Connect INTERLOCK OUT test jack to AC POWER ON test jack and observe that PS FAULT indicator goes out	Paragraph 4-7
24	Power supply interlock input check	Set INTLK INPUT switch to INTLK and observe that PS FAULT indicator lights	Paragraph 4-7
25	Preparation for crowbar checks	a. Set INTLK INPUT switch to OFF	None
		b. Remove jumper from INTERLOCK OUT and AC POWER ON test jacks	
		c. Set AUX AC and 115 VAC switches to OFF (all test fixture indicators go out)	
		d. Disconnect power supply from test fixture	
		e Remove wires from 2A1PS1A7 pin 6 (fig. 5-18). Leave wires connected together	
		f Connect power supply to test fixture (fig. 4-1)	
		g. Set 115 VAC, AUX AC, and AC POWER switches to ON Verify that power supply output voltages, except auxiliary +4.7 V and auxiliary +28 V, are o Vdc maximum	
		h. Set all load switches to OFF and verify that AUX 28 V switch is set to OFF	
		Note: In sequence no. 26 through 31, the DVM indication must be monitored closely for sudden change.	

Sequence no.	Item	Procedure	Reference
26	Positive voltage crowbar check (+28 V)	a. Adjust dual dc power supply B output to 0 volts b Connect dual dc power supply B (+) output to +28 VDC test jack and (-) output to EXT 28V RTN input jack c Connect DVM input to +28 VDC test jack d. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly e. DVM indicates +33.75 (±1.25) V at point of change	If voltage level in e is out of tolerance, refer to paragraph 4-39b. If voltage level cannot be adjusted or DVM indication is not as specified in d, refer to paragraph 4-7
27	Positive voltage crowbar check (+15 v)	a. Set dual dc power supply B output to 0 volts b. Set AUX AC switch to OFF then back to ON in e, refer to paragraph 4-7 c. Connect dual dc power supply B (+) output to +15 VDC test jack d. Connect DVM input to +15 VDC test jack e. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly f DVM indicates +18.75 (+1.25) V at point of change	If voltage level in f is out of tolerance, refer to paragraph 4-39b. If voltage level cannot be adjusted or DVM indication is not as specified
28	+5 V crowbar check	a. Set dual dc power supply B output to 0 volts b. Set AUX AC switch to OFF then back to ON paragraph 4-7 c. Connect dual dc power supply B (+) output to +5 VDC test jack d. Connect DVM input to +5 VDC test jack e. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly f. DVM indicates +6.5 (-0.5) V at point of change	If voltage level in f is out of tolerance, refer to paragraph 4-39b. If voltage level cannot be adjusted or DVM indication is not as specified in e, refer to

Sequence no.	Item	Procedure	Reference
29	Positive voltage crowbar check (filtered +4.7 V)	Perform the following operations: a. Set dual dc power supply B output to 0 volts b. Set AUX AC switch to OFF then back to ON c. Connect dual dc power supply B (+) output to FILTERED 4.7 VDC test jack d. Connect DVM input to FILTERED 4.7 VDC test jack e. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly f DVM indicates +5.6 (+o.6) V at point of change	Paragraph 4-7
30	Negative voltage crowbar check (-15 V)	a. Set dual dc power supply B output to 0 volts b. Set AUX AC switch to OFF then back to ON to paragraph 4-7 c. Connect dual dc power supply B (-) output to -15 VDC test jack and B (+) output to EXT 28V RTN input jack d. Connect DVM input to -15 VDC test jack e. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly f DVM indicates -18.75 (±1.25) V at point of change	If voltage level in f is out of tolerance, refer to paragraph 4-39b. If voltage level cannot be adjusted or DVM indication is not as specified in e, refer
31	Negative voltage crowbar check (-25 V)	a. Set dual dc power supply B output to 0 volts b. Set AUX AC switch to OFF then back to ON to paragraph 4-7 c. Connect dual dc power supply B (-) output to -25 VDC test jack d. Connect DVM input to -25 VDC test jack	If voltage level in f is out of tolerance, refer to paragraph 4-39b. If voltage cannot be adjusted or DVM indication is not as specified in e, refer

Sequence no.	Item	Procedure	Reference
		e. Slowly increase dual dc power supply B output until DVM indication stops rising or drops suddenly f DVM indicates -30 (+i) V at point of change	
32	Shutdown	a. Set dual dc power supply B output to 0 volts b. Simultaneously set AC POWER and AUX AC switches to OFF c. Set 115 VAC switch to OFF d. Disconnect power supply 2AIPS1 from test fixture e. Connect wires removed in sequence no. 25, step e	None

4-6. Special Purpose Electrical Cable Assembly Checks and Troubleshooting (fig. 5-9)

Checks and troubleshooting of special purpose electrical cable assemblies consists of a visual inspection of connectors, contacts (pins and sockets), and exterior tubing and continuity checks. Additional troubleshooting may be performed by resistance and hi-pot checks from pin to pin and pin to connector shell. Procedures for removal and replacement of connectors and connector contacts are contained in paragraph 3-47. A typical configuration of special purpose electrical cable assemblies is illustrated in figure 3-5.

4-7. Power Supply 2A1PS1 Troubleshooting Chart

a. Troubleshooting Chart

The following chart provides procedures for isolating malfunctions to discrete components and modules. The numbers listed in the Sequence no. column correspond to the sequence numbers in the test procedure chart in paragraph 4-5c. The Symptom column lists the abnormal indications which may occur for the test with the corresponding sequence number. The Probable trouble column lists the discrete component(s) or module(s) most likely to cause the abnormal indication. The Corrective action column contains references to recommended procedures for correcting the trouble. When using standard fault isolation procedures, refer to figures 5-5 and 5-10 and the wire lists in appendix C, volume 2.

Sequence no.	Item	Procedure	Reference
1	a. All of the following indicators light: (1) PS FAULT	a. A2 or KT	a. Replace A2 (paragraph 4-12) or KI (paragraph 4-19)

Sequence no.	Item	Procedure	Reference
		(2) VM NO GO (3) +VCB (4) -VCB (5) +5 VDC CB	
	b. Any of the following indicators light:	b Probable troubles are as follows:	b. Perform the following corrective action:
	(1) PS Fault	(1) A2	(1) Replace A2 (paragraph 4-1 2)
	(2) VM NO-GO	(2) A5	(2) Replace A5 (paragraph 4--12)
	(3) +VCB	(3) A4	(3) Replace A4 (paragraph 4-12)
	(4) -VCB	(4) A3	(4) Replace A3 (paragraph 4-12)
	(5) +5 VDC CB	(5) A7 or Q1	(5) Replace A7 (paragraph 4-11) or Q1 (paragraph 4-10)
	c. Any of the following combinations of indicators light	c Probable troubles are as follows:	c Perform the following corrective action:
	(I) PS FAULT and VM NO-GO VR6, VR7, or VR8	(1) VR2, VR3, VR4,	(1) Perform standard fault isolation procedures
	(2) PS FAULT and +VCB	(2) VR4, VR6, or VR8	(2) Perform standard fault isolation procedures
	(3) PS FAULT and -VCB	(3) V2 or VR3	(3) Perform standard fault isolation procedures
	(4) PS FAULT and +5 VDC CB	(4) VR7	(4) Replace VR7 (paragraph 4-29)
	d. DVNI indications not as specified	d. A2 d, Replace A2 (paragraph 4-12)	
2	a. DVM indication not as specified	a. C4 through C9, R1, R2 R3, CR1, CR2, FLI, VRI, or T1	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR1	b. Replace VR1 (paragraph 4-15)
3	a. DVM indication not as specified	a. FL2	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. C6, C7, or CS	b Perform standard fault isolation procedures
5	a. DVM indication not as specified	a. A5, A4, FL7, VR4, RI1, R9, A6R7, A6R5, K2, A6CR6, C12, L2, A1Z1, A1Z2, A1T1, K1, C1 through C4. or A2	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR4	b. Replace CR4 (paragraph 4-16)

Sequence no.	Item	Procedure	Reference
6	a. DVM indication not as specified	a. A5, A4, VR6, FL9, R20, R21, or A6CR11	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR6	b. Replace VR6 (paragraph 4-17)
7	a. DVM indication not as specified	a. A5, A7, Q1 R22, C15, FLS, FL10, FL11, A6R12, A6CR7, C13, L3, A1Z3, A1Z4, ATTI, VR7A6, VR7L1, VR7R3 through VR7R4, VR7C1, VR7C2, VR7C3, VR7Q1, VR7Q2, or VR7CR1	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR7A1	b. Replace VR7A1 (paragraph 4-33)
8	a. DVM indication not as specified	a. A5, A4, VR8, R15, R16, R19, A6CR10, C14, FL12, or CR12	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR8	b. Replace VR8 (paragraph 4-15)
9	a. DVM indication not as specified	a. A1Z1 A122, L1, C11, A6R6, FL6, R2, A6R4, A6CR8, R13, R17, A5, A3, or VR3	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR3	b. Replace VR3 (paragraph 4-16)
10	a. DVM indication not as specified	a. A6CR5, R8, R10, FL5, A3, A5, or VR2	a. Perform standard fault isolation procedures
	b. Ripple level excessive	b. VR2	b. Replace VR2 (paragraph 4-16)
12	DVM indication not as specified and/or ripple level excessive	VR4	Replace VR1 (paragraph 4-16)
13	DVM indication not as specified and/or ripple level excessive	VR6	Replace VR6 (paragraph 4-16)
14	DVM indication not as specified and/or ripple level excessive	VR7A1, VR7Q1, or VR7Q2	Perform standard fault isolation procedures
15	a. DVM indication not as specified	a CR12 or VR8	a. Perform standard fault isolation procedures
	b Ripple level excessive	b. VRS	b. Replace VR8 (paragraph 4-15)
16	DVM indication not as specified and/or ripple level excessive	VR3	Replace VR3 (paragraph 4-16)
17	DVM indication not as specified	VR2	Replace VR2 (paragraph 4-16)

Sequence no.	Item	Procedure	Reference
19	PS FAULT and VM NO-GO indicators do not light aid/or DVM indications 01ot as specified	A2, A4, or A5	Perform standard fault isolation procedures
20	PS FAULT and VMI NO-GO indicators do not go out	A2	Replace A2 (paragraph 4-12)
21	PS FAULT and V NO-GO indicators do not light and/or DVM indications not as specified	A3 or A5	Perform standard fault isolation procedures
23	PS FAULT indicator does not go out	A2	Replace A2 (paragraph A-12)
24	PS FAULT indicator does not light	A2	Replace A2 (paragraph 4-12)
26	DVM indication not as specified	A4 or A2	Perform standard fault isolation procedures
27	DVM indication not as specified	A4	Replace A4 (paragraph 4-12)
28	DVM indication not as specified	A7 or A2	Perform standard fault isolation procedure
29	DVM indication not as specified	A4	Replace A4 (paragraph 4-12)
30	DVM indication not as specified	A3 or A2	Perform standard fault isolation procedures
31	DVM indication not as specified	A3	Replace A3 (paragraph 4-1 2)

Section III. REMOVAL, REPLACEMENT, REPAIR,AND ADJUSTMENTS

4-8. General

Procedures in this section provide instructions for removal and replacement of components, assemblies, and modules of power supply 2AlPS1 and repair of special purpose electrical cable assemblies.

NOTE

When performing replacement procedures, use sealant on attaching hardware when a mechanical locking device (lockwasher, locknut, etc) is not specified.

4-9. Instructions for Removal and Replacement of Power Supply 2AlPSI Modules, Assemblies, and Components

Procedures in paragraphs 4-10 through 4-38 apply to modules, assemblies, and components of power supply PSI. Refer to figure 5-10for location of components not indexed in figure 4-2. Upon completion of removal and replacement procedures in paragraph 4-10 through 4-38, perform test procedures in paragraph 4-5.

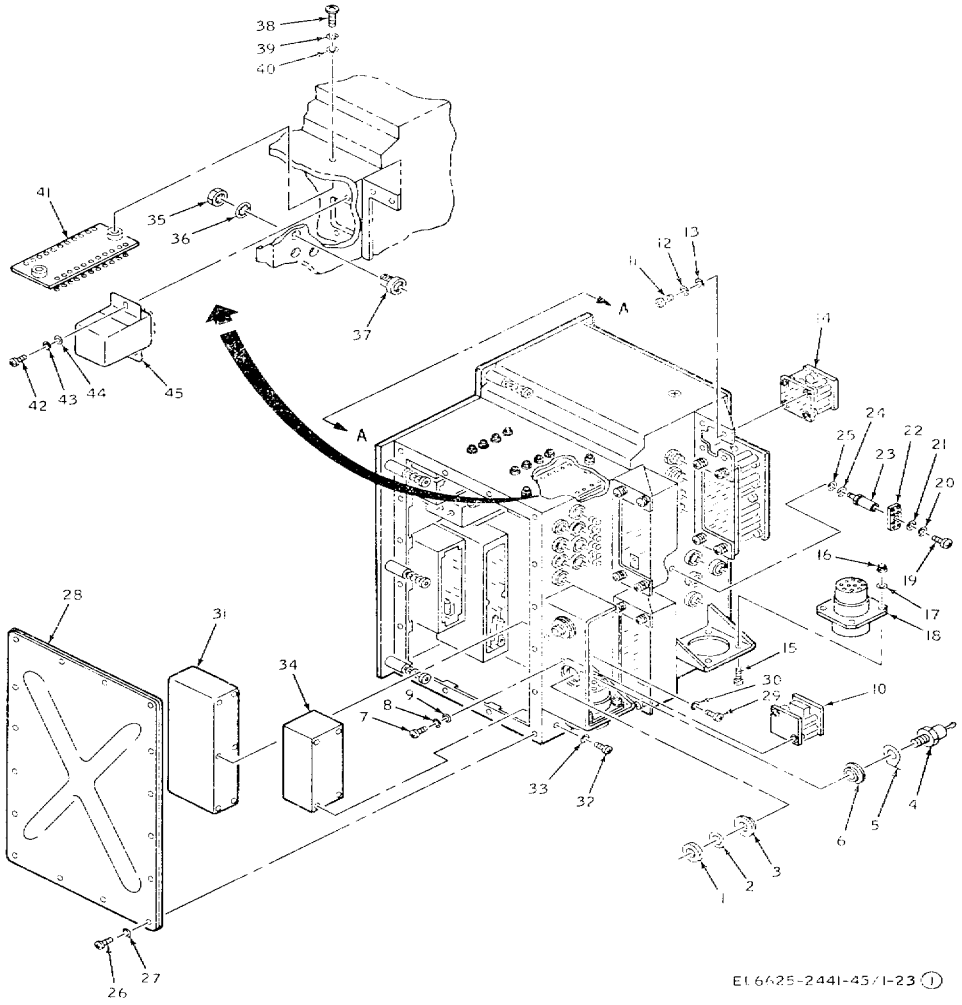


Figure 4-2 (1). Power Supply 2A IPSI, exploded view (part 1 of 3)

1 Nut (2)
2 Flatwasher (2)
3 Insulating shoulder washer (2)
4 Semiconductor (2; 2AlPSlQ1, 2A1PSlCR12)
5 Lug (2)
6 Insulating shoulder washer (2)
7 Screw (2)
8 Locekwasher (2)
9 Flatwasher (2)
10 +5 V crowbar 2AlPSlA7
11 Screw (16)
12 Lockwasher (16)
13 Flatwasher (16)
14 Module (4: 2AlPSlA2, 2AlPSlA3, 2A1PS1A4, 2AlPSlA5)
15 Screw (8)
16 Locknut (8)
17 Flatwasher (8 i0 Flat40.hcr 1'9
18 Connector (2; 2AIPSlJl, 2AlPSlJ2)
19 Screw
20 Lockwasher
21 Flatwasher
22 Bus bar 2AIPSlW1
23 Insulated standoff
24 Lockwasher
25 Flatwasher
26 Screw (14)
27 Flatwasher (11t)
28 Covet-
29 Screw (12)
30 Flatwashec (12)
31 Voltage regulator (2; 2A1 PS1 VR,R 2A1PS1VR8)
32 Screw (16)
33 Flatwasher (16)
34 Voltage regulator (4; 2AlPSlVR2, 2AlPS1VR3, 2AlPS1 VR4, 2AlPS1VR6)
35 Nut (12)
36 Lockwasher (12)
37 Filter (12, 2AlPSlFLl through 2AlPSlFL12)
38 Screw (2)
39 Lockwasher (2)

41 Component assembly 2A1PS1A6
42 Screw (3)
43 Lockwasher (3)
44 Flatwasher (3)
45 Relay 2A1IPS1K1

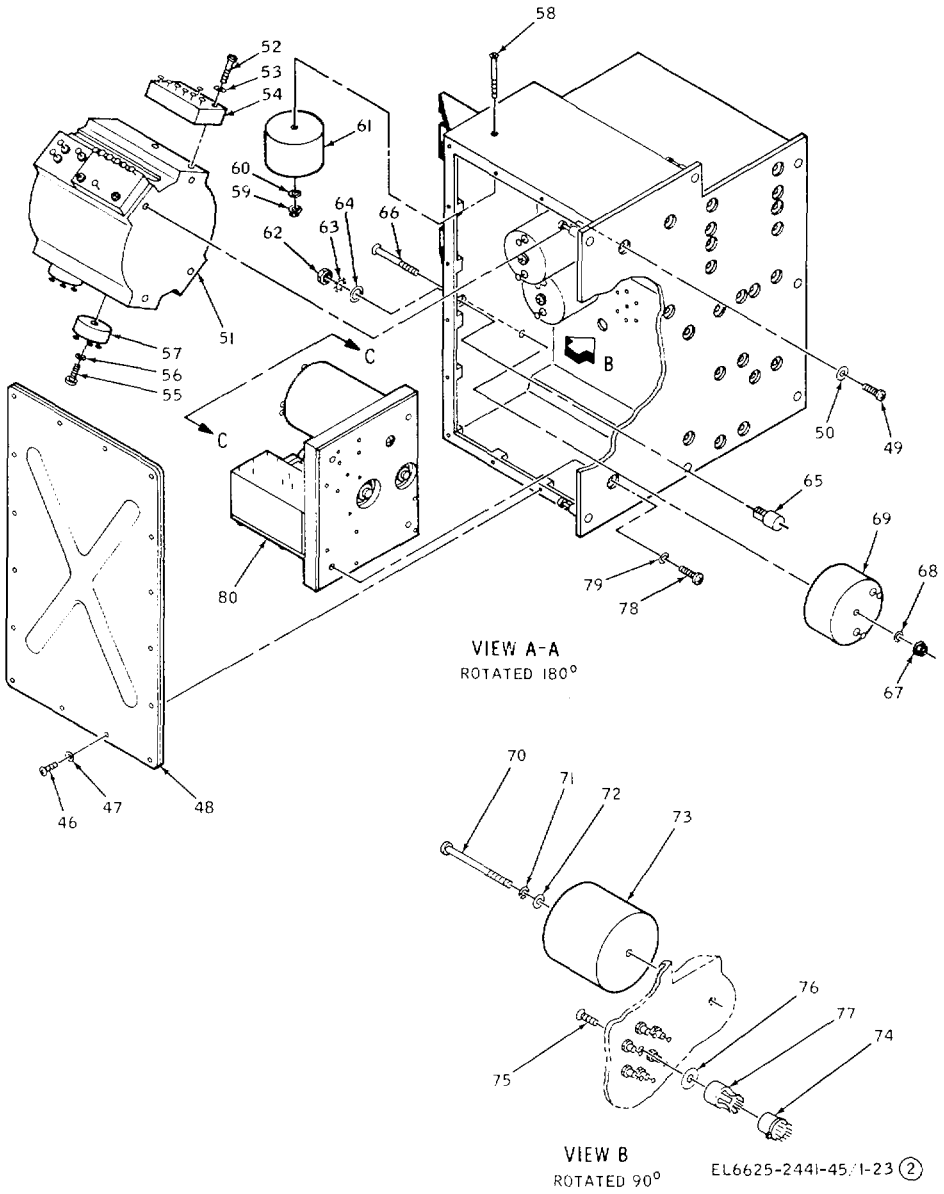


Figure 4-2 (2). Power Supply 2A1PS1, exploded view (part 2 of 3).

46 Screw (14)
47 Flatwasher (14)
48 Cover
49 Screw (4)
50 Flatwasher (4)
51 Transformer rectifier assembly 2AlPSIA1
52 Screw (4)
53 Flatwasher (4)
54 Diode assembly (2; 2AlPSlAlZ3, 2AIPSIAlZ4)
55 Screw (2)
56 Flatwasher (2)
57 Diode assembly (2; 2AIPSlAIZ1, 2AIPSlAlZ2)
58 Screw
59 Locknut
60 Flatwasher
61 Transformer 2ATPSIT1
62 Nut (5)
63 Lockwasher (5) 2AlPSIVR7
64 Flatwasher (5)
65 Capacitor (5, 2AlPSlCl through 2AIPSlC5)
66 Screw
67 Locknut
68 Flatwasher
69 Inductor 2AlPSIL3
70 Screw (2)
71 Lockwasher (2)
72 Flatwasher (2)
73 Inductor (2; 2AlPSILT, 2AlPSlL2)
74 Relay 2AlPS1K2
75 Screw
76 Flatwasher
77 Heat sink 2AIPSIMP4
78 Screw (5)
79 Flatwasher (5)
80 +5 V switching regulator

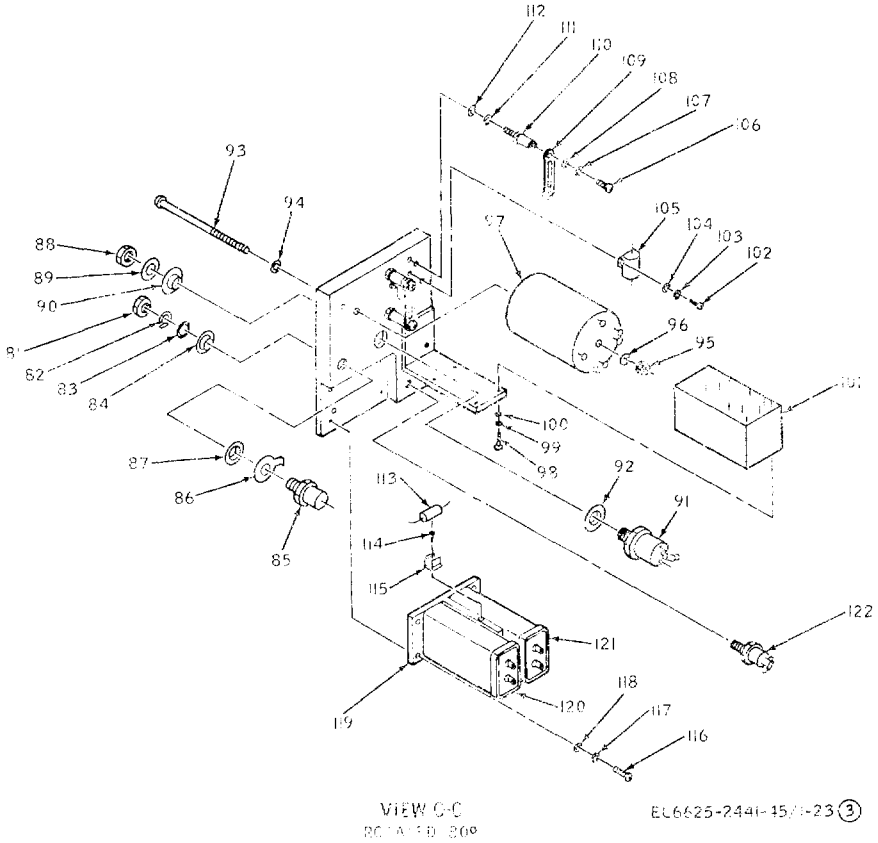


Figure 4-2 (3) . Power Supply 2A1PS1, exploded view (part 2 of 3).

81 Nut
82 Lockwasher
83 Flatwasher
84 Insulating shoulder washer
85 Diode 2AlPSlVR7CRI
86 Lug
87 Insulating shoulder washer
88 Nut
89 Flatwasher
90 Insulating shoulder washer
91 Transistor 2A1PS1VR7Q2
92 Insulating shoulder washer
93 Screw
94 Flatwasher
95 Locknut
96 Flatwasher
97 Inductor 2AlPS1VR7LI
98 Screw (4)
99 Lockwasher (1)
100 Flatwasher (4)
101 Regulator controller assembly 2A1PS1VR7A1
2A1PS1VR7Q1
102 Screw (4)
103 Lockwasher (4)
104 Flatwasher (4)
105 Resistor (2; 2A1PS1VR73, 2A1PS1VPSR4)
106 Screw (4)
107 Lockwasher (4)
108 Flatwasher (4)
109 Bus bar (2; 2A1PS1VR7W1, 2A1PS1VPSR7W2)
110 Insulated standoff (4i
111 Lockwasher (4)
112 Flatwasher (1)
113 Capacitor 2A1PS1VR7C3,
114 Screw
115 Clip
116 Screw (4)
117 Lockwasher(4)
118 Flatwasher (1)
119 Capacitor bracket
120 Capacitor 2A1PS1VR7C1
121 Capacitor 2A1PS1VR7C2
122 Transistor

4-10. Removal and Replacement Semi-conductors 2A1PS1CR12 and 2A1PS1Q1 (fig. 4-9,)

a. Removal

NOTE

When removing semi-conductor 2A1PS1Q1, do not remove resistor 2A1PS1R22 or capacitor 2A1PS1R15 from 2A1PS1Q1 terminals.

(1) Tag and unsolder wires from semi conductor and lug.

(2) Remove nut (1), flatwasher (2), insulating shoulder washer (3), semiconductor (4), lug (5) and insulating shoulder washer (6)

b. Replacement

NOTES

1. Before insulating semiconductor 2A1PS1Q1, attach replacement resistor 2A1PS1R22 and capacitor 2A1PS1C15 to transistor terminals.
2 Apply a thin coating of insulating compound to insulating shoulder washer (3) and (6) before installing

(1) Attach semiconductor (4) to mounting bracket using lug (5), insulating shoulder washer (6) and (3) flatwasher (2), and nut 1)

(2) Solder tagged wires to proper semiconductor terminals and lug.

4-11. Removal and Replacement of +5V Crowbar 2A1PS1A7

a. Removal

(1) Tag and remove wires from terminals of +5 V crowbar A7

(2) Remove two screws (7), lockwashers (8) , and flatwashers (9); remove +5 V crowbar A7 (10)

b. Replacement

(1) Attach +5 V crowbar A7 (10) to bracket using two flatwashers (9), lockwashers (8, and screws (7)

(2) Solder tagged wires to proper terminals of +5 V crowbar A7.

4-12. Removal and Replacement of Modules 2A1PS1A2 through 2A1PS1A5

a. Removal

(1) Tag and unsolder wires from assembly terminals.

(2) Remove four screws (11), Lockwashers (12) and flatwashers (13); remove assembly (14)

b. Replacement

(1) Attach assembly (14) to bracket using four flatwashers (13) Lockwashers and screws (11).

(2) Solder tagged wires to proper assembly terminals.

4-13. Removal and Replacement for Connectors 2A1PS1J1 and 2A1PS1J2.

a. Removal

(1) Tag and remove wires and contacts from connector.

(2) Remove four screws (15), locknut s (16), and flatwashers (17); remove connector (18)

b. Replacement

(1) Attach connector (18) to bracket using four flatwashers (17), locknuts (16), and screws (15)

(2) Insert tagged wires and contacts into connector.

4-14. Removal and Replacement of Bus Bar 2A1PS1W1

a. Removal

(1) Unsolder wires from bus bar W1.

(2) Remove scr4ew (19), lockwasher (20), and flatwasher (21); remove bus bar W1 (22). If insulated standoff; remove lockwasher (24) and flatwasher (25)

b. Replacement

(1) If insulated standoff (23) has been removed, attach insulated standoff, flatwasher (25), and lockwasher (24) to power supply chassis. Attach bus bar W1 (22) to insulated standoff (23) using flatwasher (21), lockwasher (20), and screw (19)

(2) Solder wires to bus bar W1

4-15. Removal and Replacement of Voltage Regulators 2A1PS1VRA1 and 2A1PS1VR8 (fig 4-2)

a. Removal

(1) Remove 14v screws (26) and flatwashers (27); remove cover (28).
(2) Tag and unsolder wires from terminals of voltage regulator
(3) Remove six screws (29), and flatwashers, (30), remove voltage. Regulator (31) with discrete components (s) attached..

b. Replacement

NOTE

Before installing replacement voltage regulator, mount discrete components on voltage regulator. Refer to figures 5-5 and 5-10 for reference designations and location

(1) .attach voltage regulator (31); to power supply chassis using six flatwashers (30) and screws (29-).
(2) Solder tagged wires to voltage regulator terminals.
(3) attach cover (28) using 14 flatwashers (27) and screws (26). Do not use two corner holes adjacent to power supply -mounting plate.

4-16. Removal and Replacement of Voltage Regulators 2A1PS1VR2, 2A1PS1VR3, 2A1PS1VR4, AND 2A1-S1VR6

a. Removal

(1) Remove 14 screws (26) and flatwashers (27); remove cover (28).
(2) Tag and unsolder wires from voltage regulator terminals
(3) Remove four screws (32) and flatwasher (38); remove voltage regulator (34) with discrete components (s) attached

b. Replacement

NOTE

Before installing voltage regulator, mount discrete components on replacement voltage regulator. Refer to figure 5-5b and 5-10 for reference designations locations.

(1) Attach voltage regulator (34) to power supply chassis using four flatwashers (33) and screws (32)
(2) Solder tagged wires to voltage regulator terminals.
(3) Attach cover (28) using 14 flatwashers (27) and screws (26). Do not use corner holes adjacent to power supply mounting plate.

4-17. Removal and Replacement of Filters 2A1PS1FL1 through 2A1PS1FL12 (fig 4-2)

When performing removal and replacement procedures for filters FL1, FL2, FL4 through FL7, FL9, or FL12, remove and replace cover (28). For filters FL3, FL8, FL10, or FL11, remove and replace cover (48)

a. Removal

(1) Remove 14 screws (26) or (46) and flatwashers (27) or (47); remove cover (28) or (48)
(2) Unsolder wires from filter terminals
(3) Remove nut (35) using Lockwasher (36) and nut (35)

b. Replacement

(1) Attach filter 37) using lockwasher (36) and nut (35)
(2) Solder wires to filer terminals

(3) Attach cover (28) or (48) using 14 Flatwashers (27) or (47) and screws (26) or (46). Do not use two corner holes adjacent to power supply mounting plate.

4-18. Removal and Replacement of Component Assembly 2A1PS1A6 (fig. 4-2)

a. Removal

(1) Remove 14 screws (26) and flatwashers (27); remove cover (28).
(2) Tag and unsolder wires from component assembly A6 terminals.
(3) Remove two screws (38), lockwashers (39), and flatwashers (40); remove component assembly A6 (41).

b. Replacement

(1) Attach component assembly A6 (41) to power supply chassis using two flatwashers (40), lockwashers (39), and screws (38).
(2) Solder tagged wires to component assembly A6 terminals.
(3) Attach cover (28) using 14 flatwashers (27) and screws (26). Do not use two corner holes adjacent to power supply mounting plate.

4-19. Removal and Replacement of Relay 2A1PS1K1 (fig. 4--2)

a. Removal

(1) Remove 14 screws (46) and flat washers (47): remove cover (48).
(2) Tag and unsolder wires from relay terminals.
(3) Remove 14 screws (26,) flatwashers, (27); remove cover (28).
(4) Remove three screws (42), lockwashers (43), and flatwashers (44); remove relay K1 (45).

b. Replacement

NOTE

Before installing relay K1, attach diode 2A1PS1CR3 to pin X1 and X2 of relay K1l. Refer to figure 5-10 for polarity.

(1) Attach relay K 1 (45) to power supply chassis using three flatwashers (44), lockwashers (43), and screws (42)
(2) Solder tagged wires to relay K1 terminals.
(3) Attach cover (48) using 14 flatwashers (47) and screws (46).
(4) Attach cover (28) using 14 flatwashers (27) and screws (26). Do not use two corner holes adjacent to power supply mounting plate.

4-20. Removal and Replacement of Transformer Rectifier Assembly 2A1PS1A1 (fig. 4-2)

a. Removal

(1) Remove 14 screws (46) and flatwashers (47); remove cover (48).
(2) Remove four screws (49) and flatwashers (50). Carefully remove transformer rectifier assembly A1 (51) from power supply chassis.
(3) Tag and unsolder all input and output leads from transformer rectifier assembly A1 terminals.

b. Replacement

(1) Solder tagged wired to transformer rectifier assembly A1 terminals

CAUTION

Insure that wiring is clean when installing transformer rectifier assembly A1 in power supply chassis.

(2) Attach transformer rectifier assembly A1 (51) to power supply chassis using four flatwashers (50

(3) Attach cover (48) using 14 flatwashers (47) and screws (46). Do not use two comer holes adjacent to power supply mounting plate.

4-21. Removal and Replacement of Diode Assemblies 2A1PS1A1Z3 and 2AlPSlAlZ4 (fig. 4-2)

a. Removal

(1) Remove cover and transformer rectifier assembly as described in 4-20a(1) and (2).
(2) Tag and unsolder wires from diode assembly terminals.
(3) Remove two screws (52) and flatwashers (53); remove diode assembly (54) from transformer rectifier assembly 2A1PS1A1 (51).

b. Replacement

(1) Attach diode assembly (54) to transformer rectifier assembly 2A1PS1A1 (5i) using two flatwashers (53) and screws (52).
(2) Solder tagged wires to diode assembly terminals.
(3) Install transformer rectifier assembly 2AlPS1Al and cover as described in 4-20b(2) and (3).

4-22. Removal and Replacement of Diode Assemblies 2AlPSIA1Z1 and2AlPSlAlZ2 (fig. 4-2)

a. Removal

(1) Remove cover and transformer rectifier assembly as described in 4-20a(1) and (2).
(2) Tag and unsolder wires from diode assembly terminals.
(3) Remove screw (55) and flatwasher (56); remove diode assembly (57) from transformer rectifier assembly 2AlPS1A1 (51).

b. Replacement

(1) Attach diode assembly (57) to transformer rectifier assembly 2A1PSlA1 (51) using flatwasher (56) and screw (55).
(2) Solder tagged wires to diode assembly terminals.
(3) Install transformer rectifier assembly 2AlPSlA1 and cover as described in 4-20b(2) and (3).

4-23. Removal and Replacement of Transformer 2AIPSlTl (fig. 4-2)

a. Removal

(1) Remove 14 screws (46) and flatwashers (47); remove cover (48).
(2) Tag and unsolder wires from transformer TI terminals.
(3) Remove screw (58), locknut (59), and flatwasher (60): . remove transformer T1 (61).

b. Replacement

(1) Attach transformer T1 (61) to power supply chassis using flatwasher (60), locknut (59), and screw (58).
(2) Solder tagged wires to transformer T1 terminals, (3) Attach cover (48) using 14 flatwashers (47) and screws (46).

4-24. Removal and Replacement of Capacitors 2AIPSlCl through 2A1PS1C5 (fig. 4-2)

a. Removal

(1) Remove 14 screws (46) and flatwashers (47); remove cover (48).
(2) Tag and unsolder wires from capacitor terminals.
(3) Remove nut (62), lockwasher (63), and (flatwasher (64), remove capacitor (65).

b. Replacement

(1) Attach capacitor (65) to power supply chassis using flatwasher (64), lockwasher (63), and nut (62)

(2) Solder tagged wires to capacitor terminals.

(3) Attach cover (48) using 14 flatwashers (47) and screws (46). Do not use two corner holes adjacent to power supply mounting plate.

4-25. Removal and Replacement of Inductor 2A1PS1L3 (fig 4-2)

a. Removal.

(1) Remove 14 screws (46) and flatwasher (47); remove4 cover (48).

(2) Tag and unsolder wires from inductor L3 terminals.

(3) Remove screw (66) locknut (67) and flatwashers (68); remove inductor L3 (69

b. Replacement

(1) Attach inductor (73) to power supply chassis using flatwasher (72), lockwasher (71), and screw (70).

(2) Solder tagged a. wires to inductor L3 terminals..

(3) Attach cover (48) using 14 flatwashers (47) and screws (47). Do not use two corner holes adjacent to power supply mounting plate.

4-27. Removal and Replacement of Relay 2A1PS1K2 (fig. 4-2)

a. Removal

(1) Remove 14 screws (26) and flatwashers (27); remove cover (28).

(2) Unsolder relay K2 leads from terminals 2A1PS1E4 through 2A1PS1E9.

(3) Note position of relay index tab, and carefully pull relay K2 (74) from heat sink 2A1PS1MP4.

b. Replacement

(1) Carefully insert relay K2 (74) into beat sink 2A1PS1MP4 (77). Insure that index that is in same position as noted in removal of tab.

(2) Solder leads of relay K2 to proper terminals (refer to figure 5-5 for connections).

(3) Attach cover (28) using 14 flatwashers (27) and screws (26). Do not use holes adjacent to power supply mounting plate.

4-28. Removal and Replacement of Heat Sink 2A1FSIAP4 (fig. 4-2.

a. Removal.

(1) Remove K2 as described in 4-276a.

(2) Remove 14 screws (46) and flatwashers (47); remove cover (48),

(3) Remove screw (75)) and flatwasher (76); remove cover heat sink MP4 (77)

b. Replacement

(1,) Attach heat sink MP4 (77) to power supply chassis using flatwasher (76) and screw (75).

(2) Attach cover (48) using 14 flatwashers (47) and screws (46).

(3) Install relay 2AiPS1K2 and cover as described in 4—27b.

4-29. Removal and Replacement of +5V Switching Regulator 2A1PS1VR7 (fig. 4--2)

a. Removal

(1) Remove 14 screws (46) and flatwashers (47); remove cover (48).

(2) Tag and unsolder all input and output wires from +5 V switching regulator VR7 terminals.

(3) Remove five screws (78) and flatwashers ('47); remove +5 V switching regulator VR7 (80)

b. Replacement

(1) Attach +5 V switching regulator VR7 (80) to power supply chassis using five flatwashers (79) and screws (78).

(2) Solder tagged wires to 45 V s regulator VR7 terminals.

(3) Attach cover (48) using 14 flatwashers (47) and screws (46). Do not use two corner holes adjacent to power supply mounting plate.

4-30. Removal and Replacement of Diode 2A1PS1VR7CR1 (fig. 4-2)

a. Removal

(1) Remove +5 V switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Tag and unsolder wires from diode CR1 and lug.

(3) Remove nut (81), lockwasher (82), flatwasher (83), and insulating shoulder (84); remove diode CR1 (85). lug (86), and insulating shoulder washer (87).

b. Replacement

NOTE

Before installing diode CR1. apply thin coating of insulating compound to insulating shoulder washers (84) and (87).

(1) Attach insulating shoulder washer (87), lug (86) and diode CR1 (85) to base using insulating shoulder washer (83), lockwasher (82), and nut (81)

(2) Solder tagged wires to lug and diode CR1.

(3) Install +5 V switching regulator 2A1PS1VR7 in power supply chassis 3s described in 4-29b.

4-31. Removal and Replacement of Transistor 2A1PS1VR7Q2 (fig. 4-2)

a. Removal

(1) Remove +5 V switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Tag and unsolder wires from transistor Q2 terminals.

(3) Remove nut (88), flatwasher (89) and insulating shoulder washer (90); 1.remove transistor Q2 (91), with resistor 2A1PS1VR7R2 attached, and insulating shoulder washer ('92).

b. Replacement

NOTE

Before installing transistor Q2, apply a thin coat of insulating compound to insulating sho9ulder washers (90) and (92)

(1) Attach insulating shoulder washer (892) and transistor Q2 (91) to mounting shoulder washer (90), flatwasher (89), and nut (88).

(2) Solder tagged wires and replacement resistor 2A1PS1VR7R2 to proper transistor Q2 terminals.

(3) Installed +5 V switching regulator 2A1PS1VR7 as described in 4-29b.

4-32. Removal and Replacement of Inductor 2A1PS1VR7L1 (fig 4-2)

a. Removal.

(1) Remove +5 V switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Tag and unsolder wires from regulator controller assembly A1 terminals.

(3) Remove screws (93), lockwashers (94), Locknut, flatwashers (96); remove regulator inductor L1 (97).

b. Replacement

(1) Attach inductor L1 (97) using flatwasher (96), locknut (95), flatwasher (94) and screw (93).

(2) Solder tagged wires to inductor L1 terminals.

(3) Install +5 V switching regulator 2A1PS1VR7 as described in 4-29b.

4-33. Removal and Replacement of Regulator Controller Assembly 2A1PS1VR7A1 (fig 2)

a. Removal

(1) Remove +5 V switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Tag and unsolder wires from regulator controller assembly terminals.

b. Replacement

(1) Attach regulator controller assembly A1 (101) to the mounting bracket using four flatwashers (100), lockwashers (99), and screws (98).

(2) Solder tagged wires to regulator controller assembly A1 terminals.

(3) Install +5 V switching regulator 2A1PS1VR7 as described in 4-29h.

4-34. Removal and Replacement of Resistors 2A1PS1VR7R3 and 2A1PS1VR7R4 (fig. 4-2)

a. Removal

(1) Remove +5 V switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Unsolder wires from resistor terminals.

(3) Remove two screws (102), lockwashers (103), and flatwashers (104); remove resistor (105).

b. Replacement

(1) Attach resistor (105) to mounting base using two flatwashers (104), lockwashers (103), and screws (102).

(2) Solder wires to resistor terminals.

(3) Install +5 V switching regulator 2A1PS1VR7 as describe in 4-295b.

4-35. Removal and Replacement of Bus Bars 2A1PS1VR7WI and 2A1PS1VR7W2 and Insulated Standoffs (fig. 4-2)

The following removal and replacement procedures include removal and replacement of

the insulated standoffs. Remove and replace bus bar or insulated standoff as required.

a. Removal

(1) Remove +5 V switching regulator 2AlPSlVR7 as described in 4-29a.
(2) Unsolder wires from bus bar only if bus bar is to be replaced.
(3) Remove two screws (106), lockwashers (107), and flatwashers (108); remove bus bar (109).
(4) Remove two insulated standoffs (110), lockwashers (111), and flatwashers (112).

b. Replacement

(1) Attach two flatwashers (112), lockwashers (111), and insulated standoff (110) to mounting base.
(2) Attach bus bar (109) to insulated standoffs (110) using two flatwashers (108), lockwashers (107), and screws (106).
(3) Solder wires to bus bar if bus bar was replaced.
(4) Install +5 V switching regulator 2AlPSlVR7 as described in 4-29b.

4-36. Removal and Replacement of Capacitor 2A1PS1VR7C3 and Clip (fig. 4-2)

a. Removal

(1) Remove +5 V switching regulator 2AlPSlVR7 as described in 4-29a.
(2) Unsolder capacitor C3 leads from diode 2A1PS1VR7CR1 and transistor 2AlPSIVR7Q2. Remove capacitorC3 (113) from clip (115).
(3) Remove screw (114) and clip (115) from capacitor bracket (119).

b. Replacement

(1) Attach clip (115) to capacitor bracket (119) using screw (114).
(2) Place capacitor C3 (113) in clip (115). Solder capacitor C3 leads to diode 2A1PS1VR7CR1 and transistor 2A1PS1VR7Q2.
(3) Install +5 V switching regulator 2A1PS1VR7 as described in 4-29b.

4-37. Removal and Replacement of Capacitors 2A1PS1VR7C1 and 2AlPSlVR7C2 (fig. 4-2)

The following removal and replacement procedures provide the necessary instructions for replacing capacitors C1 and C2. The capacitors are bonded to the capacitor bracket with epoxy adhesive.

a. Removal

(1) Remove +5 V switching regulator 2A1PSlVR7 as described in 4-29a.
(2) Remove capacitor 2A1PSlVR7C3 (113) from clip (115). Do not unsolder capacitor C3 leads.
(3) Tag and unsolder wires from capacitor C1 and C2 terminals.
(4) Remove four screws (116), lockwashers (117), and flatwashers (118); remove capacitor bracket (119) with capacitors C1 (120) and C2 (121) attached.
(5) Remove faulty capacitor from capacitor bracket and clean all epoxy adhesive residue from capacitor bracket.

b. Replacement

(1) Apply thin film of epoxy adhesive to bonding surfaces of replacement capacitor and capacitor bracket. Press surfaces together firmly.
(2) Cure epoxy adhesive in precision oven for 2 hours minimum at 165° (+5°)F or 7 days at room temperature of 750 (+-5°)F.

(3) Attach capacitor bracket (119) to mounting base using four flatwashers (118), lockwashers (117) and screws (116).

(4) Solder tagged wires to terminals of capacitors C1 (120) and C2 (121).

(5) Insert capacitor 2A1PS1VR7C3 into clip (115).

(6) Install +5 V switching regulator 2A1PS1VR7 as; described in; 4-29b.

4-38. Removal and Replacement of Transistor 2A1PS1VR7Q1 (fig. 4--2)

a. Removal

(1) Remove -+-5 V Switching regulator 2A1PS1VR7 as described in 4-29a.

(2) Tag and unsolder wires from transistor terminals.

(3) Remove transistor Q1 (122) with resistor 2A1PS1VR7R1 attached.

b. Replacement

(1) Screw transistor Q1 (122) into mounting base.

(2) Solder resistor 2A1PS1VR7R1 and tagged wires to proper transistor Q1 terminals.

(3) Install +5 V switching regulator 2A1PSVIR7 as described in 4-29b.

4-39. Special Purpose Electrical Cable Assembly Repair

Repair of special purpose electrical cable assemblies is limited to replacement of connectors or connector contracts. A typical -configuration of single and multi-conductor shielded cable is illustrated in figure 3-5. Refer to figure 5-9 for special purpose electrical cable assembly wiring. Paragraph 3-47 lists the cable contact tools. Proceed as. described in paragraph 3--47a and, use standard maintenance practices when replacing, connector contacts..

WARNING

Power supply 2A1PS1 contains voltages which may cause DEATH or SERIOUS INJURY. Be careful when making adjustments.

CAUTION

Some of power supply 2A1PS1 adjustments are very close to exposed pins and terminals. Use extreme caution when making adjustments to prevent damage to power supply 2A1PS1.

4-40. Power Supply 2A1PS1 Adjustments (fig. 5 10)

Procedures contained in this paragraph provide instructions for adjusting power supply voltages .and crowbar thresholds. These adjustments are made in conjunction with test procedures and after replacement of modules.

a. Power Supply 2A1PS1 Voltage Adjustment Chart. The following chart lists the power supply voltage adjustments with the corresponding potentiometers. The numbers listed in the Sequence no. column correspond to the sequence numbers in the test procedure chart (paragraph 1-5c) for tests in which voltage adjustments are recommended. The Potentiometer column lists the reference designation of the potentiometer to be adjusted. The DVM indication column lists the voltage requirement of each adjustment. Refer to figure 5-0 for potentiometer locations.

Sequence no.	Potentiometer	DVM indication (V)		
2	VR1R13	+4.69	to	+4.71
5	VR4R14	+27.94	to	+28.05
6	VR6R14	+14.97	to	+15.03
7	VR7AIR13	+4-99	to	+5.01
8	VR8R13	+4 69	to	+4.71
9	VR3R14	+14 97	to	-15.03
10	VR2R14,	-24.95	to	-25.05

b. Power Supply 2A1PS1 Crowbar Adjustment C1iart. The following chart lists the adjustments required to set each crowbar threshold to the proper level. The numbers listed in the Sequence no. column correspond to the sequence numbers in the test procedure chart (paragraph 4-5c) for tests in which crowbar adjustments are recommended. The Potentiometer column lists the reference designation of the potentiometer associated with each crowbar. The DVM indication column lists the acceptable voltage range of each adjustment. It may be necessary to repeat

Sequence no.	Potentiometer	DVM indication (V)		
26	V4R14	+32.5	to	+35.0
27	V4R14	+17.5	to	+20.0
28	V7R7	+6.07	to	+7.0
30	V3R16	-17.5	to	-20.0
31	V3R16	-29.0	to	-31.0

Section IV. DEPOT OVERHAULS STANDARDS

4-41. Applicability of Depot Overhaul Standards

The tests outlined in this section are designed to measure the performance capability of a repaired equipment. Equipment that is to be returned to stock should meet the standards given in these tests.

4-42. Applicable References

a. Repair Standards. Applicable procedures and the general standards for repaired electronic equipment are given in TB S1G 355-1, Depot Inspection Standard for Repaired Signal Equipment; TB S1G 355-2, Depot Inspection Standard for Refinishing Repaired Signal Equipment; and TB S1G 355-3, Depot Inspection Standard for Moisture and Fungus Resistant Treatment and TM, -6625?441-45-1 the procedures of the referenced sequence number to obtain the desired results. Refer to figure -5-10 for potentiometer locations. form a part of the requirements for testing the equipment.

b. Modification Work Orders. Perform all applicable modification work orders pertaining to this equipment before making the tests specified. DA Pam 310-7 lists all current MWO's.

4-43. Test Facilities Required

The test facilities required are identical to those specified in paragraph 4-2.

4-44. Test Procedures

Test procedures are the same as the confidence check and automatic self test procedures in TM 11-6625-2441-12. Acceptable standards of performance for depot overhaul are the same as those given in these tests.

APPENDIX A

REFERENCES

The following publications contain information applicable to the operation and maintenance of Test Set, Navigational Computer-Control Indicator AN/ASM-386.

DA Pam 310-4	Military Publications: Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	U.S. Army Equipment Index of Modification Work Orders.
TM 11-6625-2441-12	Operator's and Organizational Maintenance Manual: Test Set, Navigational Computer-Control Indicator AN/ASM-386.
TM 11-6625-2441-20P	Organizational Maintenance Repair Parts and Special Tools List: Test Set, Navigational Computer-Control Indicator AN/ASMA--386.
TM 11-6625-2441-45P	General Support and Depot Maintenance Repair Parts and Special Tools List: Test Set, Navigational Computer-Control AN/ASM-386.

APPENDIX B
PROGRAM LISTING

Section I. INTRODUCTION

B-1. General

This appendix contains the self-test program listing in section II. This section contains a list of column headings used in the listing, with explanations of entries and definitions of abbreviations and symbols used.

B-2. Program Listing Column Heading and Entries

Column headings and entry definitions are listed in a below. Abbreviations and symbol definitions are listed in b below.

a. Column Heading Listing

Column heading	Entry
TEST NO.	A four-digit, two-part test indication displayed on the LCU front panel TEST NUMBER indicator. The two most significant digits from 00 through 99 indicate the major test being performed. The two least significant digits from 00 through 99 indicate the minor test, the lower order of the major test being performed.
DEC1SION LEVEL	Any digit from 1 through 12. A 1 indicates that all previous tests have been successfully completed; i.e., this is the first decision level for each test. When applicable test conditions exist, a yes/no or go/no-go decision must be made. A 2 or subsequent number indicates the lower order test condition at which that decision is made.
TEST/FAULT NUMBER	The entry in this column is an alpha numeric code indicating a test or a fault location, test sequence number, and no-go flag state. A T denotes a test, and an F denotes a fault location. The number portion identifies the test sequence. Tests and related faults carry the same test sequence number. A1phabetical suffixes, N or G, are used to denote a program no-go flag or program-go-condition. The number of times a N or a G is repeated is a history of decisions made within the test sequence. A numeric suffix, if used, denotes a decision that is not based upon a program no-go flag; i.e., an in-process self-test fault. The numeric suffix and alphabetical suffix are separated by a point symbol.
SELF-TEST PROGRAM	This column contains test or fault description, LCU front panel indications, and corrective action instructions. The self-test program listing is divided into parts in accordance with the portion of the test set being tested. Each division of the listing is titled and the title enclosed in a box made up of asterisks. The test/fault description is on the same line as its test/fault number. If more than one line is required for the description, the second and subsequent lines are not indented. Signal routing information is subscripted. A description of test set operation for each test or fault is indented two spaces. The chart that follows, indented nine spaces, lists the LCU front panel TEST STATUS indications and REGISTERS display with the assemblies to be replaced for the listed indications.
REMARKS	The remarks column provides additional information for the listed test/fault data. A remarks entry in line with a test/fault test set operation description provides information about the state of the test set during the

Column heading	Entry
	operation. A remarks entry in line with an assembly replacement listing gives further information concerning the cause of a malfunction should assembly replacement fail to correct the malfunction.

b. Abbreviations and Symbol Definitions

Abbreviations or Symbol	Definitions
AANC	Instruction code
ADDR	Address
AMP	Amplifier
AND	Logic "AND" function
AREG	A register
AUTO	Automatic
AZ. C.	Computer analog signal
BCLK	B register clock
BNMJ	Instruction code
BR	Branch
BREG	B register
BRMJ	Instruction code
BRNO	Instruction code
B. T.	Bit time
BUFF	Buffer
CANT	Cannot
CC	Clock counter
CCBT	Count complete bit time
CFLG	Computer flag
CH	Check
CHAN	Channel
CIAR	Character
CIU	Control indicator unit
ClU1	Instruction code
ClU2	Instruction code
CL	Clear
CLK	Clock
CMAB	Instruction code
CMPLT	Complete
CNTR	Counter
COIMP	Computer
CP	Computer register
CREG	C register
D. A.	Computer analog signal
DC1U	Instruction code
DEF	Defines
DEIP	Instruction code
DEV	Computer analog signal
DIFF	Different
DIHR	Discrete input word-holding register
DISC	Discrete
DNCU	Instruction code
DOWD	Discrete output word
DR	Driver
DSPL	Display
DSTS	Instruction code
EA	Computer register
EB	Computer register
EIOPB	External input/output from/to B register
EIP	External input
EIPA	External input from A register
EMJT	Instruction code
EN	Enable
EOP	External output
EOPA	External output from A register
EOTF	Instruction code
EVPC	Instruction code
EXM	External memory
EXMW	External memory word
EXT	External
FF	flip-flop
FUNC	Function
GDATC	Control-indicator signal
GEN	Generate
GINT	Instruction code
GREG	G register
G. S.	Computer analog signal
GSPU	Gyro stabilized platform unit
GSP1	Instruction code
GSP3	Instruction code
NEX	Hexidecimal
HMFL	Instruction code
IBT	Instruction bit time
IN	Input
INB	Inhibit
INCM	Instruction code
INH	Inhibit
INMX	Input multiplexer
INST	Instruction
INTF	Interface
I/O	Input/Output
LACW	Instruction code
LCU	Logic conditioning unit
LD	Load
LDAB	Instruction code
LDCA	Instruction code
LDCE	Instruction code
LDC1	Instruction code
LDCM	Instruction code
LDCP I	Instruction code
LDMB	Instruction code
LDS1	Instruction code
LOC	Location
LQJD	Instruction code
L. S.	Computer analog signal
LSB	Least significant bit
LSD	Least significant digit
LSHD	Least significant hexidecimal digit
LSOD	Least significant octal digit
LVWC	Instruction code
LXMB	Instruction code
MABC	Major branch comparator
MAJ	Major
MAL	Malfunction
MATR	Major test address register
MDPL	Map display bit field
MEM	Memory
MFIL	Instruction code
MIBC	Minor branch comparator
MIN	Minor
MISC	Miscellaneous
MSB	Most significant bit

Abbreviations or Symbol	Definitions
MSD	Most significant digit
MSHD	Most significant hexidecimal digit
MSOD	Most significant octal digit
MTC	Minor test counter
MTW1	Miscellaneous test word number 1
MUX	Multiplexer
MVET	Instruction code
NET	Network
NOOP	Instruction code
NOPE	Instruction code
OCT	Octal
OP(S)	Operation(s)
OR	Logic "OR" function
PE	Parallel enable
PJB	Computer buffered EB register
PLS	Pulse
POR	Power on reset
POSFIX	Position fix
PREAMP	Preamplifier
R&C	Read and compare
RCAA	Instruction code
RCAM	Instruction code
RCAQ	Instruction code
RCCA	Instruction code
RCCE	Instruction code
RCC1	Instruction code
RCCM	Instruction code
RCCP	Instruction code
RCDW	Instruction code
RCEA	Instruction code
RCEB	Instruction code
RCEX	Instruction code
RCFM	Instruction code
RCMA	Instruction code
RCMB	Instruction code
RCM1	Instruction code
RCM2	Instruction code
RCNC	Instruction code
RCNU	Instruction code
RCPC	Instruction code
RCPJ	Instruction code
RCVVI	Instruction code
RCW1	Instruction code
RCW2	Instruction code
RCW3	Instruction code
RCXM	Instruction code
REC	Receiver
REG	Register
REPL	Replace
REQ	Required
REV	Reverse
RICP	Instruction code
RIIC	Instruction code
RIM	Register input multiplexer
RINC	Instruction code
RINM	Instruction code
RINP	Instruction code
RIOC	Instruction code
RMBA	Instruction code
ROM	Register output multiplexer
RSET	Instruction code
RS1D	Instruction code
RS10	Instruction code
SAT	Saturation
SB	Significant bit
SCU	Signal conditioning unit
SCWM	Instruction code
SDRG	Instruction code
SEG	Segment
SEL	Selected
SHT	Short
S1CP	Instruction code
S1G	Significant
S1IC	Instruction code
S1M	Simulated
S1NC	Instruction code
S1NM	Instruction code
S1NP	Instruction code
S1OC	Instruction code
SLMA	Instruction code
SLMC	Instruction code
SMFL	Instruction code
SREM	Instruction code
SRT	Start
SS1D	Instruction code
SS1O	Instruction code
ST	Self-test
STATE 2	Tape search fast reverse
STATE 3	Tape search slow forward => approach to found location
STCL	Instruction code
STOP	Instruction code
STP	Stop
STREG	Self-test register
SW	Switch
TA	Test address on tape
TAC	TACAN
TRANS	Transfer
TS	Tape search => search for tape address location
TST1	Instruction code
TST2	Instruction code
TST3	Add
UNBR	Instruction code
UNC	Unconditional
VS	Versus
WD	Word
W1	Word 1
X	Unspecified
<	Less than
>	Greater than
=	Equals
→	Data path (from to)
@	At (as a punch tape code, address character)
ε	And (as a punch tape code, end of data)
/	And/or (as a punch tape code, instruction character)
#	Number (as a punch tape code, data)
=>	Implication
Φ_D	Phase D

B-3. How to Use the Self-Test Program Listing

The following is a description of the self-test program listing as it relates to test set self-test

operation. An excerpt from the self-test program listing is described.

a. Starting with the entry in the TEST NO. column, 3651, (major test 36, minor test 51); the TEST/FAULT NUMBER column entry is test sequence 175, this number prefixed by the letter T denotes a test, the DEC1S1ON LEVEL column entry is a 1, which denotes the first decision level in test sequence 175. Arrival at decision level 1 in the program denotes that all previous tests have been successfully completed.

b. The test description listed in the SELFTEST PROGRAM column is the test instruction code RCMA and the result of the compare, a no-go flag. The test set operation is serially load the B register with hexidecimal number AFFFFFFF and read and compare the memory address (MA) lines with the A register. When the no-go flag is achieved, branch to test no. major 36 minor 58. Arrival at test no. major 36 minor 58, which is test sequence 176, denotes that test sequence 175 was successfully completed. Non-arrival at test no. major 36 minor 58 indicates a go condition exists at test sequence number 175 because the no-go flag was not achieved. Therefore, this is the first decision level.

c. If, before the test set was conditioned to achieve a no-go flag during test sequence T175, the test set in-process self-test detected a fault, the tape would stop. The test sequence number 1 75v would be prefixed by a F and suffixed by .1, indicating a fault location in test sequence 175 not based upon a self-test program no-go flag. this fault location is a decision level 2. The fault description is fault location within test sequence 175, not a programmed stop, and probable cause is RCMIA latch not reset. The LCU front panel indication is TEST STATUS TEST SET FAULT indicator lighted and REGISTERS display is 1000000. To correct malfunction, replace assembly 1A1A4A15.

d. If during test sequence T175 a no-go flag was not achieved, the program would not branch, but would step to test no. major 36 minor 53, test sequence T175.2. The test description is -test for a fault in read memory address (MA) enable (EN). The test set operation is compare the B register with the A register and branch to test no. major 36 minor 55 if a no-go is achieved.

e. If in test sequence T175.2 a no-go flag was achieved, the self-test program would branch to test no. major 36 minor 55. This is fault location F175.2.N, which is still part of test sequence 175.2. The N suffix denotes that in the previous test a no-go was achieved. The fault description is fault in RCMA instruction bit time (IBT) or latch. Test set operation is enable vertical parity check, stop tape, display the C register, and no-go light on. The LCU front panel indication is TEST STATUS NO GO indicator lighted and REGISTERS display is 1777777777. To correct malfunction, replace assemblies lA1A2A18, and/or 1A1A4A (15, 16).

f. If in test sequence T175.2 a no-go flag was not achieved and a go condition existed, the self-test program would not branch, but would step to test no. major 36 minor 54. This is fault location F175.2.G, which is still part of test sequence 175.2. The G suffix denotes that in the previous test a go condition existed. The fault description is read memory address (MA) fault. Test set operation is enable vertical parity check, stop tape, display the C register, and no-go light on. The LCU front panel indication is TEST STATUS NO GO indicator lighted and REGISTERS display is blank. To correct malfunction, replace assembly 1A1A4A15. If assembly replacement does not correct malfunction, the REMARKS column entry indicates logic term AAC017* stopped at 1 may be cause of malfunction.

g. After correction of the malfunction, the operator will re-run the self-test program to insure test sequence 175 is successfully completed.

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE LEADER 12 INCHES LONG	
			PUNCH TAPE CODES - 20 70 F8 20 20 20 20 20 20 08 F8 08 00 B8 68 F8	
			00 F8 28 F8 00 08 F8 08 00 E8 A8 B8 00 00 00 00	
			00 B8 C8 88 00 20 20 20 D0 E0 A0 F8 00 F8 28 38	
			00 F8 28 38 00 F8 88 F8 00 F8 08 08 00 E0 A0 F8	
			00 20 20 20 00 80 F8 88 00 F8 A8 F8 00 F0 20 38	
			00 E0 A0 F8 00 F8 88 F8 00 00 00 00 00 08 F8 08	
			00 E8 A8 B8 00 88 A8 F8 00 08 F8 08 00 00 00 08	
			28 F8 00 80 80 F8 00 88 A8 F8 00 E8 A8 B8 00 20	
			20 20 00 E8 A8 B8 00 08 F8 08 00 F8 00 88 88 F8	
			00 88 88 F8 00 F8 40 20 10 F8 00	LEADING HEADER
			PUNCH TAPE LEADER 72 INCHES LONG	
			**********	
			* *	
			* INITIAL CONFIDENCE TESTS (FAULT ISOLATION) *	
			* *	
			**********	
00	00		PUNCH TAPE LEADER 24 INCHES LONG	
00	01			
00	02			
00	03			
00	04			
00	05			
00	06			
00	07			
00	08			
00	09			
00	10			
00	11		PUNCH TAPE LEADER 36 INCHES LONG	
00	12			
00	13			
00	14			
00	15			
00	16			
00	17			
00	18			
00	19			
00	20			
00	21			
00	22		PUNCH TAPE LEADER 36 INCHES LONG	
00	23			
00	24			
00	25			
00	26			
00	27			
00	28			
00	29			
00	30			
00	31			
00	32			
00	33		PUNCH TAPE LEADER 36 INCHES LONG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
00 34				
00 35				
00 36				
00 37				
00 38				
00 39				
00 40				
00 41				
00 42				
00 43				
00 44			PUNCH TAPE LEADER 36 INCHES LONG	
00 45				
00 46				
00 47				
00 48				
00 49				
00 50				
00 51				
00 52				
00 53				
00 54				
00 55			PUNCH TAPE LEADER 36 INCHES LONG	
00 56				
00 57				
00 58				
00 59				
00 60				
00 61				
00 62				
00 63				
00 64				
00 65				
00 66			PUNCH TAPE LEADER 36 INCHES LONG	
00 67				
00 68				
00 69				
00 70				
00 71				
00 72				
00 73				
00 74				
00 75				
00 76				
00 77			PUNCH TAPE LEADER 36 INCHES LONG	
00 78				
00 79				
00 80				
00 81				
00 82				
00 83				
00 84				
00 85				
00 86				
00 87				

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
00 88			PUNCH TAPE LEADER 36 INCHES LONG	
00 89				
00 90				
00 91				
00 92				
00 93				
00 94				
00 95				
00 96				
00 97				
00 98				
00 99			PUNCH TAPE LEADER 36 INCHES LONG LOAD A REGISTER WITH A381F INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBF7FOFFF	INH MEM LD BREG ON CMA121, ROM->DSPL/INH MEM LD BREG ON KMA152
			DSPL = 10000000000 LOAD A REGISTER WITH 40000000 PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 11111111111 LOAD A REGISTER WITH 49249249 PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 22222222222 LOAD A REGISTER WITH 92492492 PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 33333333333 LOAD A REGISTER WITH DB6DB6DB PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 4444444444 LOAD A REGISTER WITH 24924924 PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 5555555555 LOAD A REGISTER WITH 2DB6DB6D PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 6666666666 LOAD A REGISTER WITH 36DB6DB6 PUNCH TAPE LEADER 48 INCHES LONG	
			DSPL = 7777777777 LOAD A REGISTER WITH 3FFFFFFF PUNCH TAPE LEADER 24 INCHES LONG	
13 00			PUNCH TAPE CODES - &C PUNCH TAPE LEADER 12 INCHES LONG	FORMAT ERROR: TWO ADDRESS CHAR, THEN END OF DATA CHAR

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
13 01			PUNCH TAPE CODES - /9 /8 &C	IBT TEST: INVALID INSTRUCTION = OCTAL 211
13 02			PUNCH TAPE CODES - #0 /F /6 &C	FORMAT ERROR: DATA THEN INSTRUCTION
13 03			PUNCH TAPE CODES - /F /8 &C	IBT TEST: S.T. NOOP
13 04			PUNCH TAPE CODES - /0 /8 &C /1 /C &C	IBT TEST: S.T. NOPE, SMEL + MSD
13 05			INITIATE SELF TEST MODE 3-COMPARE SELF TEST REGISTER TO A REGISTER WITH REPEAT PATTERN: 1	CHECK LOADING OF A REG VS. SELF TEST REG
13 06			ENABLE VERTICAL PARITY CHECK END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
29	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
32	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
44	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
55	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
66	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
78	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
89	00		GENERATE NO OPERATION CODE OCTAL 000 PUNCH TAPE LEADER 36 INCHES LONG	
			PUNCH TAPE CODES - @1 @1 @9 /0 /0 &C	ADDR = 91, 3ADDR = FORMAT ERROR, NOPE
			PUNCH TAPE LEADER 36 INCHES LONG END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** AUTO BRANCH TESTS **********	
	1		ENABLE LOW LEVEL ON GTC001* RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*)	AVOID ENABLE OF S.T. POSFIX TEST DURING LOAD OF S.T. REG
	1	T1	TEST UNC. BRANCH WITHIN MAJOR TO MINOR 1 LOAD A REGISTER WITH 00102	BRANCH ADDR SET UP FOR VARIABLE BRANCH
00 00	2	F10.3 F11.2	FAULT LOCATION WITHIN TEST T1 (NOT A PROGRAMMED STOP)	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES TEST SET FAULT / 2100000000001 / PROCEED PER PARAGRAPH 3-12D — STATE 2 & SEL ADDR > TA TEST SET FAULT / 1000000000001 / PROCEED PER PARAGRAPH 3-12D — STATE 3 & SEL ADDR < TA TEST SET FAULT / 2200000000001 / 1A1A1A(25,26) — THIS FAULT LOC IS AT 02 00 ON TAPE, BUT APPEARS AS 00 00 ON FRONT PANEL	
		T1(CONT.)	BRANCH TO ADDRESS LOCATION IN A REGISTER	VARIABLE BRANCH, PART OF T1: IF FROM — GO TO 1) INITIAL CONF. — MINOR 1 2) MAJ 12 MIN 3 — MINOR 4 3) MAJ 1 MIN 80 — MINOR 12
	2	T1.11	TEST OF UNC. BRANCH OUT OF MAJOR WITH NO BRANCH MODE IN T1 BRANCH TO MAJOR 2 MINOR 19	
	3	F1.11.1	TEST OF DIFF. SCU INST. & FAULT LOCATION READ & COMPARE PJB LINES WITH 5555555 INITIATE SELF TEST MODE 3-COMPARE SELF TEST REGISTER TO A REGISTER WITH REPEAT PATTERN: 1 LOAD A REGISTER WITH 55555555 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT / DISPLAY: 2000 / REPLACE ASSEMBLIES: 2A1A1A02, 2A1A2A09	NO LOAD OF B REG WITH RCPJ
			INDICATORS: TEST SET FAULT / DISPLAY: 10000 / REPLACE ASSEMBLIES: 1A1A1A09	NO "END OF DATA" TO SCU
			INDICATORS: TEST SET FAULT / DISPLAY: 1000 / REPLACE ASSEMBLIES: 2A1A1A02	NO "END OF DATA" TO 2A1A2
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
			INDICATORS: NO GO / DISPLAY: 25252525252 / REPLACE ASSEMBLIES: 1A1A1A(4,6), 2A1A2A(8,9,10)	SHORT DATA ACTIVE
			INDICATORS: NO GO / DISPLAY: 37252525252 / REPLACE ASSEMBLIES: 1A1A1A14, 2A1A2A(6,12)	NO BRANCH MODE, RCPJ OK
00 01	1	T2	TEST OF BNMJ WITHOUT NO-GO PUNCH TAPE CODES - /F /7 #9 #2 #0 &C BRANCH TO MAJOR 00 MINOR 28 ON NO-GO ENABLE VERTICAL PARITY CHECK	INCM 029; GO TO MIN 29 IF BRMJ NOT RESET
	1	T3	TEST OF BRANCH ON "NO-GO" WITH "NO-GO". TEST SKIP MINORS LOAD A REGISTER WITH 07900 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7E4F7F PUNCH TAPE CODES - /5 /1 #2 #0 #7 #0 &C	IF XPF362 S@1 GO TO 79 NOT 7 ROM->DSPL, CLK RUN TAPE STP, SIM NO-GO, ROM->RIM BNMJ 2 7 - MAJ 2 IS ADDED TO TEST BRANCH WITHIN MAJ FUNC
	2	T3.6	TEST BNMJ WITH "NO-GO FLAG" SET UP SERIALLY LOAD THE B REGISTER WITH A COMPARE THE B REGISTER TO AF BRANCH TO MAJOR 00 MINOR 54 ON NO-GO	C = 0F000000
	3	T3.6.G	CHECK OTHER BRANCH ON NO-GO INST, BRNO BRANCH TO MAJOR 2 MINOR 74 ON NO-GO	
	4	T3.6.G.2	TEST IF BNMJ LATCH IS SET LOAD A REGISTER WITH 0 BRANCH TO MAJOR 2 MINOR 22	
	5	F3.6.G.2.3	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-13	
00 02	2	F3.4	CANT SKIP MINORS ENABLE VERTICAL PARITY CHECK INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM->DSPL
			INDICATORS: NONE / DISPLAY: 34XXXXXX / REPLACE ASSEMBLIES: 2A1A2A(9,10,12)	
00 03	2	F1.3 F3.2	FAULT IN BIT OF BRANCH ADDR FIELD TO MINOR COMPARATOR, BIT 22 OR BIT 23 ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00502 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM->DSPL
			INDICATORS: NONE / DISPLAY: 4XXXXXX / REPLACE ASSEMBLIES: 2A1A1A(23,24)	BIT 23 OF ROM INACTIVE
			INDICATORS: NONE / DISPLAY: 34XXXXXX / REPLACE ASSEMBLIES: 2A1A1A(12,23,24)	BIT 22 OF A REG OR ROM ACTIVE
			INDICATORS: NONE / DISPLAY: 24XXXXXX / REPLACE ASSEMBLIES: 1A1A1A01, 2A1A2A11	6TH OR 7TH SIG BIT OF MIRC OR MTC
00 04	1		MANUAL MODE PROGRAM LOCATION- BRANCH TO VERIFY TESTS "VERIFY ENTIRE TAPE" SECTION DEFINE EIP DATA FIELD AS PRESENT CONTENTS OF A REGISTER BRANCH TO MAJOR 00 MINOR 15 BRANCH TO MAJOR 00 MINOR 15	FROM VARIABLE BRANCH MIN 00 THIS INST WILL BE BRANCHED OVER BUT DEIP LATCH WILL RESET BR ADDR IN AREG => BR TO MIN 100
00 05	2	F1.4 F3.3	FAULT IN BIT OF BRANCH ADDR. FIELD TO MINOR COMPARATOR, BIT 22 OR BIT 23 ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00302 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM->DSPL

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NONE / 4XXXXXX / 2A1A1A(23,24)	BIT 22 OF ROM INACTIVE
			NONE / 34XXXXXX / 2A1A1A(12,23,24)	BIT 23 OF A REG OR ROM ACTIVE
			NONE / 14XXXXXX / 1A1A1A01 2A1A2A11	6SB OR 7SB OF MIBC, OR MTC
00 06	2	F22.1	CANT BRANCH FORWARD OUT OF MAJOR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / BLANK / PROCEED PER PARAGRAPH 3-12D	
00 07	1	T4	CHECK RESET OF TST2 PUNCH TAPE CODES - /F /7 #9 #2 #0 &C	INCM 029; GO TO MIN 29 IF BNMJ NOT RESET
00 08			SERIALLY LOAD THE B REGISTER WITH A30F0F0F	SET UP ADDR TO BRANCH TO IF TST2 FF KYR702 NOT RESET
	2	F4.2	FAULT LOC WITHIN TEST T4, NOT A PROGRAMMED STOP- IN-PROCESS FAULT DETECTED ASSOCIATED WITH LDAB FUNC	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			TEST SET FAULT / 40000012A1A1A(6,25)	
			TEST SET FAULT / 20000012A1A1A(2,5,6,8,10,13)	
			TEST SET FAULT / 10000 / PROCEED PER PARAGRAPH 3-12D	
	1	T4(CONT)	PUNCH TAPE CODES - /5 /1 #F #F #F #4 #F #F #0 #0 #4 #2 &C	BNMJ 42 IF KYR702* @ 1. IF KYR702* @ 0,DATA->STREG = SIM NO-GO, BRANCH TO PREVIOUS ADDR IN AREG
	1	T5	TEST FOR SELF TEST REG NOT RESET INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. BRANCH TO MAJOR 00 MINOR 62 ON NO-GO	
	1	T6	CHECK RESET OF LCU SECTION OF STREG ENABLE CONTROLLED TIMING PULSE INTERVAL 1 ON GTC001*	
	2	F6.1	FAULT LOC WITHIN TEST T6- SELF TEST REG NOT RESET OR CLK COUNTER ERROR	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NONE; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A(20,21), 1A1A3A23	KYR023 FF NOT RESET
			INDICATORS: TEST SET FAULT; DISPLAY: 20000001; REPLACE ASSEMBLIES: 1A1A3A(6,7,8,9,10)	CLK COUNTER ERROR
	1	T7	CHECK RESET OF TST1 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F3FFF4FFF BRANCH TO MAJOR 00 MINOR 10 ON NO-GO	SIM NO GO -SHOULD BE PULS
	1	T8	TEST OF 2ND & 3RD SIG BITS OF MTC TO MIBC OR AT MIBC SERIALLY LOAD THE B REGISTER WITH A30F0F0F LOAD A REGISTER WITH 10000000 BRANCH TO MAJOR 00 MINOR 60	
00 09	2	F1.5	SSB OF BRANCH ADDR FIELD ACTIVE ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00102 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F8F7F0FFF STOP TAPE	ROM->RIM
			INDICATORS: NONE; DISPLAY: 4XXXXXX; REPLACE ASSEMBLIES: 1A1A1A01, 2A1A2A11	SSB OF MTC OR MIBC
			INDICATORS: NONE; DISPLAY: 44XXXXXX; REPLACE ASSEMBLIES: 2A1A1A(12,23,24)	BIT 24 OF A REG OR ROM ACTIVE
00 10	2	F7.1	FAULT IN TST1 RESET OR SELF TEST REG PE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A3A(14,15,16)	
00 11	2	F1.6	4SB OF BRANCH ADDR FIELD ACTIVE ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00102 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F8F7F0FFF STOP TAPE	ROM->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NONE — DISPLAY: 4XXXXXX — REPLACE ASSEMBLIES: 1A1A1A11, 2A1A2A10	4SB OF MTC OR MIBC
			INDICATORS: NONE — DISPLAY: 104XXXXXX — REPLACE ASSEMBLIES: 2A1A1A(12,21)	BIT 25 OF A REG OR ROM ACTIVE
00 12	1		MANUAL MODE PROGRAM LOCATION- BRANCH BACK TO MANUAL MEMORY CONTROL TESTS MAJ 12 BRANCH TO MAJOR 2 MINOR 10	FROM VARIABLE BRANCH MIN 00
00 13 00 14	1	T15	TEST SIOC RESET OF TST2 AND RIOC RESET OF SIOC SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) BRANCH TO MAJOR 00 MINOR 86 ON NO-GO INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4FFF BRANCH TO MAJOR 00 MINOR 72 ON NO-GO BRANCH TO MAJOR 00 MINOR 97	RESET TST2 USED IN T13 RESET SIOC TEST IF TST2(SIM NO-GO) IS RESET SIM NO-GO IF SIOC NOT RESET GO TO MIN 97 INSTEAD OF MIN 72 = T14
00 15			SPARE	
00 16 00 17	1		NOT A TEST LOCATION- BRANCH HERE FROM MIN 32 IF T18 PASSED BRANCH TO MAJOR 00 MINOR 25	GO TO T19
00 18	2	F9.1	FAULT IN MSB OF MTC TO MIBC, OR IN MSB OF MIBC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A25, 2A1A2A(8,10)	
00 19	3	F1.11.3	OPEN INPUT AT GATE BPJ031, "OR" OF BRANCHES ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A12	
00 20	2	F8.1	FAULT IN 2SB OF MTC TO MIBC, OR IN 2SB OF MIBC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A11, 2A1A2A10	
00 21	2	F1.7	3SB OF BRANCH ADDR FIELD ACTIVE ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00102 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM -> DSPL
			INDICATORS: NONE — DISPLAY: 4XXXXXX — REPLACE ASSEMBLIES: 1A1A1A11, 2A1A2A10	3SB OF MTC OR MIBC
			INDICATORS: NONE — DISPLAY: 204XXXXXX — REPLACE ASSEMBLIES: 2A1A1A(12,21)	BIT 25 OF A REG OR ROM ACTIVE
00 22	5	F3.6.6.2.1	FAULT IN BRANCH ON NO-GO "OR" FUNCTION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1700000000 — REPLACE ASSEMBLIES: 2A1A2A(6,12)	
00 23 00 24	1		NOT A TEST LOCATION- BRANCH HERE FROM MIN 26 IF T18 PASSED BRANCH TO MAJOR 00 MINOR 52	GO TO T19
00 25 00 26	1	T19	TEST 6SB OF MIBC, ENABLE OF STATE 2 BRANCH TO MAJOR 00 MINOR 23	
00 27	2	F19.1	6SB OF MIBC CAN NOT ENABLE STATE 2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A11	BPJ261* SA1
00 28	2	T2.2	CHECK STATE OF "NO-GO" FLAG, ATTEMPT RESET SERIALLY LOAD THE B REGISTER WITH AAAAAAAA COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 00 MINOR 49 ON NO-GO	
	3	F2.2.6	NO-GO FLAG WAS RESET, BUT INITIALLY WAS SET ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A1A04 OR HIGHER LEVEL OF MAINTENANCE	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A2A17	
00 29	2	F2.1 F4.1 F11.1 F14.1	BRANCH LATCH NOT RESET PUNCH TAPE CODES - /F /7 /1 /0 &C ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	3 INST CHAR = FORMAT ERROR, 1ST 2 = INCM, 2ND 2 = RESC, 4TH CLEARS VERTICAL PARITY
			INDICATORS: TEST SET FAULT — DISPLAY: 4000000000 — REPLACE ASSEMBLIES: 2A1A2A06 OR HIGHER LEVEL OF MAINTENANCE	APJ045*
00 30	2	F4.4	TST2 FF "KYR702" NOT RESET ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A15	
00 31 00 32	1	T18	TEST BSB OF MIBC, ENABLE OF STATE 2 BRANCH TO MAJOR 00 MINOR 16	
00 33	3	F10.2N	UNBR IBT OR LATCH INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A(6,12)	
00 34 00 35	1		NOT A TEST LOCATION- BRANCH HERE FROM MIN 76 IF T11 PASSED ENABLE VERTICAL PARITY CHECK BRANCH TO MAJOR 00 MINOR 82	GO TO T12
00 36	2	F18.1	BSB OF MIBC CAN NOT ENABLE STATE 2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A2A10	BPJ231* S@1
00 37 00 38	1	T17	TEST 5SB OF MIBC, ENABLE OF STATE 2 BRANCH TO MAJOR 00 MINOR 31	
00 39	2	F17.1	5SB OF MIBC CAN NOT ENABLE STATE 2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A2A11	BPJ251* S@1
00 40	2	F8.2	2SB OF MTC TO MIBC OR IN 2SB OF MIBC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: (1A1A1A11 / 2A1A2A10)	
00 41	2	F1.8	2SB OF BRANCH ADDR FIELD ACTIVE ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH 00102 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM -> DSPL
			INDICATORS: NONE; DISPLAY: 4XXXXXX; REPLACE ASSEMBLIES: 1A1A1A11	2SB OF MTC OR MIBC
			INDICATORS: NONE; DISPLAY: 404XXXXXX; REPLACE ASSEMBLIES: (2A1A1A10 / 2A1A1A(12,21))	BIT 27 OF A REG OR ROM ACTIVE
00 42 00 43	2	T4.3	TEST RESET OF TST2 WITH COMPARE (RCEB) READ & COMPARE THE EB LINES WITH A0000000 BRANCH TO MAJOR 00 MINOR 44 ON NO-GO	CHECK IF RCEB RESET NO-GO OF TST2
	3	F4.3.6	FAULT IN LDAB LATCH , IBT, INPUT TO "CAR036" OR INST DECODE MATRIX ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /0 /0 &C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	INVALID INST = 0/1/5 OCTAL-TEST DECODE MATRIX

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT / NO GO — DISPLAY: 40 / BLANK — REPLACE ASSEMBLIES: 2A1A1A(1,2) / 2A1A2A02 / PROCEED PER PARAGRAPH 3-120	FAULT IN INST DECODE MATRIX
00 44	3	T4.3.N	RESET TST2 WITH SIOC	
00 45			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	RESET SIOC
			BRANCH TO MAJOR 00 MINOR 46 ON NO-GO	
	4	T4.3.NG	CHECK FOR "RESET LATCHES" ACTIVE, CAR036 S@0, OR AYR714* INACTIVE	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4FFF	SFM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABA?00	EA ADDR = 350
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABA000	I/O REQ ACTIVE
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000	
			BRANCH TO MAJOR 00 MINOR 63 ON NO-GO	
	5	F4.3.NGG	FAULT IN "AANC CMAB LOAB" RESET OF TST2, OR "CAR036"	
			ENABLE VERTICAL PARITY CHECK	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF07FF	B -> ROM
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 177777777 — REPLACE ASSEMBLIES: 2A1A1A(1,2) / 2A1A3A15	AYR714* S@1
			INDICATORS: NO GO — DISPLAY: 125777777777 — REPLACE ASSEMBLIES: 2A1A1A01	CAR036 S@0
00 46	4	T4.3.NN	ISOLATE FAULT WITHIN SELF TEST CONTROL, TST1 RESET OF SELF TEST REG	
			INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG.	
			BRANCH TO MAJOR 00 MINOR 64 ON NO-GO	
	5	F4.3.NNG	FAULT IN RESET OF TST2	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A(15,16)	
00 47	1		NOT A TEST LOCATION- BRANCH HERE FROM MIN 53 IF /20 PASSED	
00 48			BRANCH TO MAJOR 00 MINOR 66	GO TO T21
00 49	3	T2.2.N	CHECK OTHER BRANCH ON NO-GO, BSNO	
			BRANCH TO MAJOR 0 MINOR 89 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	4	F2.2.NG	NO-GO INPUT AT INST DECODE GATE "CAD025" OPEN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A01	
00 50			SPARE	
00 51			SPARE	
00 52	1	T20	TEST 4SB OF MIBC, ENABLE STATE 2	
00 53			BRANCH TO MAJOR 00 MINOR 47	
00 54	3	T3.6.N	CHECK FOR ACTIVE MEMORY CONTROL	
00 55			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFF10FFF	ALL MEMORY LOAD & REG ACTIVE
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	RESET SIOC
			COMPARE THE B REGISTER TO THE A REGISTER	
			BRANCH TO MAJOR 2 MINOR 4 ON NO-GO	GO TO (00)T3.6.NN (MAJ 19 MIN 3) VIA MAJ 2 MIN 4
			BRANCH TO MAJOR 00 MINOR 58	
00 56			SPARE	
00 57	2	F20.1	4SB OF MIBC INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A11, 2A1A2A10	CPU241* S01
00 58	4	T3.6.NG	CHECK STATE OF GTC001*	
00 59			READ & COMPARE MISCELLANEOUS WORD 1 WITH A00000C0 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 00 MINOR 68 ON NO-GO	
	5	T3.6.NGG	TEST RESET OF GTC001* FOUND ACTIVE IN T3.6.NG, RESET WITH RCNC SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE CONTROLLED TIMING PULSE INTERVAL TO CONDITIONALLY ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A0 LOGICALLY 'AND' C REGISTER AND A00000C0 - RESULT IN B & C REGISTER BRANCH TO MAJOR 00 MINOR 92 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	6	F3.6.NGGG	PROBLEM IN RESET OF CLOCK CONTROL FF USING STCL ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A18; 1A1A3A(12,13)	
00 60	1	T9	TEST MSB, 4SB, 5SB OF BRANCH ADDR FIELD FOR INACTIVE, 8SB FOR ACTIVE LOAD A REGISTER WITH 80	SET UP 8 OF 98 IN BRANCH ADDR TO CHECK FOR PASS THRU MIN 60
00 61			LOAD A REGISTER WITH 09 BRANCH TO ADDRESS LOCATION IN A REGISTER	SET UP 9 OF 98 IN BRANCH ADDR- WILL = 90 IF MISS MIN 60
00 62	2	F5.N	FAULT IN RESET OF SELF TEST REG ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH A30F0F0F STOP TAPE	
			INDICATORS: NONE — DISPLAY: 12430360741712A1A3A(15,16)	GYR707 S@0 OR IYR717* S@1
			INDICATORS: NONE — DISPLAY: BLANK — 12A1A1A(4,7)	GYR777* S@1 OR SEG OF ST REG
00 63	5	F4.1.NGN	"RESET LATCHES" ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — 12A1A1A(1,6,17)	GAR021 S@0
00 64	5	F4.1.NNN	FAULT IN RESET OF SELF TEST REG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — 12A1A3A15	MULTIPLE FAULT
00 65	1	T22	TEST OF BRANCH FORWARD OUT OF MAJ, SKIP MAJ 1, GO TO MAJ 21 VIA MAJ 2 MIN 6 ENABLE VERTICAL PARITY CHECK BRANCH TO MAJOR 2 MINOR 6	
00 66	1	T21	TEST 1ST OF MIDC, ENABLE STATE 2	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 17000000000 — REPLACE ASSEMBLIES: 2A1A2A06	AAT091 S@0
00 75	1	T11	TEST BRANCH IN STATE 2 WITHIN MAJ PUNCH TAPE CODES - /F /7 #9 #2 #0 &C	INCM 029, GO TO MIN 29 IF UNBR NOT RESET
00 76			BRANCH TO MAJOR 00 MINOR 34	
00 77	2	F16.1	2SB CAN NOT ENABLE STATE 2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A10	BPJ221* S@1
00 78	3	T8.3.1	PARTIAL BREG -> ROM ENABLE ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A1A19	
00 79	2	F3.7	END OF DATA ALWAYS ACTIVE AT BRANCH CONTROL, OR KY3722 S@0 ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF STOP TAPE	ROM->DSPL
			INDICATORS: NONE — DISPLAY: 240000000000 — REPLACE ASSEMBLIES: 2A1A1A02	
			INDICATORS: NONE — DISPLAY: 74400XXXX — REPLACE ASSEMBLIES: 2A1A2A09	
			INDICATORS: NONE — DISPLAY: 74400XXXX — REPLACE ASSEMBLIES: 2A1A3A(15,16)	KY3722 S@0
00 80	3	T3.1.N	CONFIRM FAULT IN BRANCH SHORT DATA EN SERIALLY LOAD THE B REGISTER FROM THE A REGISTER COMPARE THE B REGISTER TO A80AAAAA LOAD A REGISTER WITH 08400 BRANCH TO ADDRESS LOCATION IN A REGISTER	
	4	F3.1.NG	FAULT IN BRANCH SHORT DATA EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | 17000000001 2A1A2A06	AAT091 S@0
00 75	1	T11	TEST BRANCH IN STATE 2 WITHIN MAJ PUNCH TAPE CODES - /F /7 #9 #2 #0 &C	INCM 029, GO TO MIN 29 IF UNBR NOT RESET
00 76			BRANCH TO MAJOR 00 MINOR 34	
00 77	2	F16.1	2SB CAN NOT ENABLE STATE 2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK | 2A1A2A10	BPJ221* S@1
00 78	3	T8.3.1	PARTIAL BREG -> ROM ENABLE ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | XXXXXXXXXXXX 2A1A1A19	
00 79	2	F3.7	END OF DATA ALWAYS ACTIVE AT BRANCH CONTROL, OR KYR722 S@0 ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBF7F0FFF STOP TAPE	ROM->DSPL
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NONE | 240000000001 2A1A1A02 | 2A1A2A09 NONE | 74400XXXX 2A1A3A(15,16)	KYR722 S@0
00 80	3	T3.1.N	CONFIRM FAULT IN BRANCH SHORT DATA EN SERIALLY LOAD THE B REGISTER FROM THE A REGISTER COMPARE THE B REGISTER TO A80AAAAA LOAD A REGISTER WITH 08400 BRANCH TO ADDRESS LOCATION IN A REGISTER	
	4	F3.1.NG	FAULT IN BRANCH SHORT DATA EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	PRECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A1A29
		2A1A2A10

00 81 2 F1.9

MSB OF BRANCH ADDR FIELD ACTIVE
ENABLE VERTICAL PARITY CHECK
LOAD A REGISTER WITH 00102
INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF/F0FFF — ROM->DSPL
STOP TAPE

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NONE	4XXXXXX	1A1A1A25	MSB MIC->MIBC OR AT MIBC
		2A1A1A10	
NONE	1004XXXXXX	2A1A1A(12,21)	BIT 28 OF A REG OR ROM ACTIVE

00 82 1 T12

TEST OF BRANCH ON NO-GO OUT OF MAJ WITHOUT NO-GO
BRANCH TO MAJOR 0 MINOR 85 ON NO-GO

1 T13

TEST OF BRANCH OUT OF MAJ ON NO-GO WITH NO-GO
INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4F7F — SIM NO-GO, POSFIX PULSE CHECK
BRANCH TO MAJOR 0 MINOR 83 ON NO-GO

2 F13.1

FAULT IN BRNO TBT OR LATCH, OR TST2
ENABLE VERTICAL PARITY CHECK
SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*)
ENABLE CONTROLLED TIMING PULSE INTERVAL 20 ON GTC001*
STOP TAPE

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NONE	BLANK	2A1A3A(15,16)	KYR722 NOT RESET
NO GO	BLANK	2A1A2A(1,6)	BRNO TBT OR LATCH

00 83 1 T14

TEST MSB OF MIBC, ENABLE STATE 2
PUNCH TAPE CODES - /F /7 #9 #2 #0 &C — INCM 029, GO TO MIN 29 IF BRNO NOT RESET
BRANCH TO MAJOR 00 MINOR 13

00 84 4 F3.1.NN

NOT A NORMAL FAULT LOCATION
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-13	
00 85	2	F12.1	NO GO INPUT TO B?NO IBT DECODE GATE "CA0024" OPEN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A01	
00 86	2	T15.1	CHECK SIOC->GTC010*->MTW1 SET THE I/O COMPLETE FLAG (GTC010*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A0080000 - RESULT IN B & C REGISTER BRANCH TO MAJOR 00 MINOR 87 ON NO-GO	MASK ALL BUT GTC010*->OUTOP?
	3	F15.1.G	FAULT IN SIOC RESET OF TST2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A12	CEC499* Sal
			REPLACE ASSEMBLIES: 2A1A3A(15,3,4,5,7)	
00 87	3	F15.1.N	SIOC IBT OR GTC010* DRIVER, INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000001 — REPLACE ASSEMBLIES: 2A1A2A(2,12,17,18)	
00 88	2	F9.2	4SB OF MIBC OR MTC TO MIBC INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A11	
			REPLACE ASSEMBLIES: 2A1A2A10	
00 89	4	F2.2.NN	CANT RESET NO-GO FLAG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A1A07
		2A1A2A06

00 90 2 F9.3

5SB OF MIBC OR MTC TO MIBC INACTIVE. OR 8SB ACTIVE
ENABLE VERTICAL PARITY CHECK
INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBF7FOFFF — ROM->DSPL
STOP TAPE

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NONE	114000XXXX	1A1A1A01	
		2A1A2A11	
NONE	110140XXXX	1A1A1A01	
		2A1A2A11	
NONE	114604000000	2A1A1A(12,17)	IRA084* S@1

00 91 6 F3.6.NGNN

FAULT IN SCU LSD INST DECODE
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	20000000	2A1A2A(1,2)

00 92 6 F3.6.NGGN

CANT RESET CLOCK CONTROL FF
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	30011	A1A3A(2,6,7,12,13)

00 93 2 F14.2

MSB OF MIBC CANT ENABLE STATE 2
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	BLANK	2A1A2A10	BPJ211* S@1

00 94 3 T3.1.G
00 95

CONFIRM FAULT IN SHORT DATA EN AT 2A1A1
SERIALLY LOAD THE B REGISTER FROM THE A REGISTER
COMPARE THE B REGISTER TO A94AAAAA
LOAD A REGISTER WITH 09600
BRANCH TO ADDRESS LOCATION IN A REGISTER

4 F3.1.GG

FAULT IN SHORT DATA EN AT 2A1A1
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO-GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A1A1(12,17,28)	
00 96	4	F3.1.GN	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO-GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-13	
00 97	2	F15.2	FAULT IN RIOC LOGIC OR INST DECODE MATRIX ENABLE VERTICAL PARITY CHECK READ & COMPARE PJB LINES WITH A0000000 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	C REG = OFFFFFFF SHOULD DSPL ONES IN C REG
			INDICATORS: NO-GO — DISPLAY: 17777777772 — REPLACE ASSEMBLIES: 2A1A2A1(12,17)	FAULT IN RIOC LOGIC
			INDICATORS: NO-GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	FAULT IN INST DECODE MATRIX
00 98 00 99	1	T10	TEST OF UNCONDITIONAL BRANCH OUT OF MAJ TO SAME MAJ- ENABLE STATE 2 BRANCH TO MAJOR 0 MINOR 75 ON NO-GO	
	2	T10.2	TEST OTHER BRANCH OUT OF MAJ, BRNO INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF BRANCH TO MAJOR 0 MINOR 33 ON NO-GO	SIM NO-GO
	3	F10.2.G	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO-GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-13	
00 00			MINOR 100- BR LOGIC WILL INTERPRET AS MINOR 00=> RESET BR MODE OF MINOR 4 SERIALLY LOAD THE B REGISTER FROM THE A REGISTER LOAD A REGISTER WITH 066	RESET DEIP LATCH SET UP BR ADDR FOR MAJ 01 MIN 01
			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
*****************************************************************************************************
*                                                                                                   *
*                                          MANUAL MODE SECTION                                      *
*                                                                                                   *
*                  MAJORS 1 THRU 18 -- REFER TO PARAGRAPH 13.3 FOR MANUAL TEST PROCEEDURE           *
*                                                                                                   *
*****************************************************************************************************
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*****************************************************************************************************
*                                                                                                   *
* TESTS IN MAJOR 01 INCLUDE: INSTRUCTION DECODE, DISPLAY, BRANCH, PANEL INDICATOR LOGIC, TAPE CONTROL, *
* AND MEMORY VERIFY ENTIRE TAPE.                                                                    *
*                                                                                                   *
*                                                                                                   *
*                                THERE ARE THREE ADDR 01 WITHIN THIS MAJOR                          *
*                                                                                                   *
*                                                                                                   *
*                    THERE ARE VARIOUS AUTO SECTION FAULT LOCATIONS WITHIN THIS MAJOR                *
*                                                                                                   *
*****************************************************************************************************
```

01 00 2 (00)F22.3 FIRST ADDR 01

AUTO SECTION FAULT LOC- 7SB OF MABC CAUSES > INSTEAD OF =

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
TEST SET FAULT	1210000000001	A1A1A1(11,14,21,22,23)	
TEST SET FAULT	1 10000000001	A1A1A1(11,12,13,14,15,18)	
NO GO	1	BLANK 12A1A1A19	
NONE	1	BLANK 12A1A2A1(9,11,17)	KPJ121

PUNCH TAPE LEADER 12 INCHES LONG
BRANCH TO ADDRESS LOCATION IN A REGISTER

01 01 2 (00)F1.10 AUTO SECTION FAULT LOC- ALWAYS START BRANCH IN STATE 2 OR BSB OF BRANCH ADDR FIELD INACTIVE- ALSO MANUAL SECTION TEST

ENABLE VERTICAL PARITY CHECK
PUNCH TAPE CODES - /8 /8 &C

INVALID INST = 2/1/0 DET

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES TEST SET FAULT / 4000004012A1A2A(8,9,10,11)	
01 02	2	(02)F30.1	AUTO SECTION FAULT LOCATION- 3SB OF MAJOR ADDR FIELD TO MABC INACTIVE- ALSO MANUAL SECTION TEST ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /9 /8 &C	INVALID INST = 2/1/1
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES TEST SET FAULT / 4000004011A1A1A(21,22,23)	
01 03			PUNCH TAPE CODES - /A /8 &C	INVALID INST = 2/1/2 OCT
01 04			PUNCH TAPE CODES - /B /8 &C	INVALID INST = 2/1/3 OCT
01 05			PUNCH TAPE CODES - /C /8 &C	INVALID INST = 2/1/4 OCT
01 06	2	(00)F22.2	AUTO SECTION FAULT LOC- CAN NOT BRANCH OVER MAJORS- ALSO MANUAL SECTION TEST ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /D /8 &C	INVALID INST = 2/1/5 OCT
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES TEST SET FAULT / 4000004011A1A1A(11,14,21,23)	
01 07			PUNCH TAPE CODES - /F /8 &C	INVALID INST = 2/1/7 OCT
01 08			PUNCH TAPE CODES - /6 /8 &C	INVALID INST = 2/0/6 OCT
01 09			PUNCH TAPE CODES - /6 /9 &C	INVALID INST = 2/2/6 OCT
01 10			PUNCH TAPE CODES - /E /9 &C	INVALID INST = 2/3/6 OCT
01 11			PUNCH TAPE CODES - /6 /C &C	INVALID INST = 3/0/6 OCT
01 12			PUNCH TAPE CODES - /E /C &C	INVALID INST = 3/1/6 OCT
01 13	2	(00)F14.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "MTC > A"- ALSO MANUAL SECTION TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /6 /D &C	INVALID INST = 3/2/6 OCT
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 4000000012A1A2A(9,10)	
01 14			PUNCH TAPE CODES - /E /D &C	INVALID INST = 3/3/6 OCT
01 15			PUNCH TAPE CODES - /6 /E &C	INVALID INST = 3/4/6 OCT
01 16	2	(00)F18.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "CPJ215"- ALSO MANUAL SECTION TEST ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /E /E &C	INVALID INST = 3/5/6 OCT
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 4000000012A1A2A10	
01 17			PUNCH TAPE CODES - /6 /F &C	INVALID INST = 3/6/6 OCT
01 18			PUNCH TAPE CODES - /E /F &C	INVALID INST = 3/7/6 OCT
01 19			PUNCH TAPE CODES - /9 /0 &C	INVALID INST = 0/1/1 OCT
01 20			PUNCH TAPE CODES - /D /0 &C	INVALID INST = 0/1/5 OCT
01 21			PUNCH TAPE CODES - /0 /2 &C	INVALID INST = 0/4/0 OCT
01 22			DEFINE SELF TEST TAPE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 23	2	(00)F19.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "CPJ225"- ALSO MANUAL SECTION TEST ENABLE VERTICAL PARITY CHECK ENABLE MODE SWITCH TEST STOP TAPE	

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|TEST|DECISION | TEST/FAULT |                          SELF-TEST PROGRAM                           |              REMARKS              |
|_NO.|__LEVEL__|___NUMBER___|______________________________________________________________________|___________________________________|


                                        ---------------------------------------------------------------
                                        |__INDICATORS___|_DISPLAY___|________REPLACE_ASSEMBLIES________|
                                        |NONE___________|_8888008888|2A1A2A11__________________________|

                                BRANCH TO MAJOR 01 MINOR 24
                                STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON


01 24                           STOP TAPE
                                BRANCH TO MAJOR 01 MINOR 25
                                STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON


01 25                           STOP TAPE


01 26                           SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                  (GTC003*)
                                ENABLE LOW LEVEL ON GTC001*                                          AVOID ENABLE OF S.T. POSFIX
                                                                                                      TEST DURING LOAD OF S.T.
                                                                                                      REG

                                PUNCH TAPE CODES - /3 /4 #0 #0 #0 #0 #0 #0 #0 #0 #0 #0 &C            SHOULD CAUSE SELF TEST REG
                                                                                                      ERROR


01 27                                                                                                TST3 (1022 ONES) SHOULD
                                                                                                      CAUSE PROCEED ERROR
                                PUNCH TAPE CODES - /3 /4 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
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                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
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                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                                   #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
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```
|TEST|DECISION | TEST/FAULT  |                           SELF-TEST PROGRAM                                  |          REMARKS           |
|_NO.|__LEVEL__|___NUMBER____|______________________________________________________________________________|____________________________|

                                  #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                  #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
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                                  #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1 #1
                                  &C

                              INITIATE SELF TEST MODE 3-COMPARE SELF TEST REGISTER TO A REGISTER
                                WITH REPEAT PATTERN: 5                                            SHOULD NOT CAUSE SELF TEST
                                                                                                   REG ERROR

                              INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4FFF   SIM NO-GO
                              BRANCH TO MAJOR 01 MINOR 28 ON NO-GO
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

01 28                         STOP TAPE
                              BRANCH TO MAJOR 01 MINOR 35 ON NO-GO
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
01 29			RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) STOP TAPE	
01 30			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) DEFINE CIU TEST TAPE	
01 31	2	(00)F17.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "MTC>A"- ALSO MANUAL SECTION TEST DEFINE NCU TEST TAPE	
			INDICATORS: SELF TEST FLASH; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A2A(9,11)	
			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	AVOID ENABLE OF S.T. POSITN TEST DURING LOAD OF S.T. REG
01 01			BRANCH TO MAJOR 01 MINOR 1 PUNCH TAPE CODES - /F /7 &C	MINOR 1 IF POR IN MIN 31, OTHERWISE MINOR 32
01 02				MINOR 33 IF NO POR IN MIN 31
			LOAD A REGISTER WITH A12	SET BRANCH ADDR FOR MAJ 1 VARIABLE BRANCH
01 00			GENERATE NO OPERATION CODE OCTAL 016 PUNCH TAPE LEADER 12 INCHES LONG	2ND ADDR 01
01 00				3RD ADDR 01
			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	AVOID ENABLE OF S.T. POSITN TEST DURING LOAD OF S.T. REG
			PUNCH TAPE LEADER 12 INCHES LONG	
01 01			BRANCH TO ADDRESS LOCATION IN A REGISTER	VARIABLE BRANCH, MAJ 1

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				IF FROM GO TO
				1) FIRST ADDR 01 MINOR 12
				2) END OF MAJ 01 MINOR 1F
01 02			SPARE	
01 03			SPARE	
01 04			SPARE	
01 05			SPARE	
01 06			SPARE	
01 07			SPARE	
01 08			SPARE	
01 09			SPARE	
01 10			SPARE	
01 11			SPARE	
01 12			SERIALLY LOAD THE B REGISTER WITH A4 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FFF PUNCH TAPE CODES - /3 /1 #1 &C	INACTIVE BIT PATTERN BRMJ (OPD=11), ADDR FIELD NOW =14
01 13			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 14			SERIALLY LOAD THE B REGISTER WITH A1 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF2FFF PUNCH TAPE CODES - /3 /1 #3 &C	SIM NCJ POR BRMJ (OPD=3), ADDR FIELD NOW =30 IF POR WORKED, =31 IF NOT
01 15			MINOR 01 WITH POR IN MINOR 14	
01 16			SPARE	
01 17			SPARE	
01 18			BRANCH TO MAJOR 01 MINOR 40	BRANCH HERE FROM VARIABLE BRANCH
01 19			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 20			SPARE	
01 21			SPARE	
01 22			SPARE	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
01 23			SPARE	
01 24			SPARE	
01 25			SPARE	
01 26			SPARE	
01 27			SPARE	
01 28			SPARE	
01 29			SPARE	
01 30			SPARE	
01 31			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	MIN 17 WITH POR IN MIN 14
01 32			SPARE	
01 33			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 34	2	(00)T11.2	AUTO SECTION TEST LOC- TEST IF "MTC=A" ENABLES STATE 2. USE C->ROM TO VARY BRANCH ADDR. 1ST TIME THROUGH TEST =34, 2ND TIME =30 COMPARE THE B REGISTER TO THE A REGISTER LOGICALLY 'AND' C REGISTER AND 03F - RESULT IN B & C REGISTER INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOBFF BRANCH TO MAJOR 01 MINOR 4	C->ROM
01 35			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 36			SPARE	
01 37	2	(00)F16.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "CPJ215" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A2A10

01 38			SPARE	
01 39			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 40			BRANCH TO MAJOR 01 MINOR 88	
01 41			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 42			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 43			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 44			BRANCH TO MAJOR 01 MINOR 81	MIN 30 WITH POR IN MIN 14
01 45			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 46			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 47	2	(00)F20.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "CPJ215"	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A2A10	
01 48			SPARE	
01 49			SPARE	
01 50			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 51			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 52			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 53			SPARE	
01 54			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 55			SPARE	
01 56			SPARE	
01 57			SPARE	
01 58			SPARE	
01 59			SPARE	
01 60	3	F10.1.G	AUTO SECTION FAULT LOC- STATE 2 ONLY WHEN BRANCH WITHIN MAJ STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A1A(23,2) 2A1A2A(8,9,10,11)	
01 61			SPARE	
01 62			SPARE	
01 63			SPARE	
01 64			SPARE	
01 65	2	(00)F21.2	AUTO SECTION FAULT LOC- OPEN INPUT TO "CPJ225" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A2A11	
01 66			BEGIN TEST 01 "VARIFY ENTIRE TAPE" MINORS 66-80	
01 67			INITIAL SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFSF8FOFFF	EN LOAD OF SREG ON EMAIL
			ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 12 INCHES LONG RESET MEMORY FULL MODE PUNCH TAPE LEADER 12 INCHES LONG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER BRANCH TO MAJOR 01 MINOR 68 ON NO-GO BRANCH TO MAJOR 01 MINOR 69	
01 68			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 69				
01 70			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FDFFF0FFF COMPARE THE B REGISTER TO A00008 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 01 MINOR 71 ON NO-GO BRANCH TO MAJOR 01 MINOR 72	
01 71			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 72				
01 73			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1F070FFF ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 12 INCHES LONG RESET MEMORY FILL MODE PUNCH TAPE LEADER 12 INCHES LONG COMPARE THE B REGISTER TO A001 LOGICALLY 'AND' C REGISTER AND AE014 - RESULT IN B & C REGISTER BRANCH TO MAJOR 01 MINOR 74 ON NO-GO BRANCH TO MAJOR 01 MINOR 76	EN MTW1->BREG ON KMV011
01 74			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
01 75	2	(00)T10.1	AUTO SECTION TEST LOCATION- NO STATE 2 WITH UNBR, CHECK STATE 2 WITH BRMJ BRANCH TO MAJOR 01 MINOR 60	
01 76				
01 77			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO AE014 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 01 MINOR 78 ON NO-GO BRANCH TO MAJOR 01 MINOR 79	

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|TEST|DECISION | TEST/FAULT  |                          SELF-TEST PROGRAM                          |          REMARKS          |
|_NO.|__LEVEL__|___NUMBER____|_____________________________________________________________________|___________________________|


01 78                          STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON



01 79
01 80                          LOAD A REGISTER WITH 012
                               ENABLE MEMORY VERIFY ENTIRE TAPE MODE
                               STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON



01 81                        SPARE
01 82                        SPARE
01 83                        SPARE
01 84                        SPARE
01 85                        SPARE
01 86                        SPARE
01 87                        SPARE
01 88                        SPARE
01 89                        SPARE
01 90                        SPARE
01 91                        SPARE
01 92                        SPARE
01 93                        SPARE
01 94                        SPARE
01 95                        SPARE
01 96                        SPARE
01 97                        SPARE
01 98                        SPARE

01 99                         MINOR 85 IF POR IN MINOR 14
                               LOAD A REGISTER WITH 01800                                          SET UP BRANCH ADDR FOR
                                                                                                    VARIABLE BRANCH MAJ 1 MIN 1
                             FOLLOWING IS 498 NO OPS
                               PUNCH TAPE CODES - /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
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|TEST|DECISION | TEST/FAULT |                         SELF-TEST PROGRAM                              |       REMARKS          |
|_NO.|__LEVEL__|___NUMBER___|________________________________________________________________________|________________________|

                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                               /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                               /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                               &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
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SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
                                        /E /O &C /F /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /E /O &C /F /O &C /E /O &C /E /O &C /F /O
                                        &C /F /O &C /E /O &C /F /O &C /E /O &C /F /O &C
                                        /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /F /O &C /E /O &C /E /O &C /E /O &C /F /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /E /O &C /E /O &C /E /O &C /E /O &C /F /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /F /O &C /E /O &C /E /O &C /F /O &C /E /O &C /E
                                        /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /F /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /E /O &C /E /O &C /E /O &C /E /O &C /F /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /E /O &C /F /O &C /E /O &C /E /O &C /E /O &C /E
                                        /O &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O
                                        &C /E /O &C /E /O &C /E /O &C /E /O &C /E /O &C
                                        /E /O &C /E /O &C
END OF MAJOR TEST
```

TEST/REGISTER NO.	TEST/FAULT LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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*****************************************************************************************
*                                                                                       *
*                                    MAJOR TEST 02                                      *
*                                                                                       *
*                                                                                       *
*                              CONTAINS THE FOLLOWING SECTIONS :                        *
*                                1)TEST T30 OF AUTO SECTION                             *
*                                2)TEST (00)T1.11.3 OF AUTO SECTION                     *
*                                3)TEST (00)T2.6.3.3 OF AUTO SECTION                    *
*                                4)VARIOUS AUTO SECTION FAULT LOC.                      *
*                                5)BRANCH LOC TO AVOID PROCEED ERROR                    *
*                                                                                       *
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02 00 2 (00)F22.4 FAULT IN MABC, < INSTEAD OF =
LOAD A REGISTER WITH 001
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
PUNCH TAPE LEADER 12 INCHES LONG

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
TEST SET FAULT	2100000000	1A1A1A(23,14)	
		1A1A2A15	
NO GO	XXXXXXXXXXX	2A1A2A(8,9,10,11)	CPJ036*
TEST SET FAULT	1000000000	1A1A1A(21,22,23)	MPC062

FOLLOWING IS 524 NO OPS
PUNCH TAPE CODES - /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
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&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
&C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
/E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
/0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
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|TEST|DECISION | TEST/FAULT  |                              SELF-TEST PROGRAM                                 |         REMARKS           |
|_NO.|__LEVEL__|___NUMBER____|________________________________________________________________________________|__ ________________________|

                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0
                                                  &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
                                                  /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C /E
                                                  /0 &C /E /0 &C /E /0 &C /E /0 &C /E /0 &C
        2       (00)F1.12
                (00)F3.8
                (00)F8.3
                (00)F9.4
                (00)F22.5    NO BRANCH OR T.S. CONTROL

                                      ---------------------------------------------------------------
                                      |__INDICATORS___|_DISPLAY___|________REPLACE_ASSEMBLIES_________|
                                      |TEST_SET_FAULT_|220000000000|1A1A1A(10,11,21,22,23,12)__________|
                                      |TEST_SET_FAULT_| 20000000000|PROCEED_PER_PARAGRAPH_3-12D________|

                               PUNCH TAPE LEADER 12 INCHES LONG


02 01   2       (00)F1.1     AUTO SECTION FAULT LOC- BRANCH WITHIN MAJ INACTIVE
                               ENABLE VERTICAL PARITY CHECK
                               STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

                                      ---------------------------------------------------------------
                                      |__INDICATORS___|_DISPLAY___|________REPLACE_ASSEMBLIES_________|
                                      |NO_GO__________|___BLANK___|2A1A2A(6,8,9)______________________|


02 02                        SPARE
02 03                        SPARE


02 04   3       (00)T3.6.N   AUTO SECTION BRANCH LOC- TRANS T3.6.N -> T3.6.NN THRU MAJ 2 TO AVOID
                             PROCEED ERROR AT 02 00
                               BRANCH TO MAJOR 19 MINOR 3                                        GO TO T3.6.NN
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
02 05	5	(00)F3.6.6	FAULT IN WAIT FOR END OF DATA STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A1A09	APF351* 501
02 06	1	T30	AUTO SECTION TEST LOCATION - TEST OF LSB, 6SB, 4SB, 3SR OF MABC PREVIOUS TEST = (00)T22 ENABLE VERTICAL PARITY CHECK BRANCH TO MAJOR 37 MINOR 2	
02 07	2	(00)F3.5	INPUT TO "BRANCH WITHIN MAJ" OPEN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 12A1A2A06	
02 08			SPARE	
02 09			SPARE	
02 10	1		MANUAL SECTION BRANCH LOC- TRANSFER 00 12 -> 12 01 THRU HERE TO AVOID PROCEED ERROR AT 02 00 BRANCH TO MAJOR 12 MINOR 1	GO TO FINAL TESTS OF MANUAL MEMORY CONTROL TESTS
02 11			SPARE	
02 12			SPARE	
02 13			SPARE	
02 14			SPARE	
02 15			SPARE	
02 16			SPARE	
02 17			SPARE	
02 18			SPARE	
02 19 02 20	3	(00)T1.11.	TEST SCU INST DECODE MATRIX USING LDAB & CMAB SERIALLY LOAD THE B REGISTER WITH AAAAAAAA COMPARE THE B REGISTER TO 55555555 BRANCH TO MAJOR 02 MINOR 21 ON NO-GO	
	4	F1.11.2.6	FAULT IN SCU INST DECODE MATRIX, LSDD=3 ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /B /8 6C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	INVALID INST = 7713 OCTAL

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			TEST SET FAULT / 400000001 2A1A2A(1,2)	IAI544 S@0
			TEST SET FAULT / 400000401 HIGHER LEVEL OF MAINTENANCE	IAI544 STRING
			NO GO / BLANK / PROCEED PER PARAGRAPH 13-3	
02 21	4	F1.11.2.N	FAULT AT BRMJ IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / 37777777777 / 2A1A2A(6,12)	
02 22	5	(00)F3.6.G	FAULT IN NO-GO "OR"GATE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / 17000000000 / 2A1A2A06	AAT091 S@0
02 23			SPARE	
02 24			SPARE	
02 25			SPARE	
02 26			SPARE	
02 27			SPARE	
02 28			SPARE	
02 29			SPARE	
02 30	3	(01)F11.2.	"MTC= A" OK BUT "MTC>A" FAILS ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / 30000000002 / 2A1A2A(8,9,10)	IPJ016* S@1
02 31			SPARE	
02 32			SPARE	
02 33			SPARE	
02 34	3	(01)F11.2.	BOTH "MTC>A" & "MTC=A" FAIL ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 320000000012A1A2A(8,10) — REPLACE ASSEMBLIES	CPJ036* S@1
02 35			SPARE	
02 36			SPARE	
02 37			SPARE	
02 38			SPARE	
02 39			SPARE	
02 40			SPARE	
02 41			SPARE	
02 42			SPARE	
02 43			SPARE	
02 44			SPARE	
02 45			SPARE	
02 46			SPARE	
02 47			SPARE	
02 48			SPARE	
02 49			SPARE	
02 50			SPARE	
02 51			SPARE	
02 52			SPARE	
02 53			SPARE	
02 54			SPARE	
02 55			SPARE	
02 56			SPARE	
02 57			SPARE	
02 58			SPARE	
02 59			SPARE	
02 60	3	(01)F10.1.	CAN NOT BRANCH IN REV DIRECTION, NO AUTO START T.S. ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A10; 1A1A3A05; 2A1A2A(11,8,9,17)	
02 61			SPARE	
02 62			SPARE	
02 63			SPARE	
02 64			SPARE	
02 65			SPARE	
02 66			SPARE	
02 67			SPARE	
02 68			SPARE	
02 69			SPARE	
02 70			SPARE	
02 71			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
02 72			SPARE	
02 73			SPARE	
02 74	4	(OC)T3.6.G	TEST SCU INST DECODE MATIX USING TST1	
02 75			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEEFOFF7 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 2 MINOR 76 ON NO-GO	PJB -> RIM
	5	F3.6.G.3.C	FAULT IN SCU INST DECODE MATRIX, LSOD=5 ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /D /8 &C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	INVALID INSR = 2/1/5 OCTAL

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
TEST SET FAULT	400000001	2A1A2A(1,2)	IAI546 S@0
TEST SET FAULT	400000401	HIGHER LEVEL OF MAINTENANCE	IAI546 STRING
NO GO	BLANK	PROCEED PER PARAGRAPH 13-3	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
02 76	5	F3.6.G.3.N	BNMJ IBT OF LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	177777777712	A1A2A(1,6)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
02 77			SPARE	
02 78			SPARE	
02 79			SPARE	
02 80			SPARE	
02 81			SPARE	
02 82			SPARE	
02 83			SPARE	
02 84			SPARE	
02 85			SPARE	
02 86			SPARE	
02 87			SPARE	
02 88			SPARE	
02 89			SPARE	
02 90			SPARE	
02 91			SPARE	
02 92			SPARE	
02 93			SPARE	
02 94			SPARE	
02 95			SPARE	
02 96			SPARE	
02 97			SPARE	
02 98			SPARE	
02 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE LEADER 12 INCHES LONG	
			DEFINE SELF TEST TAPE	
			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NOJ CLOCK MODE (GTC003*)	
			ENABLE LOW LEVEL ON GTC001*	
			BRANCH TO MAJOR 5 MINOR 0	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
04	01		BRANCH TO MAJOR 5 MINOR 2	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
04	02		BRANCH TO MAJOR 5 MINOR 3	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
04	03		BRANCH TO MAJOR 5 MINOR 4 ON NO-GO	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
04	04		END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
05 00			STOP TAPE	
			BRANCH TO MAJOR 05 MINOR 5	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 01			STOP TAPE	
			BRANCH TO MAJOR 4 MINOR 1	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 02			STOP TAPE	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4FFF	SIM NO-GO
			BRANCH TO MAJOR 4 MINOR 2 ON NO-GO	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 03			STOP TAPE	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF4FFF	SIM NO-GO
			BRANCH TO MAJOR 4 MINOR 3	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 04			STOP TAPE	
			BRANCH TO MAJOR 05 MINOR 6	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 05			BRANCH TO MAJOR 05 MINOR 1	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
05 06			ENABLE VERTICAL PARITY CHECK	
05 07			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
*****************************************************************************************************
*                                                                                                   *
*                                  TEST FORMAT CHECK WITH WRONG FORMAT                              *
*                                                                                                   *
*****************************************************************************************************

06 00                          DEFINE SELF TEST TAPE
                             1ST ADDR CHAR FOLLOWING 2ND INST CHAR
                               PUNCH TAPE CODES - /F /7 @6                          ADDR = 60 01

                               PUNCH TAPE CODES - @0 /F /7 &C /F /7 &C              SET UP TEST ADDR

                             1ST ADDR CHAR FOLLOWING 1ST INST CHAR
                               PUNCH TAPE CODES - /F @6                             ADDR = 60 02

                             2ND INST CHAR FOLLOWING 1ST ADDR CHAR
                               PUNCH TAPE CODES - /7                                ADDR = 60 03

                             2ND ADDR CHAR FOLLOWING 2ND INST CHAR
                               PUNCH TAPE CODES - @0                                ADDR = 06 00

                               PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C /F /7 &C   SET UP TEST ADDR

                             1ST INST CHAR FOLLOWING DATA CHAR
                               PUNCH TAPE CODES - #0 /F                             ADDR = 06 04

                               PUNCH TAPE CODES - /7 &C                             SET UP TEST ADDR

                             1ST INST CHAR FOLLOWING 1ST ADDR CHAR
                               PUNCH TAPE CODES - @6 /F                             ADDR = 60 05

                             2ND ADDR CHAR FOLLOWING 1ST INST CHAR
                               PUNCH TAPE CODES - @0                                ADDR = 06 00

                               PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C
                               PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C        SET UP TEST ADDR

                             DATA CHAR FOLLOWING 1ST INST CHAR
                               PUNCH TAPE CODES - /F #0                             ADDR = 06 06

                             2ND INST CHAR FOLLOWING DATA CHAR
                               PUNCH TAPE CODES - /7                                ADDR = 06 07
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE CODES - &C /F /7 &C	SET UP TEST ADDR
			DATA CHAR FOLLOWING 1ST ADDR CHAR PUNCH TAPE CODES - @6 #0	ADDR = 60 08
			2ND ADDR CHAR FOLLOWING DATA CHAR PUNCH TAPE CODES - @0	ADDR = 06 00
			PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C	SET UP TEST ADDR
			END OF DATA CHAR FOLLOWING 1ST ADDR CHAR PUNCH TAPE CODES - @6 &C	ADDR = 60 09
			PUNCH TAPE CODES - @0 /F /7 &C PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C PUNCH TAPE CODES - /F /7 &C /F /7 &C /F /7 &C	SET UP TEST ADDR
06	10		7 HOLE PRESENT PUNCH TAPE CODES - 40	
06	11		HORIZONTAL PARITY EVEN => FAULT PUNCH TAPE CODES - &4 PUNCH TAPE CODES - 88 08 80	2ND & 3RD CHAR EVEN VERTICAL PARITY
			CHECK FOR CORRECT VERTICAL PARITY PUNCH TAPE CODES - /1 /5 &9	ENABLE VERTICAL PARITY CHECK
06	12		COLUMN 1 = ODD VERTICAL PARITY => FAULT PUNCH TAPE CODES - &4 PUNCH TAPE CODES - /1 /5 &5	ENABLE VERTICAL PARITY CHECK
06	13		COLUMN 2 = ODD VERTICAL PARITY PUNCH TAPE CODES - &4 PUNCH TAPE CODES - 02 PUNCH TAPE CODES - /1 /5 &5	SET UP VERTICAL PARITY FAULT ENABLE VERTICAL PARITY CHECK
06	14		COLUMN 3 = ODD VERTICAL PARITY PUNCH TAPE CODES - &4 PUNCH TAPE CODES - 02	SET UP VERTICAL PARITY FAULT

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE CODES - /1 /5 &0	ENABLE VERTICAL PARITY CHECK
06	15		COLUMN 4 = ODD VERTICAL PARITY	
			PUNCH TAPE CODES - &4	
			PUNCH TAPE CODES - 08	SET UP VERTICAL PARITY FAULT
			PUNCH TAPE CODES - /1 /5 &0	ENABLE VERTICAL PARITY CHECK
06	16		COLUMN 6 = ODD VERTICAL PARITY	
			PUNCH TAPE CODES - &4	
			PUNCH TAPE CODES - 20 80 80	SET UP VERTICAL PARITY FAULT
			PUNCH TAPE CODES - /1 /5 &0	ENABLE VERTICAL PARITY CHECK
06	17		COLUMN 8 = ODD VERTICAL PARITY	
			PUNCH TAPE CODES - &4	
			PUNCH TAPE CODES - 20 80 80	SET UP VERTICAL PARITY FAULT
			PUNCH TAPE CODES - /1 /5 &4	ENABLE VERTICAL PARITY CHECK
06	18		CHECK FOR CORRECT VERTICAL PARITY	
			PUNCH TAPE CODES - &4	CLEAR VERTICAL PARITY
			PUNCH TAPE CODES - /1 /5 &4	ENABLE VERTICAL PARITY CHECK
			END OF MAJOR TEST	

TEST DECISION NO.	TEST/FAULT LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** IN-PROCESS REGISTER FAULTS TESTS AND REGISTERS TESTS **********	
07 00			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	
			COMPARE THE B REGISTER TO 00000000	BOTH A&B REG SATURATED WITH 0 S => NO FAULT
07 01			COMPARE THE B REGISTER TO FFFFFFFF	A ALL 1 S, B ALL 0 S => FAULT
07 02			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFDFOFBF SERIALLY LOAD THE B REGISTER WITH FFFFFFFF COMPARE THE B REGISTER TO 00000000	GREG->DSPL, MSHD DSPL->RIM A ALL 0 S,B ALL 1 S => FAULT
07 03			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFDFOFBF SERIALLY LOAD THE B REGISTER WITH AFFFFFFF COMPARE THE B REGISTER TO 0	GREG->DSPL, MSHD DSPL->RIM TEST CL AREG
07 04			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFDFOFBF LOGICALLY 'AND' C REGISTER AND AFFFFFFF - RESULT IN B & C REGISTER COMPARE THE B REGISTER TO THE A REGISTER	GREG->DSPL, MSHD DSPL->RIM TEST C->B & PE OF MSHD WITH AANC BREG SATURATED WITH 1 S => FAULT
07 05			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF LOGICALLY 'AND' C REGISTER AND AFFFFFFF - RESULT IN B & C REGISTER COMPARE THE B REGISTER TO A	MSHD DSPL=0->RIM TEST C=0 S->B & PE OF MSHD=0 WITH AANC BREG SATURATED WITH 0 S => FAULT
07 06			LOGICALLY 'AND' C REGISTER AND AFFFFFFF - RESULT IN B & C REGISTER COMPARE THE B REGISTER TO 5 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 07			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 08			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFDFOFBF SERIALLY LOAD THE B REGISTER WITH FFFFFFFF COMPARE THE B REGISTER TO THE A REGISTER	GREG->DSPL, MSHD=F->RIM BOTH A&B REG SATURATED WITH 1S =>NO FAULT
07 09			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 07 MINOR 10 ON NO-GO BRANCH TO MAJOR 07 MINOR 11	
07 10			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 11				
07 12			LOGICALLY 'AND' C REGISTER AND AFFFFFFF - RESULT IN B & C REGISTER COMPARE THE B REGISTER TO A BRANCH TO MAJOR 07 MINOR 13 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 07 MINOR 14	
07 13			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 14				
07 15			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			COMPARE THE B REGISTER TO THE A REGISTER	
			BRANCH TO MAJOR 07 MINOR 16 ON NO-GO	
			BRANCH TO MAJOR 07 MINOR 17	
07 16			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 17				
07 18			SERIALLY LOAD THE B REGISTER WITH A0000000	
			COMPARE THE B REGISTER TO THE A REGISTER	
			BRANCH TO MAJOR 07 MINOR 19 ON NO-GO	
			BRANCH TO MAJOR 07 MINOR 20	
07 19			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 20				
07 21			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			SERIALLY LOAD THE B REGISTER WITH A	
			COMPARE THE B REGISTER TO A0000000	
			BRANCH TO MAJOR 07 MINOR 22 ON NO-GO	
			BRANCH TO MAJOR 07 MINOR 23	
07 22			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 23				
07 24			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			COMPARE THE B REGISTER TO AEFFFFFF	
			BRANCH TO MAJOR 07 MINOR 26 ON NO-GO	
07 25			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 26				
07 27			LOGICALLY 'AND' C REGISTER AND AFFFFFFF - RESULT IN B & C REGISTER	
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 07 MINOR 29 ON NO-GO	
07 28			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 29				
07 30			COMPARE THE B REGISTER TO A1	
			BRANCH TO MAJOR 07 MINOR 31 ON NO-GO	
			BRANCH TO MAJOR 07 MINOR 32	
07 31			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
07 32			ENABLE VERTICAL PARITY CHECK	
07 33			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			**********	
			*	
			* MANUAL MEMORY TEST CONTROL SELF TEST	
			* MAJORS 8, AND 10 - 12	
			*	
			**********	
08 00			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	
08 01			ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 24 INCHES LONG RESET MEMORY FILL MODE STOP TAPE	
08 02			ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 36 INCHES LONG RESET MEMORY FILL MODE PUNCH TAPE LEADER 12 INCHES LONG STOP TAPE	
08 03			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F7F0F0FFF ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 0	SIM CM7, INH ALL MEM
08 04			RESET MEMORY FILL MODE	
08 05			ENABLE VERTICAL PARITY CHECK	
08 06			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST/SUBDIVISION NO.	TEST/FAULT LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
09 00				
09 01			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
09 02	2	F242.1 F332.1	AUTO FAULT LOC - ABS111 OR ABS112 SET STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO-GO	BLANK	11A1A1A22

09 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
10 00			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	
10 01			ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0	
10 02			RESET MEMORY FILL MODE	
10 03			BRANCH TO MAJOR 11 MINOR 20	
10 04			END OF MAJOR TEST	

TEST DECISION	TEST/FAULT	SELF-TEST PROGRAM	REMARKS
GO/NO-GO	LEVEL / NUMBER		
	11 00	BRANCH TO ADDRESS LOCATION IN A REGISTER	VARIABLE BRANCH
	11 01	ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: A022C680 PUNCH TAPE LEADER 12 INCHES LONG	
	11 02	STOP TAPE SERIALLY LOAD THE B REGISTER WITH A0180008 COMPARE THE B REGISTER TO A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F8F0FFF	CREG->ROM, ROM->WI DR, LOAD BREG ON XMA152
		ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: A022C680 PUNCH TAPE LEADER 12 INCHES LONG	
	11 03	BRANCH TO MAJOR 11 MINOR 4 ON NO-GO BRANCH TO MAJOR 11 MINOR 5	
	11 04	STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
	11 05	LOAD A REGISTER WITH A26 RESET MEMORY FILL MODE PUNCH TAPE LEADER 6 INCHES LONG STOP TAPE	
	11 06	SPARE	
	11 07	SPARE	
	11 08	SPARE	
	11 09	SPARE	
	11 10	SPARE	
	11 11	SPARE	
	11 12	SPARE	
	11 13	SPARE	
	11 14	SPARE	
	11 15	SPARE	
	11 16	SPARE	
	11 17	SPARE	
	11 18	SPARE	
	11 19	SPARE	
	11 20	STOP TAPE PUNCH TAPE LEADER 6 INCHES LONG SERIALLY LOAD THE B REGISTER WITH A01AC688 COMPARE THE B REGISTER TO A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F0F08FF	CREG->ROM, ROM->WI DR, INIT ALL MEM
		RESET MEMORY FILL MODE PUNCH TAPE LEADER 3 INCHES LONG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
11	21		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
11	22		SPARE	
11	23		SPARE	
11	24		SPARE	
11	25		SPARE	
11	26		ENABLE VERTICAL PARITY CHECK	
11	27		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
12 00			DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (STC003*) ENABLE LOW LEVEL ON STC001* BRANCH TO MAJOR 12 MINOR 3	AUTO MODE MEMORY VERIFY TESTS
12 01			STOP TAPE	
12 02			BRANCH TO MAJOR 12 MINOR 7	
12 03			LOAD A REGISTER WITH 004 ENABLE MEMORY VERIFY ENTIRE TAPE MODE	
12 04			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
12 05			SPARE	
12 06			SPARE	
12 07			ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 12 INCHES LONG RESET MEMORY FILL MODE PUNCH TAPE LEADER 12 INCHES LONG	
12 08			STOP TAPE	
12 09			ENABLE HI SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 PUNCH TAPE LEADER 12 INCHES LONG ENABLE MEMORY VERIFY ENTIRE TAPE MODE PUNCH TAPE LEADER 3 INCHES LONG	
12 10			STOP TAPE PUNCH TAPE LEADER 12 INCHES LONG	
12 11			RESET MEMORY FILL MODE PUNCH TAPE LEADER 6 INCHES LONG	
12 12			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
12 13			BRANCH TO MAJOR 12 MINOR 15	
12 14			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
12 15			ENABLE VERTICAL PARITY CHECK	
12 16			END OF MAJOR TEST	

```
| TEST| DECISION | TEST/FAULT |                    SELF-TEST PROGRAM                    |          REMARKS          |
| NO. |  LEVEL   |   NUMBER   |                                                         |                           |

*****************************************************************************************************
*                                                                                                   *
*                          MANUAL MULTIPLEXER SYSTEM TESTS, MAJORS 14 & 16                          *
*                                        PART 1 = MAJOR 14                                          *
*                                        PART 2 = MAJOR 16                                          *
*                                                                                                   *
*                                            PART 1 :                                               *
*                      MUX CONTROL & ROM -> DSPL LOGICAL FAULTS - MINORS 1 THRU 7                   *
*                                ROM -> DSPL SHORTS - MINORS 8 THRU 71                              *
*                                                                                                   *
*****************************************************************************************************

14 00                   INITIALIZE
                          DEFINE SELF TEST TAPE
                          ENABLE LOW LEVEL ON GTC001*

14 01                   TEST BREG = ZERO -> DSPL => DSPL = BLANK
                          INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F07FF      BREG->ROM, ROM DSPL
                          STOP TAPE

14 02                   TEST BREG = FFFFFFFF HEX -> DSPL => DSPL = 37777777777
                          LOAD A REGISTER WITH FFFFFFFF
                          INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F       ROM->RIM
                          INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F07FF       BREG->ROM, ROM DSPL
                          STOP TAPE

14 03                   TEST CREG = FFFFFFFF HEX -> DSPL => DSPL = 37777777777, NO-GO IND
                          SERIALLY LOAD THE B REGISTER WITH AFFFFFFF
                          COMPARE THE B REGISTER TO 5
                          STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

14 04                   TEST AREG = ZERO -> DSPL => DSPL = BLANK
                          LOAD A REGISTER WITH 00000000
                          INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF       ROM->DSPL
                          STOP TAPE

14 05                   TEST AREG = ZERO -> DSPL, BREG = FFFFFFFF, CREG = ZERO => DSPL = BLANK
                          LOAD A REGISTER WITH FFFFFFFF
                          INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F       ROM->RIM
                          LOAD A REGISTER WITH 00000000
                          INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF       ROM->DSPL
                          STOP TAPE

14 06                   TEST AREG = ZERO -> DSPL, BREG = ZERO, CREG = FFFFFFFF => DSPL = BLANK
                          SERIALLY LOAD THE B REGISTER WITH AFFFFFFF
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO 5	
			LOAD A REGISTER WITH 00000000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F	ROM->RIM
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF	ROM->DSPL
			STOP TAPE	
14	07		AREG = FFFFFFFF -> DSPL, BREG = CREG = ZERO => DSPL = 37777777777	
			SERIALLY LOAD THE B REGISTER WITH A	
			COMPARE THE B REGISTER TO A	
			LOAD A REGISTER WITH 00000000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F	ROM->RIM
			LOAD A REGISTER WITH FFFFFFFF	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF7F0FFF	ROM->DSPL
			STOP TAPE	
			**********	
			*	
			* TEST FOR SHORT IN ROM -> DSPL, MINORS 8 - 71	
			* PROCEED PER PARAGRAPH 3-4	
			*	
			**********	
14	08		DSPL =20000000000	
			SERIALLY LOAD THE B REGISTER WITH A	
			COMPARE THE B REGISTER TO 2	
14	09		DSPL = 1777777777	
			COMPARE THE B REGISTER TO 0FFFFFFF	
14	10		DSPL =10000000000	
			COMPARE THE B REGISTER TO E	
14	11		DSPL =27777777777	
			COMPARE THE B REGISTER TO 1FFFFFFF	
14	12		DSPL =4000000000	
			COMPARE THE B REGISTER TO 8	
14	13		DSPL =33777777777	
			COMPARE THE B REGISTER TO 7FFFFFFF	
14	14		DSPL =2000000000	
			COMPARE THE B REGISTER TO B	
14	15		DSPL =35777777777	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO 4FFFFFFF	
14	16		DSPL =1000000000 COMPARE THE B REGISTER TO A8	
14	17		DSPL =36777777777 COMPARE THE B REGISTER TO 57FFFFFF	
14	18		DSPL =400000000 COMPARE THE B REGISTER TO A4	
14	19		DSPL =37377777777 COMPARE THE B REGISTER TO 5BFFFFFF	
14	20		DSPL =200000000 COMPARE THE B REGISTER TO A2	
14	21		DSPL =37577777777 COMPARE THE B REGISTER TO 5DFFFFFF	
14	22		DSPL =100000000 COMPARE THE B REGISTER TO A1	
14	23		DSPL =37677777777 COMPARE THE B REGISTER TO 5EFFFFFF	
14	24		DSPL =40000000 COMPARE THE B REGISTER TO A08	
14	25		DSPL =37737777777 COMPARE THE B REGISTER TO 5F7FFFFF	
14	26		DSPL =20000000 COMPARE THE B REGISTER TO A04	
14	27		DSPL =37757777777 COMPARE THE B REGISTER TO 5FBFFFFF	
14	28		DSPL =10000000 COMPARE THE B REGISTER TO A02	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
14 29			DSPL =37767777777 COMPARE THE B REGISTER TO 5FDFFFFF	
14 30			DSPL =4000000 COMPARE THE B REGISTER TO A01	
14 31			DSPL =37773777777 COMPARE THE B REGISTER TO 5FEFFFFF	
14 32			DSPL =2000000 COMPARE THE B REGISTER TO A008	
14 33			DSPL =37775777777 COMPARE THE B REGISTER TO 5FF7FFFF	
14 34			DSPL =1000000 COMPARE THE B REGISTER TO A004	
14 35			DSPL =37776777777 COMPARE THE B REGISTER TO 5FFBFFFF	
14 36			DSPL =400000 COMPARE THE B REGISTER TO A002	
14 37			DSPL =37777377777 COMPARE THE B REGISTER TO 5FFDFFFF	
14 38			DSPL =200000 COMPARE THE B REGISTER TO A001	
14 39			DSPL =37777577777 COMPARE THE B REGISTER TO 5FFEFFFF	
14 40			DSPL =100000 COMPARE THE B REGISTER TO A0008	
14 41			DSPL =37777677777 COMPARE THE B REGISTER TO 5FFF7FFF	
14 42			DSPL =40000	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A0004	
14	43		DSPL =37777737777 COMPARE THE B REGISTER TO 5FFF8FFF	
14	44		DSPL =20000 COMPARE THE B REGISTER TO A0002	
14	45		DSPL =37777757777 COMPARE THE B REGISTER TO 5FFFDFFF	
14	46		DSPL =10000 COMPARE THE B REGISTER TO A0001	
14	47		DSPL =37777767777 COMPARE THE B REGISTER TO 5FFFEFFF	
14	48		DSPL =4000 COMPARE THE B REGISTER TO A00008	
14	49		DSPL =37777773777 COMPARE THE B REGISTER TO 5FFFF7FF	
14	50		DSPL =2000 COMPARE THE B REGISTER TO A00004	
14	51		DSPL =37777775777 COMPARE THE B REGISTER TO 5FFFFBFF	
14	52		DSPL =1000 COMPARE THE B REGISTER TO A00002	
14	53		DSPL =37777776777 COMPARE THE B REGISTER TO 5FFFFDFF	
14	54		DSPL =400 COMPARE THE B REGISTER TO A00001	
14	55		DSPL =37777777377 COMPARE THE B REGISTER TO 5FFFFEFF	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
14 56			DSPL =200 COMPARE THE B REGISTER TO A000008	
14 57			DSPL =37777777577 COMPARE THE B REGISTER TO 5FFFFF7F	
14 58			DSPL =100 COMPARE THE B REGISTER TO A000004	
14 59			DSPL =37777777677 COMPARE THE B REGISTER TO 5FFFFFBF	
14 60			DSPL =40 COMPARE THE B REGISTER TO A000002	
14 61			DSPL =37777777737 COMPARE THE B REGISTER TO 5FFFFFDF	
14 62			DSPL =20 COMPARE THE B REGISTER TO A000001	
14 63			DSPL =37777777757 COMPARE THE B REGISTER TO 5FFFFFEF	
14 64			DSPL =10 COMPARE THE B REGISTER TO A0000008	
14 65			DSPL =37777777767 COMPARE THE B REGISTER TO 5FFFFFF7	
14 66			DSPL =4 COMPARE THE B REGISTER TO A0000004	
14 67			DSPL =37777777773 COMPARE THE B REGISTER TO 5FFFFFFB	
14 68			DSPL =2 COMPARE THE B REGISTER TO A0000002	
14 69			DSPL =37777777775	

OFFSET (HEX)	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO 5FFFFF5D	
14 70			DSPL =1 COMPARE THE B REGISTER TO A0000001	
14 71			DSPL =37777777775 COMPARE THE B REGISTER TO 5FFFFFFF	
14 72			COMPARE THE B REGISTER TO A END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			**********	
			* MANUAL ANALOG TESTS *	
			* MAJOR 15 *	
			**********	
15 00			DEFINE SELF TEST TAPE	
			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*)	
			ENABLE LOW LEVEL ON GTC001*	
15 01			SERIALLY LOAD THE B REGISTER WITH A408000F	SET UP 4.7VDC TEST IF NO TRANS A->B
			LOAD ANALOG CONTROL WORD WITH A00R0	TEST MONITOR SW & BUFF AMP SAT WITH NO CHANNELS EN
			RESET ANALOG CONTROL WORD	
15 02			LOAD A REGISTER WITH AFFFFFFF	SET UP DATA TO BE CLEARED
			LOAD ANALOG CONTROL WORD WITH A4080	TEST +15VDC
			COMPARE THE B REGISTER TO A4080	TEST FOR AREG CLEARED
			BRANCH TO MAJOR 15 MINOR 37 ON NO-GO	
15 03			RESET ANALOG CONTROL WORD	
			STOP TAPE	TEST CLEAR OF ANALOG CONTROL WORD
15 04			LOAD ANALOG CONTROL WORD WITH A2080	TEST 26VAC
			**********	
			* LOW LEVEL CHANNELS TESTS *	
			**********	
15 05			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00080	SET 28V ANALOG SW
			LOAD ANALOG CONTROL WORD WITH A9080	D.A.ERROR
15 06			LOAD ANALOG CONTROL WORD WITH A8880	L.S.ERROR
15 07			LOAD ANALOG CONTROL WORD WITH A8480	G.S.ERROR
15 08			LOAD ANALOG CONTROL WORD WITH A8280	DEV
15 09			LOAD ANALOG CONTROL WORD WITH A8180	AZ.C. ERROR
			**********	
			* DC VOLTAGE CHANNELS TESTS *	
			**********	
15 10			LOAD ANALOG CONTROL WORD WITH A0082	+30VDC, QUV130
15 11			LOAD ANALOG CONTROL WORD WITH A00C2	+30VDC, QUV230
15 12			LOAD ANALOG CONTROL WORD WITH A00A2	+12VDC, QUV112
15 13			LOAD ANALOG CONTROL WORD WITH A00E2	-06VDC, QUV106
15 14			LOAD ANALOG CONTROL WORD WITH A0092	+12VDC, QUV212

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
15 15			LOAD ANALOG CONTROL WORD WITH A00D2	-06VDC, QUV206
15 16			LOAD ANALOG CONTROL WORD WITH A00B2	+05VDC, QUV105
15 17			LOAD ANALOG CONTROL WORD WITH A00F2	+05VDC, QUV205
			**********	
			*	*
			* SYNCHRO CHANNELS TESTS	*
			*	*
			**********	
15 18			LOAD ANALOG CONTROL WORD WITH A0088	RSS000
15 19			LOAD ANALOG CONTROL WORD WITH A00C8	RSS001
15 20			LOAD ANALOG CONTROL WORD WITH A00A8	RSS002
15 21			LOAD ANALOG CONTROL WORD WITH A00E8	RSS003
15 22			LOAD ANALOG CONTROL WORD WITH A0098	RSS008
15 23			LOAD ANALOG CONTROL WORD WITH A00D8	RSS009
15 24			LOAD ANALOG CONTROL WORD WITH A00B8	RSS010
15 25			LOAD ANALOG CONTROL WORD WITH A00F8	RSS011
15 26			LOAD ANALOG CONTROL WORD WITH A0084	RSS006
15 27			LOAD ANALOG CONTROL WORD WITH A00C4	RSS007
15 28			LOAD ANALOG CONTROL WORD WITH A00A4	RSS012
15 29			LOAD ANALOG CONTROL WORD WITH A00E4	RSS013
15 30			LOAD ANALOG CONTROL WORD WITH A0094	RSS004
15 31			LOAD ANALOG CONTROL WORD WITH A00D4	RSS005
15 32			LOAD ANALOG CONTROL WORD WITH A00B4	RSS014
15 33			LOAD ANALOG CONTROL WORD WITH A00F4	RSS015
			**********	
			*	*
			* TESTS OF INACTIVE CONTROL WORD	*
			*	*
			**********	
15 34			LOAD ANALOG CONTROL WORD WITH A4000	MONITOR SW NOT EN
15 35			LOAD ANALOG CONTROL WORD WITH A8080	NO CHANNELS ENABLED TO PREAMP
15 36			LOAD ANALOG CONTROL WORD WITH A0880	PREAMP NOT ENABLED TO BUFF AMP
			BRANCH TO MAJOR 15 MINOR 38	
15 37			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000	
			RESET ANALOG CONTROL WORD	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
15 38			RESET ANALOG CONTROL WORD	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000	
			ENABLE VERTICAL PARITY CHECK	
			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** MANUAL MULTIPLEXER TESTS- PART 2, PART 1 = MAJOR 14 PROCEED PER PARAGRAPH 3-4 TEST FOR SHORTS INMX->RIM->BREG **********	
16	00		INITIALIZE DEFINE SELF TEST TAPE ENABLE LOW LEVEL ON GTC001*	
16	01		DSPL =20000000000 SERIALLY LOAD THE B REGISTER WITH A COMPARE THE B REGISTER TO 2 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	02		DSPL = 1777777777 COMPARE THE B REGISTER TO FFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	03		DSPL =1000000000 LOAD A REGISTER WITH 3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	04		DSPL =2777777777 COMPARE THE B REGISTER TO FFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	05		DSPL =4000000000 LOAD A REGISTER WITH 9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
16 06			DSPL =33777777777 COMPARE THE B REGISTER TO FFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 07			DSPL =2000000000 LOAD A REGISTER WITH C COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 08			DSPL =35777777777 COMPARE THE B REGISTER TO FFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BDF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 09			DSPL =1000000000 LOAD A REGISTER WITH E7 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 10			DSPL =36777777777 COMPARE THE B REGISTER TO FFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 11			DSPL =4000000000 LOAD A REGISTER WITH F3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 12			DSPL =37377777777 LOAD A REGISTER WITH FFFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
16 13			DSPL =20000000 LOAD A REGISTER WITH F9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 14			DSPL =37577777777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08BF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 15			DSPL =10000000 LOAD A REGISTER WITH FC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F083F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 16			DSPL =37677777777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08BF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 17			DSPL =40000000 LOAD A REGISTER WITH FF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08BF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 18			DSPL =37737777777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08BF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16 19			DSPL =20000000 LOAD A REGISTER WITH FF3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F08BF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
16	20		DSPL =3775777777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	21		DSPL =10000000 LOAD A REGISTER WITH FF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	22		DSPL =3776777777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	23		DSPL =4000000 LOAD A REGISTER WITH FFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	24		DSPL =3777377777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	25		DSPL =2000000 LOAD A REGISTER WITH FFE7 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	26		DSPL =3777577777 LOAD A REGISTER WITH FFFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL ->

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				RIM
16	27		DSPL =1000000 LOAD A REGISTER WITH FFF3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	28		DSPL =37776777777 LOAD A REGISTER WITH FFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	29		DSPL =400000 LOAD A REGISTER WITH FFF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	30		DSPL =37777377777 LOAD A REGISTER WITH FFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	31		DSPL =200000 LOAD A REGISTER WITH FFFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	32		DSPL =37777577777 LOAD A REGISTER WITH FFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	33		DSPL =100000 LOAD A REGISTER WITH FFFE7 COMPARE THE B REGISTER TO THE A REGISTER	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 34			DSPL =37777677777 LOAD A REGISTER WITH FFFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 35			DSPL =40000 LOAD A REGISTER WITH FFFF8 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 36			DSPL =37777737777 LOAD A REGISTER WITH FFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 37			DSPL =20000 LOAD A REGISTER WITH FFFF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 38			DSPL =37777757777 LOAD A REGISTER WITH FFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 39			DSPL =10000 LOAD A REGISTER WITH FFFFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKD DSPL -> RIM
16 40			DSPL =37777767777	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD A REGISTER WITH FFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	41		DSPL =4000 LOAD A REGISTER WITH FFFFE7 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	42		DSPL =37777773777 LOAD A REGISTER WITH FFFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	43		DSPL =2000 LOAD A REGISTER WITH FFFFF3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	44		DSPL =37777775777 LOAD A REGISTER WITH FFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	45		DSPL =1000 LOAD A REGISTER WITH FFFFF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	46		DSPL =37777776777 LOAD A REGISTER WITH FFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
16	47		DSPL =400 LOAD A REGISTER WITH FFFFFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	48		DSPL =3777777377 LOAD A REGISTER WITH FFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	49		DSPL =200 LOAD A REGISTER WITH FFFFFE7 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	50		DSPL =3777777577 LOAD A REGISTER WITH FFF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	51		DSPL =100 LOAD A REGISTER WITH FFFFFE3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	52		DSPL =3777777677 LOAD A REGISTER WITH FF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	53		DSPL =40 LOAD A REGISTER WITH FFFFFF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0BBF	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL ->

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				RIM
16	54		DSPL =3777777737 LOAD A REGISTER WITH FF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	55		DSPL =20 LOAD A REGISTER WITH FFFFFFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	56		DSPL =37777777757 LOAD A REGISTER WITH FF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	57		DSPL =10 LOAD A REGISTER WITH FFFFFFE7 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	58		DSPL =37777777767 LOAD A REGISTER WITH FF COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	59		DSPL =4 LOAD A REGISTER WITH FFFFFFF3 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL -> RIM
16	60		DSPL =37777777773 LOAD A REGISTER WITH F COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSHD DSPL ->

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				RIM
16	61		DSPL =2 LOAD A REGISTER WITH FFFFFFF9 COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKO DSPL -> RIM
16	62		DSPL =37777777775 LOAD A REGISTER WITH F COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKO DSPL -> RIM
16	63		DSPL =1 LOAD A REGISTER WITH FFFFFFFC COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKO DSPL -> RIM
16	64		DSPL =37777777776 LOAD A REGISTER WITH F COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB77F0B8F	CREG->ROM, ROM->DSPL, DSPL->INMX, MSKO DSPL -> RIM
16	65		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
*****************************************************************************************************
*                                                                                                   *
*                        CIU POSFIX PULSE TESTS, GTC001* -> QUU001* => POSFIX PULSE                 *
*                                                                                                   *
*                                              MAJOR 17                                             *
*                                                                                                   *
*                                        1. CLK RUN TAPE STOP TESTS                                 *
*                                        2. POSFIX ERROR STOP TESTS                                 *
*                                        3. POSFIX PULSE WIDTH TESTS                                *
*                                        4. CONDITIONAL CLK RUN TESTS                               *
*                    THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99                  *
*                                                                                                   *
*****************************************************************************************************

17 00                       DEFINE SELF TEST TAPE
                            SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                              (GTC003*)
                            ENABLE LOW LEVEL ON GTC001*

*****************************************************************************************************
*                                                                                                   *
*                                        CLK RUN TAPE STOP TESTS                                    *
*                                                                                                   *
*****************************************************************************************************

17 01                       INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFE0FFF      CLK RUN TAPE STOP
                            ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001*
                            BRANCH TO MAJOR 17 MINOR 3

17 02   2      F30.1    AUTO SECTION FAULT LOC - FAULT IN 3SB OF MARC
                          STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

                          | INDICATORS | DISPLAY | REPLACE ASSEMBLIES |
                          | NO-GO      | BLANK   | 1A1A1A1(21,22)     |

17 03                       INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFE0FFF      CLK RUN TAPE STOP
                            ENABLE CONTROLLED TIMING PULSE INTERVAL 10 CONDITIONALLY ON GTC001*
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** POSFIX ERROR STOP TESTS **********	
17 04			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 2 CONDITIONALLY ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK
17 05			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 999 CONDITIONALLY ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK
17 06			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK PULSE WIDTH ALMOST SHORT ENOUGH
			********** POSFIX PULSE WIDTH TESTS **********	
17 07			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 3 CONDITIONALLY ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK PULSE WIDTH ALMOST LONG ENOUGH
17 08			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 4 CONDITIONALLY ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK PULSE WIDTH ALMOST TOO SHORT
17 09			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFEOF7F ENABLE CONTROLLED TIMING PULSE INTERVAL 9 ON GTC001*	CLK RUN TAPE STOP, POSFIX PULSE CHECK PULSE WIDTH ALMOST TOO LONG

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** CONDITIONAL CLK RUN TESTS **********	
17	10		SERIALLY LOAD THE B REGISTER WITH A03 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4FBFFE077F ENABLE CONTROLLED TIMING PULSE INTERVAL 16 CONDITIONALLY ON GTC001*	ROM->CM*DR, CLK RUN TAPE STOP, BREG->ROM,POSFIX PLS CH
17	11		SERIALLY LOAD THE B REGISTER WITH A03 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4FBFFE077F ENABLE CONTROLLED TIMING PULSE INTERVAL 12 CONDITIONALLY ON GTC001*	ROM->CM*DR, CLK RUN TAPE STOP, BREG->ROM,POSFIX PLS CH
17	12		ENABLE VERTICAL PARITY CHECK	
17	13		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** EIP/EOP MANUAL TESTS (FAULT ISOLATION) MAJOR 18 **********	
			* 1. (EOP) PJB--->B, STOP, DISPLAY B - NO GO	
			* 2. (EOP) PJB--->B, DISPLAY B - STOP	
			* 3. (EOP) PJB--->B, STOP, ENABLE ANALOG CONTROL WORD, 4.7VDC	
			* 4. (EOP) BLANK ANALOG CONTROL WORD	
18	00		DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001*	
18	01		SERIALLY LOAD THE B REGISTER WITH A029CBB8 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF0FFF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3B200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3B00	ROM->W1 DR EA =354 OCTAL EOP PJB->B, STOP, DSPL B, NO-GO
18	02		SERIALLY LOAD THE B REGISTER WITH A7D63447 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF0FFF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3B600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3B400	ROM->W1 DR EA =355 OCTAL EOP PJB->B, STOP, DSPL B
18	03		LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 SERIALLY LOAD THE B REGISTER WITH A3E8 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF07FF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABF7FFFF	I/O REQ INACTIVE SET UP EA=372 OCTAL TO BE LOADED BREG->DIHR ON LDSI ROM->WD1 DR, BREG->ROM EOP PJB->B, STOP, EN ANALOG CONTROL WD- DATA TRANS= AREG->ROM->WD1* DR->PJP REC->BREG->ANALOG CONTROL WORD =4080 = 10VDC TEST
18	04		LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3EE00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3EC00 STOP TAPE	EA=373 OCTAL EOP BLANK ANALOG CONTROL WORD

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
18 05			ENABLE VERTICAL PARITY CHECK	
18 06			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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*****************************************************************************************************
*                                                                                                   *
*                                        ISOLATE FAULT IN TST2                                      *
*                                     MINORS 3 - 37 TESTS (00)T3.6.NN                               *
*                                MINORS 50 - 73 EXTENSION OF INITIAL CONFIDENCE TESTS               *
*                                                                                                   *
*****************************************************************************************************
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19 00 2 F30.2
F72.1 FAULT IN 3SB OF MABC, OR BBC536* INPUT TO MBC061 S@1

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SEL FAULT	21000000000011A1A1A121,221	

```
                    PUNCH TAPE LEADER 12 INCHES LONG

                  INITIALIZE
                    DEFINE SELF TEST TAPE
                    ENABLE LOW LEVEL ON GTC001*
                    BRANCH TO MAJOR 19 MINOR 50

19 01               STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
19 02               STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

19 03  4  (00)T3.6.N  TEST FOR RESET OF TST2(SIM NO-GO) ON CMA121 OR KTL501 WITH NO EN OF
                    CMA121 OR KTL501
19 04               SERIALLY LOAD THE B REGISTER WITH AAAAAAAA
                    INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF014FFF      RESET SIM NO-GO ON CMA121 OR
                                                                                            KTL501
                    BRANCH TO MAJOR 19 MINOR 22 ON NO-GO                                   NO-GO = PASS

19 05  5  T3.6.NNG  TEST RESET OF TST2(SIM NO-GO) WITH NO MEM LD BREG CONTROL EN
                    SET THE I/O COMPLETE FLAG (GTC010*)                                    RESET TST2
                    RESET THE I/O COMPLETE FLAG (GTC010*)
                    INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F014FFF      SIM NO-GO, INH ALL MEM EN
                    BRANCH TO MAJOR 19 MINOR 6  ON NO-GO.                                  NO-GO = PASS
                    BRANCH TO MAJOR 19 MINOR 7

19 06  6  T3.6.NNGN  FAULT IN CMA121 OR KTL501, ACTIVE => RESET TST2
                    ENABLE VERTICAL PARITY CHECK
                    STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
19 07 19 08	6	T3.6.NNGG	TEST FOR LOAD OF BREG WITH NO MEM LD BREG EN SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F014FFF COMPARE THE E REGISTER TO THE A REGISTER BRANCH TO MAJOR 19 MINOR 9 ON NO-GO BRANCH TO MAJOR 19 MINOR 13	SIM NO-GO, INH ALL MEM EN
19 09	7	F3.6.NNGGN	FAULT IN RESET OF TST2 & SELF TEST LOAD OF BREG ACTIVE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE VERTICAL PARITY CHECK ENABLE THE A REGISTER TO THE QJD LINES STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	WILL CAUSE TEST SET FAULT UNLESS ARQ052* IS ACTIVE
			INDICATORS: TEST SET FAULT — DISPLAY: 10000 — REPLACE ASSEMBLIES: 1A1A2A21; 1A1A3A(15,20); 2A1A3A16	AYR732* ACTIVE
			INDICATORS: NO GO — DISPLAY: 25252525252 — REPLACE ASSEMBLIES: 2A1A2A13	ARQ052* ACTIVE
19 10			SPARE	
19 11			SPARE	
19 12			SPARE	
19 13	7	F3.6.NNGGG	NOT A NORMAL FAULT LOC - WITH INH ALL MEM EN, RESET TST2 BUT NO LD BREG - WITH ALL MEM EN, LD BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(11,19,21); 1A1A3A(1,2); 2A1A3A(15,16)	
19 14			SPARE	
19 15			SPARE	
19 16			SPARE	
19 17			SPARE	
19 18			SPARE	
19 19			SPARE	
19 20			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
19 21				
19 22	5	T3.6.NNN	TEST FOR RESET OF TST2(SIM NO-GO) ON KMA121 OR ATL421* ACTIVE	
19 23			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F8F4FFF	RESET TST2 ON KMA121
			BRANCH TO MAJOR 19 MINOR 28 ON NO-GO	
19 24	6	F3.6.NNNG	ATL421* OR KMA121 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(11,19,21) 1A1A3A(1,3,20)	
19 25			SPARE	
19 26			SPARE	
19 27			SPARE	
19 28	6	T3.6.NNNN	TEST FOR RESET OF TST2(SIM NO-GO) ON KMA051	
19 29			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F4F4FFF	RESET TST2 ON KMA051
			BRANCH TO MAJOR 19 MINOR 34 ON NO-GO	NO-GO = PASS
19 30	7	F3.6.NNNNG	KMA051 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(1,2,20)	
19 31			SPARE	
19 32			SPARE	
19 33			SPARE	
19 34	7	T3.6.NNNNN	TEST FOR RESET OF TST2(SIM NO-GO) ON KMA061	
19 35			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F2F4FFF	RESET TST2 ON KMA061
			BRANCH TO MAJOR 19 MINOR 37 ON NO-GO	NO-GO = PASS
19 36	8	F3.6.NNNNN		
		--->G	KMA061 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A3A(1,20)	
19 37	8	F3.6.NNNNN --->N	NOT A NORMAL FAULT LOC - SIM NO-GO RESET AT MAJ 0 MIN 1, BUT NOT IN MAJ 19ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(14,15,16); 2A1A2A(1,2,13)	
19 38			SPARE	
19 39			SPARE	
19 40			SPARE	
19 41			SPARE	
19 42			SPARE	
19 43			SPARE	
19 44			SPARE	
19 45			SPARE	
19 46			SPARE	
19 47			SPARE	
19 48			SPARE	
19 49			SPARE	
19 50 19 51			TEST FOR PREMATURE RESET OF TST1 SERIALLY LOAD THE B REGISTER WITH A LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 19 MINOR 52 ON NO-GO BRANCH TO MAJOR 19 MINOR 58	ROM -> RIM
19 52 19 53			TEST I/O CMPLT -> MTW1, GTC010* -> OUT009 READ & COMPARE MISCELLANEOUS WORD 1 WITH A008 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 19 MINOR 54 ON NO-GO	
			FAULT IN AYR714* OR AYC003* ENABLE VERTICAL PARITY CHECK SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) PUNCH TAPE CODES - /B /4 #F #F #F &C RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RCNU FFF

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 2A1A2A20	GYR707 Sa1
			INDICATORS: TEST SET FAULT — REPLACE ASSEMBLIES: 2A1A3A(12,15,16)	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A04	GPE123* Sa0
			INDICATORS: NO GO — REPLACE ASSEMBLIES: 1A1A3A09	
19 54			FAULT = I/O CMPLT ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 2A1A2A(2,12,17,18)	CEC499* Sa0
19 55			SPARE	
19 56			SPARE	
19 57			SPARE	
19 58			TEST FOR NO "MODE 2 CLK EN"	
19 59			LOAD A REGISTER WITH 060 INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. BRANCH TO MAJOR 19 MINOR 65	
19 60			AYR712 Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A(15,16)	
19 61			SPARE	
19 62			SPARE	
19 63			SPARE	
19 64			SPARE	
19 65			TEST FOR NO TST2	
19 66			SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) LOAD A REGISTER WITH 073 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 069FFF0FFF BRANCH TO ADDRESS LOCATION IN A REGISTER	RESET TST2 SET UP ADDR = 73 TO BRANCH TO IF TST2 LOADS STREG THREE MSHD = BRANCH ADDR = 69 WILL BR TO 73 IF STREG LD, 69 IF NO TST2
19 67			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
19 68			SPARE	
19 69			FAULT IN TST2 IBT OR FF ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A02, 2A1A3A15	KYR702* S@1
19 70			SPARE	
19 71			SPARE	
19 72			SPARE	
19 73			FAULT IN AYR752 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(15,16)	
19 74			SPARE	
19 75			SPARE	
19 76			SPARE	
19 77			SPARE	
19 78			SPARE	
19 79			SPARE	
19 80			SPARE	
19 81			SPARE	
19 82			SPARE	
19 83			SPARE	
19 84			SPARE	
19 85			SPARE	
19 86			SPARE	
19 87			SPARE	
19 88			SPARE	
19 89			SPARE	
19 90			SPARE	
19 91			SPARE	
19 92			SPARE	
19 93			SPARE	
19 94			SPARE	
19 95			SPARE	
19 96			SPARE	
19 97			SPARE	
19 98			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK	
19 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
20 00			BRANCH TO MAJOR 20 MINOR 3	
20 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
20 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
20 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
*****************************************************************************************************
*                                                                                                   *
*                                INTERNAL MULTIPLEXER TESTS- MAJORS 21 AND 22                       *
*                          TEST OF CMAB,AANC, LDAB FUNCTIONS- MINORS 3 THRU 44 OF MAJ 21            *
*                                                                                                   *
*                                                                                                   *
*****************************************************************************************************
```

```
21 00                       INITIALIZE
                              DEFINE SELF TEST TAPE
                              ENABLE LOW LEVEL ON GTC001*
                              BRANCH TO MAJOR 21 MINOR 2

21 01                         STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

```
*****************************************************************************************************
*                                                                                                   *
*                                          TEST OF CMAB, LDAB, AANC                                 *
*                                                                                                   *
*****************************************************************************************************
```

```
21 02   1      T35          TEST CMAB WITH AREG NOT= BREG => NO-GO
                            PREVIOUS TEST = (37)T31
21 03                         INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FF7      PJB -> RIM, => B REG =
                                                                                                      AFFFFFFF
                              COMPARE THE B REGISTER TO ADF00001                                     CREG = 020FFFFE IF NO FAULT

        2      F35.1        FAULT LOC WITHIN TEST T35 - FAULT IN CMAB LOGIC
```

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SET FAULT	60000[2A1A1A(13,14)	
TEST SET FAULT	60001[2A1A1A(2,5,6,10,14,15)	
TEST SET FAULT	40001[2A1A1A(4,10,11,12,14,15	
TEST SET FAULT	20001PROCEED PER PARAGRAPH 3-12D	

```
        1      T35(CONT)      BRANCH TO MAJOR 21 MINOR 8  ON NO-GO

        2      T35.2        TEST RCPJ, AREG NOT= BREG => NO-GO
                              READ & COMPARE PJB LINES WITH A0000000                                 CREG = OFFFFFFF IF NO FAULT

        3      F35.2.1      FAULT LOC WITHIN TEST T35.2 - FAULT IN CLK TO AREG & BREG DURING COMPARE
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT / DISPLAY: 6000 / REPLACE ASSEMBLIES: 2A1A1A04	
	2	T35.2 (CONT)	BRANCH TO MAJOR 21 MINOR 5 ON NO-GO	
21 04	3	F35.2.2	FAULT IN CMAB => NO GO COMPARE THE B REGISTER TO 00000000 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	AREG SAT IF AAR045* NOT S@1
			INDICATORS: TEST SET FAULT / DISPLAY: 4000 / REPLACE ASSEMBLIES: 2A1A1A14, 2A1A2A06	NO BRANCH ON NO-GO FLAG, KAT041* S@1
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A01	CAR035 S@0
21 05	3	F35.2.3	FAULT AT CMAB IBT, LATCH, OR INPUT TO IAR026* STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1777777777 / REPLACE ASSEMBLIES: 2A1A1A(1,2), 2A1A2A06	
21 06			SPARE	
21 07			SPARE	
21 08	1	T36	TEST LDAB	
21 09			SERIALLY LOAD THE B REGISTER WITH 0AAAAAAA	
	2	F36.1	FAULT LOC WITHIN TEST T36 - FAULT IN RESET OF NO-GO FLAG	
			INDICATORS: TEST SET FAULT / DISPLAY: 600001 / REPLACE ASSEMBLIES: 2A1A1A(13,14)	IAT144* OR IAT044* S@1
	1	T36(CONT)	COMPARE THE B REGISTER TO AAAAAAAA BRANCH TO MAJOR 21 MINOR 11 ON NO-GO BRANCH TO MAJOR 21 MINOR 17	
21 10			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
21 11 21 12	2	T36.N	CHECK FOR NO "A->B SHIFT CONTROL" SERIALLY LOAD THE B REGISTER WITH AAAAAAAA COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 21 MINOR 14 ON NO-GO	
	3	T36.NG	ISOLATE BETWEEN "A->B SHIFT CONTROL" & "TRANS A->B *" LOAD A REGISTER WITH 0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F SERIALLY LOAD THE B REGISTER FROM THE A REGISTER COMPARE THE B REGISTER TO AAFFFFFF BRANCH TO MAJOR 21 MINOR 16 ON NO-GO	ROM -> RIM
	4	F36.NGG	FAULT IN "TRANS A->B" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	BLANK	2A1A1A(3,4)	ARK021* S@1 OR INPUT TO CRK035 S@1

21 13			SPARE	
21 14	3	F36.NN	FAULT IN "A->B CMPLT", INPUT TO CRK034, SERIAL INPUT TO BREG, OR MSHD OR RIM STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	24525252525	2A1A1A(3,4) 2A1A2A(20,26)	ARK121* OR AAB313* INACTIVE
NO GO	20525252525	2A1A2A01	CAB013
NO GO	10525252525	2A1A2A20	AAB014
NO GO	4525252525	2A1A2A(20,25)	IAB015
NO GO	2525252525	2A1A2A25	IAB016
NO GO	1777777777	2A1A1A(3,20)	CRK034 INACTIVE OR IRB131 INACTIVE
NO GO	525252525	1A1A3A(4,5,16) 2A1A2A19	AYR648 S@1

21 15			SPARE	
21 16	4	F36.NGN	FAULT IN A->B SHIFT CONTROL STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 240000000000 — REPLACE ASSEMBLIES: 2A1A1A03	BAR032 INACTIVE
21 17 21 18	1	T37	TEST FOR NO INH OF B REG END AROUND SERIALLY LOAD THE B REGISTER WITH A5555555 COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 21 MINOR 19 ON NO-GO BRANCH TO MAJOR 21 MINOR 20	
21 19	2	F37.N	NO INH OF B REC END AROUND SHIFT STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 177777777772 — REPLACE ASSEMBLIES: 2A1A1A20	IRB133* S@1
21 20 21 21	1	38	TEST AANC RESET OF TST2 (SIM NO-GO) INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF LOGICALLY 'AND' C REGISTER AND 00000000 - RESULT IN B & C REGISTER	SIM NO-GO
	2	F38.1	FAULT LOC WITHIN TEST T38 (NOT A PROGRAMMED STOP)- ERROR IN AANC FUNC	
			INDICATORS: TEST SET FAULT — DISPLAY: 600002 — REPLACE ASSEMBLIES: 2A1A1A14	
	1	T38(CONT)	BRANCH TO MAJOR 21 MINOR 23 ON NO-GO	
	2	F38.2	FAULT LOC WITHIN TEST T38 (NOT A PROGRAMMED STOP)- AANC NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 100002 — REPLACE ASSEMBLIES: 2A1A1A02	INPUT TO AAR023* OPEN
	1	T38(CONT)	BRANCH TO MAJOR 21 MINOR 26	
21 22			SPARE	
21 23	2	F38.3	FAULT IN AANC IBT, LATCH, OR INPUT TO AAR016 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFF0F7F COMPARE THE B REGISTER TO THE A REGISTER INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF07FF STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	ROM -> RIM B REG -> ROM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / BLANK / 2A1A1A02	AANC IBT OR LATCH
			NO GO / 24000000 / 2A1A1A02	INPUT TO AAR016 Sa1
21 24			SPARE	
21 25				
21 26	1	T39	TEST AANC DATA RESULT (A REG).(C REG)->C REG ALSO ->B REG + A0000000	
21 27			SERIALLY LOAD THE B REGISTER WITH A5555555	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM, WILL CHANGE HEX A IN MSD IF CCBT LOADS MSD
			COMPARE THE B REGISTER TO F0000FFF	RESULT IN C REG = 5555AAAA
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM, WILL CHANGE HEX A IN MSD IF CCBT LOADS MSD
			COMPARE THE B REGISTER TO THE A REGISTER	RESULT IN C REG = 5555AAAA
	2	T39.1	FAULT LOCATION WITHIN TEST T39 (NOT A PROGRAMMED STOP)- CAN NOT SHIFT END AROUND	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			TEST SET FAULT / 4000 / 2A1A1A12	
			TEST SET FAULT / 2000 / PROCEED PER PARAGRAPH 3-12D	FAULT IN B REG END AROUND CR INH ACTIVE
			TEST SET FAULT / 60000 / 2A1A1A14	
	1	T39(CONT)	LOGICALLY 'AND' C REGISTER AND 5AAA555D - RESULT IN B & C REGISTER	RESULT IN C REG = 50000008 IF NO FAULT
			BRANCH TO MAJOR 21 MINOR 29 ON NO-GO	
	2	F39.G	FAULT IN C REG,OR AANC SHIFT CONTROL,OR OPEN INPUT TO AAR033* OR BAR042*	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / BLANK / 2A1A1A(2,3,8,9)	C REG OR C REG CLK
			NO GO / 125253252 / 2A1A1A04	ARK112* Sa1
21 28	2	F35.3	FAULT IN PARTIAL CREG->ROM ENABLE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 203777776 — REPLACE ASSEMBLIES: 12A1A1A19	
21 29 21 30	2	T40	TEST FOR OPEN INPUT TO AAR033* OR BAR042* LOGICALLY 'AND' C REGISTER AND 10000000 - RESULT IN B & C REGISTER BRANCH TO MAJOR 21 MINOR 32 ON NO-GO	
	2	F40.G	FAULT AT GATE AAR033* OR BAR042* STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 12A1A1A(2,3)	
21 31			SPARE	
21 32 21 33	1	T41	TEST AANC CMPLT => LOAD HEX A INTO MSD OF B REG SERIALLY LOAD THE B REGISTER WITH A5555555 COMPARE THE B REGISTER TO 55A5A5A5 LOGICALLY 'AND' C REGISTER AND 5FAF5FAF - RESULT IN B & C REGISTER COMPARE THE B REGISTER TO A0A050A0 BRANCH TO MAJOR 21 MINOR 35 ON NO-GO BRANCH TO MAJOR 21 MINOR 37	RESULT IN C REG = F0F0F0F0
21 34			SPARE	
21 35	2	F41.N	FAULT IN AANC CMPLT OR C REG OR B REG CLK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 2400000000012 — REPLACE ASSEMBLIES: 12A1A1A02	AAR033* Sa1
			INDICATORS: NO GO — DISPLAY: 5751027651 — REPLACE ASSEMBLIES: 12A1A1A03	INPUT TO CRK015 Sa1
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 12A1A1A(2,3,8,9)	CREG OR CLK
21 36			SPARE	
21 37 21 38	1	T42	TEST "CLEAR A REG #1" SERIALLY LOAD THE B REGISTER WITH A0000000 LOAD A REGISTER WITH A5555555 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 21 MINOR 40 ON NO-GO BRANCH TO MAJOR 21 MINOR 45	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
21 39			SPARE	
21 40	2	T42.N	CHECK "CLEAR A REG #3"WITH EIP A->EB, TAPE	
21 41			INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG.	NO ACTIVE BITS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A88600	SET UP EA = 1341
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A88400	ENABLE I/O CMPLT
			LOAD A REGISTER WITH 05555555	
			LOAD EIP DATA FIELD 0 INTO A REGISTER	
			COMPARE THE B REGISTER TO OFFFFFFF	
			BRANCH TO MAJOR 21 MINOR 43 ON NO-GO	
	3	F42.NG	FAULT IN CLEAR A REG #1 OR CLEAR OF MSHD	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 12252525 — REPLACE ASSEMBLIES: 2A1A1A02, 2A1A2A17	IAR046* Sa1
			INDICATORS: NO GO — DISPLAY: 120000000 — REPLACE ASSEMBLIES: 2A1A1A17	INPUT TO ARA074 Sa1
21 42			SPARE	
21 43	3	F42.NN	FAULT IN CLEAR A REG	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 25252525 — REPLACE ASSEMBLIES: 1A1A1A04, 2A1A1A17, 2A1A2A(16,17,18)	IAR067* Sa1
			INDICATORS: NO GO — DISPLAY: 2400000012 — REPLACE ASSEMBLIES: 2A1A1A12	A REG
			INDICATORS: NO GO — DISPLAY: 1200000 — REPLACE ASSEMBLIES: 2A1A1A12	A REG
			INDICATORS: NO GO — DISPLAY: 500000 — REPLACE ASSEMBLIES: 2A1A1A12	A REG
			INDICATORS: NO GO — DISPLAY: 2400 — REPLACE ASSEMBLIES: 2A1A1A11	A REG
			INDICATORS: NO GO — DISPLAY: 120 — REPLACE ASSEMBLIES: 2A1A1A11	A REG
			INDICATORS: NO GO — DISPLAY: 5 — REPLACE ASSEMBLIES: 2A1A1A11	A REG

****

*

* TEST FOR ACTIVE RECEIVERS, ACTIVE INPUT BIT TO B REG OR FAULT IN PE *

*

****

21 44			SPARE	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
21 45 21 46	1	T43	TEST FOR ACTIVE B REG PE DURING TST2(INACTIVEI SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFLOFFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 21 MINOR 48 ON NO-GO BRANCH TO MAJOR 21 MINOR 63	ALL MEMORY EN ACTIVE
21 47			SPARE	
21 48 21 49	2	T43.N	CHECK MEMORY EN #5 SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF3FlFOFFF COMPARE THE P QEGISTER TO THE A RFGISTER BRANCH TO MAJOR 21 MINOR 51 ON NO-GO	MEM EN U5
	3	T43.NG	CHECK MEMORY EN 96 SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF3FD70FFF COMPARE THE B PEGISTER TO THE A REGISTER BRANCH TO MAJOR 21 MINOR 52 ON NO-GO	MEM EN #5
	4	T43.NGG	CHECK MEMORY EN 47 SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF3FOBOFFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 21 MINOR 61 ON NO-GO	MEM EN #7
	5	F43..NGGG	FAULT IN MEMORY CONTROL- STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	MEMORY EN #8

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO.GO	1525252525	1A1A3A(7.8)

IMV061 S@1

21 50			SPARE	
21 51	3	F41.NN	FAULT IN MEMORY CONTROL- STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	MEMORY EN #5

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO.GO	1525252525	1A1A3A(3*8*19*20)

21	52	4	T43.NGN	TEST FOR ACTIVE PE IN NCU CLOCK MODE AND MEMORY EN #6	
21	53			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*)	ACTIVATE BKFO46* ANO IK4037
				SFRIALLY LOAD THE B REGISTER WITH AAAAAAAA	
				INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF3FO7OFFF	MEN EN #6
				COMPARE THE B REGISTER TO THE A REGISTER	
				BRANCH TO MAJOR 21 MINOR 55 ON NO-GO	
				BRAMCH TO MAJOD 21 MINOR 63	
21	54			SPARE	
21	55	5	T43.NGNN	ATTEMPT SET OF "CLOCK CONTROL FF	
21	56			ENABLE CONTINUOS HIGH LEVEL ON GTCOO1*	GTCOO1* INACTIVE
				READ S COMPARE MISCELLANEOUS WORD I WITH AOOOOOC	
				LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	
				BRANCH TO MAJOR 21 MINOR 57 ON NO-GO	
		6	T43.NGNNG	RESET GTCOO1* WITH RCNU	
				ENABLE CONTROLI.EO TIMING PULSE INTERVAL 10 ON GTCOOI*	
				REAO & COMPARE MISCELLANEOUS WORD I WITH A	
				LOGICALLY *AND' C REGISTER AND AOOOOOC - RESULT IN B & : REGISTER	
				BRANCH TO MAJOR 21 MINOR 58 ON NO-GO	
		7	F43.NGNNGG	FAULT IN BKBOII	
				STOP TAPE, DISPLAY C REGISTER NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO.GO	BLANK	1A1A3A(7*14*16*20*231)

21	57	6	F43.NG.NNN	FAULT IN KMVO1l ACTIVE	
				STOP TAPE, OISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO.GO	300	1A1A3A(1*2*3*6*8)

21	58	7	F43.NGNNGN	BBK031* INACTIVE	
				STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO.GO	300	1A1A3A(4*7)

21 59 SPARE
21 60 SPARE
21 61 SPARE
21 62 SPARE

21 63 1 TI4
T43.NGNG TEST FOR ACTIVE RECEIVER ENABLE- DRIVERS ALL INACTIVE
21 64 LOAD A REGISTER WITH AFFFFFFF
SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
(GTC003*1
ENABLE CONTINUOUS HIGH LEVEL ON GTCOO1*
INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST RE5. NO REC EN
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 21 MINOR 66 ON NO-SO
ENABLE LOW LEVEL ON GTCOOI*
RESET INHIBIT TNCREMENT CP FLAG & ENABLE SELF TEST CIU :LOCK MODE
(GTC003*)
BRANCH TO MAJOR 21 MINOR 79

21 65 SPARE

21 66 2 T44.N CHECK FOR ROM -> RIM NATA DEPENDENCE
21 67 LOAD A REGISTER WITH AOOOOOOO
INITIATE SELF TEST MODE I-RETAIN PREVIOUS BIT PATTERN IN SELF TEST RE.. NOTHING ACTIVE
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 21 MINOR 68 ON NO-SO

3 F44.NS FAULT ROM -> RIM
LOAD A REGISTER WITH AFFFFFFF
INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG.
COMPARE THE B REGISTER TO A
STOP TAPE, DISPLAY C REGISTER, NO-CO LIGH1 ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	170000000012A1A2A18	
NO GO	7760000012A1A2A18	
NO GO	177600012A1A2A18	
NO GO	37712A1A2A18	
NO GO	100000000012A1A2A25	
NO GO	40000000012A1A2A25	
NO GO	20000000012A1A2A25	
NO GO	10000000012A1A2A25	
NO GO	4000000012A1A2A24	
NO GO	2000000012A1A2A24	
NO GO	1000000012A1A2A24	
NO GO	400000012A1A2A24	
NO GO	200000012A1A2A24	
NO GO	100000012A1A2A24	
NO GO	40000012A1A2A23	
NO GO	20000012A1A2A23	
NO GO	10000012A1A2A23	
NO GO	4000012A1A2A23	
NO GO	2000012A1A2A23	
NO GO	1000012A1A2A23	
NO GO	400012A1A2A22	
NO GO	200012A1A2A22	
NO GO	100012A1A2A22	
NO GO	40012A1A2A22	
NO GO	20012A1A2A22	
NO GO	10012A1A2A22	
NO GO	4012A1A2A21	
NO GO	2012A1A2A21	
NO GO	1012A1A2A21	
NO GO	412A1A2A21	
NO GO	212A1A2A21	
NO GO	112A1A2A21	

21 68 21 69	3	T44.NN	CHECK FOR SINGLE BIT FAULT LOGICALLY 'AND' C REGISTER AND AAAAAAAA - RESULT IN B & C REGISTER BRANCH TO MAJOR 21 MINOR 70 ON NO-GO BRANCH TO MAJOR 21 MINOR 72
21 70 21 71	4	T44.NNN	CHECK FURTHER FOR SINGLE BIT FAULT INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND 55555555 - RESULT IN B & C REGISTER BRANCH TO MAJOR 21 MINOR 73 ON NO-GO
	5	T44.NNNG	CHECK EXMW REC EN INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO A00003 BRANCH TO MAJOR 21 MINOR 72 ON NO-GO

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	6	F44.NNNGG	FAULT IN EXMW REC EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
21 72	6	F44.NNNGN F44.NNG	FAULT IN SINGLE BIT OF INPUT MUX OR RIM INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A(11,12) 2A1A1A16 2A1A2A(19,25)
NO GO	400000000	1A1A4A(11,12) 2A1A1A16 2A1A2A(19,25)
NO GO	200000000	1A1A4A(10,12) 2A1A1A16 2A1A2A(19,25)
NO GO	100000000	1A1A4A(10,12) 2A1A1A16 2A1A2A(19,25)
NO GO	40000000	1A1A4A(10,12) 2A1A1A16 2A1A2A(19,24)
NO GO	20000000	1A1A4A(9,12) 2A1A1A16 2A1A2A(19,24)
NO GO	10000000	1A1A4A(9,12) 2A1A1A16 2A1A2A(19,24)
NO GO	4000000	1A1A4A(9,12) 2A1A1A16 2A1A2A(19,24)
NO GO	2000000	1A1A4A(8,12) 2A1A1A16 2A1A2A(19,24)
NO GO	1000000	1A1A4A(8,12) 2A1A1A16 2A1A2A(19,24)
NO GO	400000	1A1A4A(8,12) 2A1A1A16 2A1A2A(19,23)
NO GO	200000	1A1A4A(7,12) 2A1A1A16 2A1A2A(19,23)

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

TABLE CONTINUED FROM PRECEEDING PAGE

NO GO		100000	1A1A4A(6,7) 2A1A1A15 2A1A2A(16,23)
NO GO		40000	1A1A4A(6,7) 2A1A1A15 2A1A2A(16,23)
NO GO		20000	1A1A4A(5,6) 2A1A1A15 2A1A2A(16,23)
NO GO		10000	1A1A4A(5,6) 2A1A1A15 2A1A2A(16,23)
NO GO		4000	1A1A4A(4,6) 2A1A1A15 2A1A2A(22,26)
NO GO		2000	1A1A4A(4,6) 2A1A1A15 2A1A2A(22,26)
NO GO		1000	1A1A4A(4,6) 2A1A1A15 2A1A2A(22,26)
NO GO		400	1A1A4A(3,6) 2A1A1A15 2A1A2A(22,26)
NO GO		200	1A1A4A(3,6) 2A1A1A15 2A1A2A22
NO GO		100	1A1A4A(3,6) 2A1A1A15 2A1A2A22
NO GO		40	1A1A4A(2,6) 2A1A1A15 2A1A2A21
NO GO		20	1A1A4A(2,6) 2A1A1A15 2A1A2A21
NO GO		10	1A1A4A(2,6) 2A1A1A15 2A1A2A21
NO GO		4	1A1A4A(1,6) 2A1A1A15 2A1A2A21
NO GO		2	1A1A4A(1,6) 2A1A1A15 2A1A2A21
NO GO		1	1A1A4A(1,6) 2A1A1A15 2A1A2A21

21 73	5	T44.NNNN	TEST FOR FMB OR *JB FAULT	
21 74			INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO AFFFFFFF	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 21 MINOR 76 ON NO-GO	
	6	T44.NNNNG	ISOLATE BETWEEN FMB AND PJB INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBFFFOFFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 21 MINOR 75 ON NO-GO	EN LOAD XMB
	7	F44.NNNNGG	FAULT IN FMB REC EN STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A20	
21 75	7	F44.NNNNGN	FAULT IN PJB REC EN STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A2A09	
21 76	6	F44.NNNNN	SET UP FAULT BIT PATTERN TO ISOLATE FAULT INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777760 — REPLACE ASSEMBLIES: 1A1A3A21	MA EN
			1A1A4A15	
			NO GO — 7760 — 1A1A4A17	PARTIAL MA EN
			NO GO — 1770000 — 1A1A4A17	PARTIAL MA EN
			NO GO — 1774000000 — 1A1A4A20	TOTAL WD3 EN
			NO GO — 1700000000 — 1A1A4A19	PARTIAL WD3 EN
			NO GO — 7400000000 — 1A1A4A19	PARTIAL WD3 EN
			NO GO — 3143000000 — 2A1A2A(7,9)	DISC OUT EN
			NO GO — 1777777400 — 1A1A4A20	TOTAL MTW1 EN
			NO GO — 1760000000 — 1A1A4A20	PARTIAL MTW1 EN
			NO GO — 1760000001 — 1A1A4A20	PARTIAL MTW1 EN
			NO GO — 1774001 — 1A1A4A20	PARTIAL MTW1 EN
			NO GO — 1777776000 — 2A1A2A(7,9)	MTW2 EN
21 77			SPARE	
21 78			SPARE	
21 79 21 80	1	T45	TEST FOR ACTIVE RECEIVER, ALL DRIVERS ACTIVE LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH FFBFFF8FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 21 MINOR 82 ON NO-GO	ALL DRIVERS ACTIVE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 21 MINOR 98	
21 81			SPARE	
21 82	2	T45.N	CHECK RECEIVERS DRIVEN BY LOAD WD1, ONLY	
21 83			LOAD A REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH BFBFFF0FFF	EN LOAD WD1
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 21 MINOR 84 ON NO-GO	
			BRANCH TO MAJOR 21 MINOR 85	
21 84	3	F44.NN	FAULT IN NAD RECEIVER	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1777777777	1A1A3A(19,21,24) 1A1A4A(16,19)	TOTAL NAD EN
NO GO	1777000000	1A1A4A16	PARTIAL NAD EN
NO GO	777000	1A1A4A16	PARTIAL NAD EN
NO GO	777	1A1A4A16	PARTIAL NAD EN
NO GO	1000000000	1A1A4A11	SINGLE EN INPUT SAL
NO GO	400000000	1A1A4A11	SINGLE EN INPUT SAL
NO GO	200000000	1A1A4A10	SINGLE EN INPUT SAL
NO GO	100000000	1A1A4A10	SINGLE EN INPUT SAL
NO GO	40000000	1A1A4A10	SINGLE EN INPUT SAL
NO GO	20000000	1A1A4A09	SINGLE EN INPUT SAL
NO GO	10000000	1A1A4A09	SINGLE EN INPUT SAL
NO GO	4000000	1A1A4A09	SINGLE EN INPUT SAL
NO GO	2000000	1A1A4A08	SINGLE EN INPUT SAL
NO GO	1000000	1A1A4A08	SINGLE EN INPUT SAL
NO GO	400000	1A1A4A08	SINGLE EN INPUT SAL
NO GO	200000	1A1A4A07	SINGLE EN INPUT SAL
NO GO	100000	1A1A4A07	SINGLE EN INPUT SAL
NO GO	40000	1A1A4A07	SINGLE EN INPUT SAL
NO GO	20000	1A1A4A05	SINGLE EN INPUT SAL
NO GO	10000	1A1A4A05	SINGLE EN INPUT SAL
NO GO	4000	1A1A4A04	SINGLE EN INPUT SAL
NO GO	2000	1A1A4A04	SINGLE EN INPUT SAL
NO GO	1000	1A1A4A04	SINGLE EN INPUT SAL
NO GO	400	1A1A4A03	SINGLE EN INPUT SAL
NO GO	200	1A1A4A03	SINGLE EN INPUT SAL
NO GO	100	1A1A4A03	SINGLE EN INPUT SAL
NO GO	40	1A1A4A02	SINGLE EN INPUT SAL
NO GO	20	1A1A4A02	SINGLE EN INPUT SAL
NO GO	10	1A1A4A02	SINGLE EN INPUT SAL

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO 411A1A4A01	SINGLE EN INPUT S@1
			NO GO 211A1A4A01	SINGLE EN INPUT S@1
			NO GO 111A1A4A01	SINGLE EN INPUT S@1
21 85	3	T45.NG	CHECK RECEIVERS DRIVEN BY CM & QTD	
21 86			LOAD A REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBFFF0FFF	EN LOAD QTM & QTD
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 21 MINOR 87 ON NO-GO	
			BRANCH TO MAJOR 21 MINOR 88	
21 87	4	F45.NGN	FAULT IN EXT MEM OR JCM RECEIVER	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1776000000 — REPLACE ASSEMBLIES: 1A1A3A21, 1A1A4A(15,17)	JCM EN
			NO GO — 1000000000 — 1A1A4A11	SINGLE EN INPUT S@1
			NO GO — 400000000 — 1A1A4A11	SINGLE EN INPUT S@1
			NO GO — 200000000 — 1A1A4A10	SINGLE EN INPUT S@1
			NO GO — 100000000 — 1A1A4A10	SINGLE EN INPUT S@1
			NO GO — 40000000 — 1A1A4A10	SINGLE EN INPUT S@1
			NO GO — 20000000 — 1A1A4A09	SINGLE EN INPUT S@1
			NO GO — 10000000 — 1A1A4A09	SINGLE EN INPUT S@1
			NO GO — 4000000 — 1A1A4A09	SINGLE EN INPUT S@1
			NO GO — 2000000 — 1A1A4A08	SINGLE EN INPUT S@1
			NO GO — 200 — 1A1A4A03	
			NO GO — 100 — 1A1A4A03	SINGLE EN INPUT S@1
			NO GO — 10 — 1A1A4A02	SINGLE EN INPUT S@1
21 88	4	T45.NGG	CHECK RECEIVERS DRIVEN BY MB	
21 89			LOAD A REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2FBFFF0FFF	EN LOAD QTB
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 21 MINOR 90 ON NO-GO	
			BRANCH TO MAJOR 21 MINOR 91	
21 90	5	F45.NGGN	FAULT IN JEB OR WD1 RECEIVER	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A3A(19,21), 1A1A4A(15,19,20)	TOTAL WD1 OR JEB EN
			NO GO — 1777760000 — 1A1A3A16, 1A1A4A(15,18,19)	JCP EN
			TABLE CONTINUED ON FOLLOWING PAGE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO 17700000011A1A4A(17,20)	PARTIAL JCP OR JEB EN
			NO GO 7760000011A1A4A17	PARTIAL JCP OR JEB EN
			NO GO 1740011A1A4A(15,17)	JCI EN
			NO GO 370011A1A4A(15,16)	JCE EN
			NO GO 7011A1A4A(15,16)	JCA EN
			NO GO 7740000011A1A4A20	PARTIAL JEB EN
			NO GO 376000011A1A4A20	PARTIAL JEB EN
			NO GO 17711A1A4A20	PARTIAL JEB EN
			NO GO 1000000000011A1A4A11	SINGLE EN INPUT Sa1
			NO GO 400000000011A1A4A11	SINGLE EN INPUT Sa1
			NO GO 200000000011A1A4A10	SINGLE EN INPUT Sa1
			NO GO 100000000011A1A4A10	SINGLE EN INPUT Sa1
			NO GO 40000000011A1A4A10	SINGLE EN INPUT Sa1
			NO GO 20000000011A1A4A09	SINGLE EN INPUT Sa1
			NO GO 10000000011A1A4A09	SINGLE EN INPUT Sa1
			NO GO 4000000011A1A4A09	SINGLE EN INPUT Sa1
			NO GO 2000000011A1A4A08	SINGLE EN INPUT Sa1
			NO GO 2000000011A1A4A08	SINGLE EN INPUT Sa1
			NO GO 1000000011A1A4A08	SINGLE EN INPUT Sa1
			NO GO 400000011A1A4A08	SINGLE EN INPUT Sa1
			NO GO 200000011A1A4A07	SINGLE EN INPUT Sa1
			NO GO 100000011A1A4A07	SINGLE EN INPUT Sa1
			NO GO 40000011A1A4A07	SINGLE EN INPUT Sa1
			NO GO 20000011A1A4A05	SINGLE EN INPUT Sa1
			NO GO 10000011A1A4A05	SINGLE EN INPUT Sa1
			NO GO 4000011A1A4A04	SINGLE EN INPUT Sa1
			NO GO 2000011A1A4A04	SINGLE EN INPUT Sa1
			NO GO 1000011A1A4A04	SINGLE EN INPUT Sa1
			NO GO 400011A1A4A03	SINGLE EN INPUT Sa1
			NO GO 200011A1A4A03	SINGLE EN INPUT Sa1
			NO GO 100011A1A4A03	SINGLE EN INPUT Sa1
			NO GO 40011A1A4A02	SINGLE EN INPUT Sa1
			NO GO 20011A1A4A02	SINGLE EN INPUT Sa1
			NO GO 10011A1A4A02	SINGLE EN INPUT Sa1
			NO GO 4011A1A4A01	SINGLE EN INPUT Sa1
			NO GO 2011A1A4A01	SINGLE EN INPUT Sa1
			NO GO 1011A1A4A01	SINGLE EN INPUT Sa1
21 91 21 92	5	T45.NGGG	CHECK RECEIVERS DRIVEN BY XMB DRIVERS LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBFFF0FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 21 MINOR 93 ON NO-GO BRANCH TO MAJOR 21 MINOR 94	EN LOAD XMB
21 93	6	F45.NGGGN	FAULT IN XMB RECEIVER STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | 1777777777 | 1A1A4A(16,18)	
			NO GO | 1000000001 | 1A1A4A12	SINGLE XMB EN INPUT S@1
			NO GO | XXX0000001 | 1A1A4A12	SINGLE XMB EN INPUT S@1
			NO GO | 400000 | 1A1A4A12	SINGLE XMB EN INPUT S@1
			NO GO | 200000 | 1A1A4A12	SINGLE XMB EN INPUT S@1
			NO GO | 100000 | 1A1A4A06	SINGLE XMB EN INPUT S@1
			NO GO | XXXXX | 1A1A4A06	SINGLE XMB EN INPUT S@1
21 94	6	T45.NGGGG	CHECK RECEIVER DRIVEN BY QJD	
21 95			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFF8FFF	EN LOAD QJD
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 21 MINOR 96 ON NO-GO	
	7	T45.NGGGGG	THIS IS NOT A NORMAL FAULT LOCATION	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | PROCEED PER PARAGRAPH 3-13	
21 96	7	F45.NGGGGN	FAULT IN SINGLE BIT OF EXT MEM RECEIVER	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | 4 | 1A1A4A01	SINGLE EN INPUT S@1
			NO GO | 20 | 1A1A4A02	SINGLE EN INPUT S@1
			NO GO | 40 | 1A1A4A02	SINGLE EN INPUT S@1
21 97			SPARE	
21 98			ENABLE VERTICAL PARITY CHECK	
21 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** INTERNAL MULTIPLEXERS TEST **********	
22 00			INITIALIZE DEFINE SELF TEST TAPE BRANCH TO MAJOR 22 MINOR 3	
22 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
22 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
22 03	2	T48	TEST A REG -> ROM -> RIM -> B REG, DATA = AFFFFFFF	PREVIOUS TEST = (21)T45
22 04			SERIALLY LOAD THE B REGISTER WITH A LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 22 MINOR 6 ON NO-GO BRANCH TO MAJOR 22 MINOR 17	ROM -> RIM
22 05			SPARE	
22 06	2	T48.N	CHECK FOR PARTIAL ROM->RIM EN FAULT	
22 07			COMPARE THE B REGISTER TO AFFFFF00 BRANCH TO MAJOR 22 MINOR 10 ON NO-GO BRANCH TO MAJOR 22 MINOR 14	
22 08			SPARE	
22 09			SPARE	
22 10	4	F48.NN	SINGLE BIT ROM -> RIM INACTIVE LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F COMPARE THE B REGISTER TO THE A REGISTER STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	ROM -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	20000000000	2A1A1A16 2A1A2A01	
NO GO	17000000000	2A1A1A16	BREG PE
NO GO	7400000000	2A1A1A16	BREG PE
NO GO	3600000	2A1A1A16	BREG PE
NO GO	170000	2A1A1A15	BREG PE
NO GO	7400	2A1A1A15	BREG PE
NO GO	360	2A1A1A15	BREG PE
NO GO	17	2A1A1A15	BREG PE
NO GO	10000000000	2A1A1A16 2A1A2A25	
NO GO	X00000000	2A1A1A16 2A1A2A(19,25)	
NO GO	XX000000	2A1A1A16 2A1A2A(19,24)	
NO GO	400000	2A1A1A16 2A1A2A(19,24)	
NO GO	200000	2A1A1A16 2A1A2A(19,24)	
NO GO	100000	2A1A1A15 2A1A2A(23,16)	
NO GO	X0000	2A1A1A15 2A1A2A(23,16)	
NO GO	X000	2A1A1A15 2A1A2A(22,26)	
NO GO	400	2A1A1A15 2A1A2A(22,26)	
NO GO	200	2A1A1A15 2A1A2A22	
NO GO	100	2A1A1A15 2A1A2A22	
NO GO	XX	2A1A1A15 2A1A2A21	

22 11 SPARE
22 12 SPARE

22 13
22 14 4 F48.NG FAULT IN ROM -> RIM EN
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A18	
22 15			SPARE	
22 16			SPARE	
22 17	1	T49	TEST A REG -> ROM -> RIM -> B REG, DATA = 50000000	
22 18			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			LOAD A REGISTER WITH 50000000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO THE A REGISTER	
			BRANCH TO MAJOR 22 MINOR 20 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 22	
22 19			SPARE	
22 20	3	F49.N	FAULT IN ROM -> PIM, BIT Sa1	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000000000C — REPLACE ASSEMBLIES: 2A1A2A(1,20)	
			INDICATORS: NO GO — DISPLAY: 10000000000012A1A2A20	BIT 31 INACTIVE
			INDICATORS: NO GO — DISPLAY: 24000000000012A1A2A(20,26)	
			INDICATORS: NO GO — DISPLAY: 36000000000012A1A2A19	
			INDICATORS: NO GO — DISPLAY: XX000000000012A1A2A25	
			INDICATORS: NO GO — DISPLAY: XX00000012A1A2A24	
			INDICATORS: NO GO — DISPLAY: XX0000012A1A2A23	
			INDICATORS: NO GO — DISPLAY: XX00012A1A2A22	
			INDICATORS: NO GO — DISPLAY: XX12A1A2A21	
22 21			SPARE	
22 22	1	T50	TEST FOR FAULT IN EN B REG OR C REG -> ROM	
22 23			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			COMPARE THE B REGISTER TO F	SET UP ALL ONES IN BIT 1 - 28 OF B & C REG
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO THE A REGISTER	
			BRANCH TO MAJOR 22 MINOR 25 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 27	
22 24			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
22 25	2	F50.N	FAULT IN B OR C -> ROM EN ACTIVE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	170000000012A1A1A19	
NO GO	776000000012A1A1A19	
NO GO	17740012A1A1A19	
NO GO	3771 2A1A1A19	
NO GO	X000000000012A1A1A20	
NO GO	XX00000000012A1A1A21	
NO GO	XX000000012A1A1A24	
NO GO	XX00012A1A1A25	
NO GO	XX012A1A1A28	
NO GO	XX12A1A1A29	

22 26			SPARE	
22 27 22 28	1	T51	TEST B REG -> ROM -> RIM -> B REG, DATA = AFFFFFFF SERIALLY LOAD THE B REGISTER WITH AFFFFFFF LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF077F COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 22 MINOR 32 ON NO-GO BRANCH TO MAJOR 22 MINOR 38	BREG->ROM, ROM->RIM
22 29			SPARE	
22 30			SPARE	
22 31			SPARE	
22 32	2	F51.N	FAULT IN B REG CHAN OF ROM STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	17777777772A1A1A(7,19)	
NO GO	170000000012A1A1A19	
NO GO	776000000 12A1A1A19	
NO GO	17740012A1A1A19	
NO GO	3771 2A1A1A19	
NO GO	X000000000012A1A1A20	
NO GO	XX00000000012A1A1A21	
NO GO	XX000000012A1A1A24	
NO GO	XX00012A1A1A25	

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO | XX00(2A1A1A28	
			NO GO | XX(2A1A1A29	
22 33			SPARE	
22 34			SPARE	
22 35			SPARE	
22 36			SPARE	
22 37			SPARE	
22 38	1	T52	TEST BREG -> ROM -> RIM -> BREG, DATA = 50000000	
22 39			LOAD A REGISTER WITH 50000000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F	ROM->RIM
			LOAD A REGISTER WITH 5FFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF077F	BREG->ROM, ROM->RIM
			COMPARE THE B REGISTER TO 5	
			BRANCH TO MAJOR 22 MINOR 40 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 47	
22 40	2	T52.N	TEST FOR NO INH OF AREG -> ROM	
22 41			COMPARE THE B REGISTER TO 5FFFFFFF	
			BRANCH TO MAJOR 22 MINOR 42 ON NO-GO	
	3	F52.NG	FAULT IN INH OF AREG -> ROM	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | 2A1A1A19	
22 42	3	F52.NN	FAULT IN BREG -> ROM, BIT SA1, OR PARTIAL AREG -> ROM EN SA1	
			COMPARE THE B REGISTER TO 5	SET UP FAULT BIT
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | X0000000000(2A1A1A(16,20)	
			NO GO | XX000000000(2A1A1A(16,21)	
			NO GO | XX0000000(2A1A1A(16,24)	
			NO GO | 400000(2A1A1A(16,25)	
			NO GO | 200000(2A1A1A(16,25)	
			NO GO | 100000(2A1A1A(15,25)	
			NO GO | X0000(2A1A1A(15,25)	
			NO GO | XX00(2A1A1A(15,28)	
			TABLE CONTINUED ON FOLLOWING PAGE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO — XX12A1A1A(15,29)	
			NO GO — 17000000000 12A1A1A19	EN AREG->ROM Sa1
			NO GO — 77600000 1A1A1A19	EN AREG->ROM Sa1
			NO GO — 17740012A1A1A19	EN AREG->ROM Sa1
			NO GO — 3771 2A1A1A19	EN AREG->ROM Sa1
22 43			SPARE	
22 44			SPARE	
22 45			SPARE	
22 46			SPARE	
22 47	1	T53	TEST C REG -> ROM -> RIM -> B REG, DATA = AFFFFFFF	
22 48			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			COMPARE THE B REGISTER TO 05555555	C = AFFFFFFF
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOB7F	C REG -> ROM, ROM->RIM
			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 22 MINOR 52 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 55	
22 49			SPARE	
22 50			SPARE	
22 51			SPARE	
22 52	2	F53.N	FAULT IN C REG CHAN OF ROM	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS — DISPLAY — REPLACE ASSEMBLIES	
			NO GO — 25252525252 12A1A1A19	
			NO GO — 17000000000 12A1A1A19	
			NO GO — 77600000 12A1A1A19	
			NO GO — 17740012A1A1A19	
			NO GO — 3771 2A1A1A19	
			NO GO — X0000000000 12A1A1A20	
			NO GO — XX000000000 12A1A1A21	
			NO GO — XX00000012A1A1A24	
			NO GO — XX00012A1A1A25	
			NO GO — XX0012A1A1A28	
			NO GO — XX12A1A1A29	
22 53			SPARE	
22 54			SPARE	
22 55	1	T54	TEST C REG -> ROM -> RIM -> B REG, DATA = 50000000	
22 56			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			COMPARE THE B REGISTER TO FAAAAAAA	C-REG = 50000000
			LOAD A REGISTER WITH 5FFFFFFF	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0B7F COMPARE THE B REGISTER TO 5 BRANCH TO MAJOR 22 MINOR 57 ON NO-GO BRANCH TO MAJOR 22 MINOR 64	C REG -> ROM, ROM->RIM
22 57 22 58	2	T54.N	TEST FOR NO INH OF AREG -> ROM COMPARE THE B REGISTER TO 5FFFFFFF BRANCH TO MAJOR 22 MINOR 60 ON NO-GO	
	3	F54.NG	FAULT IN INH OF AREG -> ROM ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
22 59			SPARE	
22 60	3	F54.NN	FAULT IN C REG -> ROM, BIT S@1 COMPARE THE B REGISTER TO 5 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	SET UP FAULT BIT
22 61			SPARE	
22 62			SPARE	
22 63			SPARE	
22 64 22 65	1	T55	TEST A REG -> ROM -> DSPL -> IN MUX -> RIM + MSHD DSPL -> B REG, DATA = AFFFFFFF LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0F8F COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 22 MINOR 70 ON NO-GO BRANCH TO MAJOR 22 MINOR 76	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	X0000000000	2A1A1A1A(8,20)
NO GO	XX000000000	2A1A1A1A(8,21)
NO GO	XX0000000	2A1A1A1A(8,24)
NO GO	4000000	2A1A1A1A(8,25)
NO GO	2000000	2A1A1A1A(8,25)
NO GO	1000000	2A1A1A1A(9,25)
NO GO	X000000	2A1A1A1A(9,25)
NO GO	XX00	2A1A1A1A(9,28)
NO GO	XX	2A1A1A1A(9,29)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
22 66			SPARE	
22 67			SPARE	
22 68			SPARE	
22 69			SPARE	
22 70	2	F55.N	FAULT IN DSPL -> IN MUX OR 4MSB DSPL -> RIM, BIT S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	17777777771	1A1A2A21	EN DSPL -> IN MUX INACTIVE
		11A1A4A18	
NO GO	12400000000012	A1A2A20	AAX017 S@0
NO GO	12000000000012	A1A2A(1,20)	
NO GO	11000000000012	A1A2A20	RIM BIT S@1
NO GO	10400000000012	A1A2A25	RIM BIT S@0
NO GO	10200000000012	A1A2A25	RIM BIT S@1
NO GO	10100000000011	A1A4A11	
NO GO	10040000000011	A1A4A11	
NO GO	10020000000011	A1A4A(10,12)	
NO GO	10010000000011	A1A4A10	
NO GO	10004000000011	A1A4A10	
NO GO	10002000000011	A1A4A(9,12)	
NO GO	10001000000011	A1A4A09	
NO GO	10000400000011	A1A4A09	
NO GO	10000200000011	A1A4A(8,12)	
NO GO	10000100000011	A1A4A08	
NO GO	10000040000011	A1A4A08	
NO GO	10000020000011	A1A4A(7,12)	
NO GO	10000010000011	A1A4A07	
NO GO	10000004000011	A1A4A07	
NO GO	10000002000011	A1A4A05	
NO GO	10000001000011	A1A4A05	
NO GO	10000000400011	A1A4A(5,6)	
NO GO	10000000200011	A1A4A04	
NO GO	10000000100011	A1A4A04	
NO GO	10000000040011	A1A4A(3,6)	
NO GO	10000000020011	A1A4A03	
NO GO	10000000010011	A1A4A03	
NO GO	10000000004011	A1A4A(2,6)	
NO GO	10000000002011	A1A4A02	
NO GO	10000000001011	A1A4A02	
NO GO	10000000000411	A1A4A(1,6)	
NO GO	10000000000211	A1A4A01	
NO GO	10000000000111	A1A4A01	

22 71			SPARE	
22 72			SPARE	
22 73			SPARE	
22 74			SPARE	
22 75			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
22 76	1	T56	TEST A->ROM->DSPL->IN MUX OR 4MSB DSPL-> RIM->B, DATA = 50000000	
22 77			LOAD A REGISTER WITH 50000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0FBF	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B PEGISTER TO THE A RFGISTER BRANCH TO MAJOR 22 MINOR 80 ON NO-GO BRANCH TO MAJOR 22 MINOR 85	
22 78			SPARE	
22 79			SPARE .	
22 80	2	T56.N	FAULT IN DSPL CHAN OF IN MUX OR RIM, BIT Sa1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1360000000012A1A1A07		FYR549* Sa1
NO GO	1240000000012A1A2A20		FYR549* INPUT TO AAB313* Sa1
NO GO	1120000000012A1A2A20		AA5215 Sa0
NO GO	1200000000012A1A2A20		RIM BIT Sa1
NO GO	1100000000012A1A2A(1,20)		RIM BIT Sa0
NO GO	1 400000000012A1A2A25		RIM BIT Sa1
NO GO	1 200000000012A1A2A25		RIM BIT Sa0
NO GO	1 100000000011A1A4A11		
NO GO	1 400000000 11A1A4A11		
NO GO	1 200000000 11A1A1A10		
NO GO	1 100000000 11A1A4A10		
NO GO	1 400000000 11A1A4A10		
NO GO	1 200000000 12A1A1A09		
NO GO	1 100000000 11A1A4A09		
NO GO	1 400000000 11A1A4A09		
NO GO	1 200000000 12A1A1A08		
NO GO	1 100000000 11A1A4A08		
NO GO	1 400000000 11A1A4A08		
NO GO	1 200000000 12A1A1A07		
NO GO	1 100000000 11A1A4A07		
NO GO	1 400000000 11A1A4A07		
NO GO	1 200000000 11A1A4A05		
NO GO	1 100000000 11A1A4A05		
NO GO	1 X00000012A1A1A04		
NO GO	1 X0000012A1A1A03		
NO GO	1 X000012A1A1A02		
NO GO	1 X00012A1A1A01		

22 81			SPARE	
22 82			SPARE	
22 83			SPARE	
22 84			SPARE	
22 85	1	T57	TEST FOR SHORT ROM -> RIM -> B REG	
22 86			LOAD A REGISTER WITH 88888888	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 88888888	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 44444444	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 44444444	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 22222222	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 22222222	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 11111111	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 11111111	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 81240000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 81240000	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 48120000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 48120000	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 24810000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 24810000	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 12480000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 12480000	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 00008124	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 00008124	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 00004812	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 00004812	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH 00002481	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F	ROM -> RIM
			COMPARE THE B REGISTER TO 00002481	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD A REGISTER WITH 00001248	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F8FFF0F7F	ROM -> RIM
			COMPARE THE B REGISTER TO 00001248	
			BRANCH TO MAJOR 22 MINOR 90 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 93	
22 87			SPARE	
22 88			SPARE	
22 89			SPARE	
22 90	2	F57.N	SHORT IN ROM -> RIM -> B REG	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXXX / REPLACE ASSEMBLIES: HIGHER LEVEL OF MAINTENANCE	
22 91				
22 92				
22 93	2	T58	TEST FOR SHORT DSPL -> IN MUX -> RIM	
22 94			LOAD A REGISTER WITH 88888888	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0FBF	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 88888888	
			BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 44444444	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0FBF	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 44444444	
			BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 22222222	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 22222222	
			BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 11111111	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0FBF	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 11111111	
			BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 81240000	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F877F0FBF	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO 81240000 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 48120000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 48120000 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 24810000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 24810000 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 12480000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 12480000 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 00008124 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 00008124 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 00004812 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 00004812 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 00002481 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 00002481 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH 00001248 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FB77F0F8F	ROM -> DSPL, DSPL -> IN MUX, 4MSB DSPL -> RIM
			COMPARE THE B REGISTER TO 00001248 BRANCH TO MAJOR 22 MINOR 96 ON NO-GO	
			BRANCH TO MAJOR 22 MINOR 98	
22 95			SPARE	
22 96	2	F58.F	SHORT IN IN MUX -> RIM, OR IN 4MSB OF RIM STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: HIGHER LEVEL OF MAINTENANCE	
22	97		SPARE	
22	98		ENABLE VERTICAL PARITY CHECK	
22	99		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** TEST SET CLOCK MODE AND NCU CLOCK CONTROL TESTS **********	
23 00			INITIALIZE- NOT A TEST DEFINE SELF TEST TAPE BRANCH TO MAJOR 23 MINOR 3	
23 01	2	F31.1	BPC638* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: A1A1A1A(21,23)	
23 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
23 03 23 04	1	T60	CHECK STATE OF GTC001*. PREVIOUS TEST = (22)T58 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A000000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 6 ON NO-GO BRANCH TO MAJOR 23 MINOR 20	MTW1 -> IN MUX NO-GO FOR GTC001* = 1
23 05			SPARE	
23 06 23 07	2	T60.N	ATTEMPT RESET OF GTC001* WITH INST STCL ENABLE LOW LEVEL ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A000000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 9 ON NO-GO	NO-GO IF GTC003* =1
23 08	3	T60.NG	TEST TST1(MTW1 ->INMX) INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A000000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 13 ON NO-GO BRANCH TO MAJOR 23 MINOR 20	MTW1->INMX
23 09	3	T60.NN	ATTEMPT RESET OF"CLOCK CONTROL FF"WITH RCNU, USES"DC CLOCK STOP"	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
23 10			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCJ CLOCK MODE (GTC003*) ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 14 ON NO-GO	NO-GO IF GTC003* =1
23 11	4	T60.NNG	ATTEMPT RESET OF "CLK CONTROL FF" WITH EOP "STOP COMP CLK" ENABLE CONTINUOUS HIGH LEVEL ON GTC001* LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E400 READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000 BRANCH TO MAJOR 23 MINOR 12 ON NO-GO	SET UP EA =0371, I/O REQ INACTIVE I/O REQ ACTIVE NO-GO IF GTC003* =1
	5	F60.NNGG	FAULT IN STCL IBT STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A3A13	BAD116* Sa1
23 12	5	F60.NNGN	CKB123* INACTIVE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 3001 — REPLACE ASSEMBLIES: 1A1A3A(12,13)	
23 13	4	T60.NGN	FAULT IN TST1(MTW1->INMX) ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 300 — REPLACE ASSEMBLIES: 1A1A2A21, 1A1A4A20	FYR010* Sa1
23 14 23 15	4	T60.NNN	ATTEMPT SET OF RESET COMPUTER FLAG ENABLE COMPUTER RESET (GTC000*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A COMPARE THE P REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 18 ON NO-GO	NO-GO FOR GTC000* = 1
	5	F60.NNNG	FAULT IN GTC001* -> MTW1 READ & COMPARE MISCELLANEOUS WORD 1 WITH A	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	NO-GO IF GTC003* =1
			INDICATORS: NO GO — DISPLAY: 300 — REPLACE ASSEMBLIES: 1A1A3A02 INDICATORS: NO GO — DISPLAY: 200 — REPLACE ASSEMBLIES: 1A1A4A03 INDICATORS: NO GO — DISPLAY: 100 — REPLACE ASSEMBLIES: 1A1A4A03	
23 16			SPARE	
23 17			SPARE	
23 18	5	F60.NNNN	FAULT IN RESET GTC001* TO 0, OR INST DECODE MATRIX STOP TAPE	
			INDICATORS: NONE — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(6,7,12,13,22)	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
23 19			SPARE	
23 20	1	T61 T60.NGG	CHECK STATE OF GTC001* IN NCU CLOCK MODE	
23 21			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*)	
	2	F61.1	FAULT LOC WITHIN TEST T61, NOT A PROGRAMMED STOP- NCU CLK MODE MAL	
			INDICATORS: TEST SET FAULT — DISPLAY: 4000000 — REPLACE ASSEMBLIES: 1A1A3A(22,25,27,28) OR 1A1A3A29	
	1	T61(CONT)	INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 22 ON NO-GO BRANCH TO MAJOR 23 MINOR 24	MTW1 -> IN MUX NO-GO FOR GTC001* = 1
23 22			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	2	F61.2	SET INPUT TO "CLK CONTROL FF" Sa1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 300(1A1A3A(3,6,7,15) — REPLACE ASSEMBLIES	
23 23			SPARE	
23 24 23 25	1	T62	TEST SET OF "CLK CONTROL FF" WITH RCPC INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. COMPARE THE B REGISTER TO A000000C LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 23 MINOR 27 ON NO-GO BRANCH TO MAJOR 23 MINOR 44	SET UP BIT PATTERN FOR TST1 FOLLOWING, MTW1->INMX NO-GO IF GTC001* = 0
23 26			SPARE	
23 27 23 28	2	T62.N	CHECK SET OF SIIC LATCH READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A01 - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 39 ON NO-GO	NO-GO IF GTC003* =1
23 29	3	T62.NG	CHECK FOR ACTIVE "OC CLK STOP" SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1F0B0FFF ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A014 - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 32 ON NO-GO	INH ALL MEM EXCEPT #7- ON KMA091, EN MTW1 -> IN MUX NO-GO IF GTC013* OR GTC020* INACTIVE
23 30	4	T62.NGS	TEST FOR APPROX 1 MICROSECOND PULSE ON GTC001* TO POSFIX RECIEVER INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFE0F7F ENABLE CONTROLLED TIMING PULSE INTERVAL 6 ON GTC001*	EN CLK RUN TAPE STOP, EN POSFIX PULSE TEST

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	5	F62.NGG.1	FAULT LOC WITHIN TEST T62.NGG- GTC001* PULSE OF INCORRECT WIDTH	
			INDICATORS: NONE — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A19; 1A1A3A(2,6,7,8,25)	NO PULSE AT ALL ON GTC001*
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A18; 1A1A3A(12,13); 2A1A2A(18,20,26)	PULSE WAS PRESENT
	4	T62.NGG (CONT)	SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) BRANCH TO MAJOR 23 MINOR 34	RESET TST2
23 31			SPARE	
23 32	4	F62.NGN	"DC CLK STOP" RESET KMA091 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 6000000 — REPLACE ASSEMBLIES: 1A1A3A(3,4,7,16,23)	BKB031* ACTIVE
23 33			SPARE	
23 34 23 35	5	T62.NGGG	CHECK FOR FAULT IN BOTH QUT051 AND QUT052 OF MTW1 READ & COMPARE MISCELLANEOUS WORD 1 WITH A00000C COMPARE THE B REGISTER TO A00000C LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS COMPARE THE B REGISTER TO A00000C BRANCH TO MAJOR 23 MINOR 37 ON NO-GO	NO-GO IF GTC001* = 0
	6	F62.NGGGG	FAULT IN RCPC SET OF GTC001* ACTIVE, OR MTW1 REC EN STOP TAPE	
			INDICATORS: NONE — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A18; 1A1A3A07; 1A1A4A20	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	FAULT IN INST DECODE MATRIX
23 36			SPARE	
23 37	6	F62.NGGGN	FAULT IN BIT 8 OR 9 OF MTW1 REC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: 200; REPLACE ASSEMBLIES: 1A1A4A03	
			INDICATORS: NO GO; DISPLAY: 100; REPLACE ASSEMBLIES: 1A1A4A03	
23 38			SPARE	
23 39 23 40	3	T62.NN	TEST LCU INST DECODE MATRIX, TRY INST RCFM SERIALLY LOAD THE B REGISTER WITH A READ & COMPARE THE FMB LINES WITH AFFFFFFF COMPARE THE P REGISTER TO THE A REGISTER BRANCH TO MAJOR 23 MINOR 42 ON NO-GO	
	4	F62.NNG	FAULT IN SIIC IBT OR LATCH STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: (1A1A2A(10,11,16)	
23 41			SPARE	
23 42	4	F62.NNN	FAULT IN LCU INST DECODE MATRIX STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
23 43			SPARE	
23 44 23 45	1	T63	CHECK RESET OF "CLK CONTROL FF" USING STCL ENABLE LOW LEVEL ON GTC001* INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 47 ON NO-GO BRANCH TO MAJOR 23 MINOR 56	MTW1 -> IN MUX NO-GO FOR GTC001* = 1
23 46			SPARE	
23 47 23 48	2	T63.N	ATTEMPT RESET OF "CLK CONTROL FF" WITH EOP "STOP COMP CLK" LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E400 READ & COMPARE MISCELLANEOUS WORD 1 WITH A COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000 BRANCH TO MAJOR 23 MINOR 50 ON NO-GO	SET UP EA =0371, I/O REQ INACTIVE I/O REQ ACTIVE NO-GO FOR GTC001* = 1
	3	F63.NG	FAULT IN STCL IBT STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A3A13	BAD116* Sa1
23 49			SPARE	
23 50 23 51	3	F63.NN	ATTEMPT RESET OF"CLOCK CONTROL FF"WITH RCNU, USES"DC CLOCK STOP" ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 53 ON NO-GO	NO-GO FOR GTC001* = 1

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	4	F63.NNG	CKB123* INACTIVE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 300011A1A3A(12,13)	
23 52			SPARE	
23 53 23 54	4	T63.NNN	ATTEMPT SET OF RESET COMPUTER FLAG ENABLE COMPUTER RESET (GTC000*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 55 ON NO-GO	NO-GO FOR GTC000* = 1
	5	F63.NNNG	FAULT IN FINAL GATE OUTPUT OF GTC001* STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — 11A1A3A02	GTC001* S@1
23 55	5	F63.NNNN	FAULT IN RESET GTC001* TO 0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000(1A1A3A(6,7,12,13)	
23 56 23 57	1	T64	SET UP "ANY MEM OP & CM7" TO RESET "CLK CONTROL FF" WITH "DC CLK STP", CHECK RESET OF TST2 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFDFOF4FFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* ENABLE SINGLE MEMORY MODE WITH ADDRESS: 0 DATA: CONTENTS OF A REGISTER INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. BRANCH TO MAJOR 23 MINOR 58 ON NO-GO SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*)	%TW1->INMX ON CMA121, SIM CM7, SIM NO-GO RESET TST2
			TEST FOR TST2 FF NOT RESET INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFFFOFOFFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* ENABLE SINGLE MEMORY MODE WITH ADDRESS: 0 DATA: CONTENTS OF A REGISTER	EN MEM #1 ON CMA121, SIM CM7,

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF BRANCH TO MAJOR 23 MINOR 63 ON NO-GO BRANCH TO MAJOR 23 MINOR 62	SIM NO GO
23 58 23 59	2	T64.1	RESET TST2 WITH LXMB PULSE THE XMB DRIVERS WITH THE A REGISTER INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG. BRANCH TO MAJOR 23 MINOR 60 ON NO-GO	
	3	F64.1.G	FAULT IN SLMA IBT,LATCH, OR CMA121 RESET OF TST2 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A15
		1A1A3A(1,7,15,20)

23 60	3	T64.1.N	ISOLATE BETWEEN FAULT IN RESET OF SELF TEST REG AND RESET OF TST2 PULSE THE XMB DRIVERS WITH THE A REGISTER BRANCH TO MAJOR 23 MINOR 61 ON NO-GO	
	4	F64.1.NG	INPUT TO GYR707 S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A3A15

23 61	4	F64.1.NN	FAULT IN"LCU B REG CLK MODE 2 ENABLE" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A3A15
		2A1A3A16
		OR
		PROCEED PER PARAGRAPH 3-13

23 62	2	F64.2	INPUT TO AYR752 S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A16	
23 63 23 64	1	T65	CHECK FOR RESET OF GTC001* TO 0 SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 66 ON NO-GO BRANCH TO MAJOR 23 MINOR 70	RESET TST2 FROM T64 NO-GO FOR GTC001* = 1
23 65			SPARE	
23 66 23 67	2	T65.N	CHECK FOR SLMA FF NOT RESET, RESULTS IN SHT DATA EN COMPARE THE B REGISTER TO A00000C BRANCH TO MAJOR 23 MINOR 68 ON NO-GO	GO IF SLMA FF IS RESET
	3	T65.NG	CHECK GTC001* WITH RCM1 READ & COMPARE MISCELLANEOUS WORD 1 WITH A00000C LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 23 MINOR 69 ON NO-GO	
	4	F65.NGG	FAULT IN "DC CLK STOP" RESET OF "CLK CONTROL FF" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(4,7,13)	
23 68	3	F65.NN	SLMA FF NOT RESET STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 125200000000C — REPLACE ASSEMBLIES: 1A1A3A(1,4,7)	
23 69	4	F65.NGN	FAULT IN TST2 LD BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 300120A1A3A15 — REPLACE ASSEMBLIES	
23 70 23 71	1	T66	TEST FOR NO "DC CLK STOP RESET OF GTC001* TO 0 IN CIU CLK MODE INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FDF0F0FFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) ENABLE SINGLE MEMORY MODE WITH ADDRESS: 0 DATA: CONTENTS OF A REGISTER COMPARE THE B REGISTER TO A000000C LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 23 MINOR 72 ON NO-GO BRANCH TO MAJOR 23 MINOR 77	MTW1->INMX ON CMA121, SIM CM7 NO-GO IF GTC001* = 0
23 72 23 73	2	T66.N	CHECK FOR SLMA FF NOT RESET, RESULTS IN SHT DATA EN COMPARE THE B REGISTER TO A000000C BRANCH TO MAJOR 23 MINOR 74 ON NO-GO	GO IF SLMA FF IS RESET
	3	T66.NG	CHECK SIIC LATCH FOR NOT RESET READ & COMPARE MISCELLANEOUS WORD 1 WITH A01 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 23 MINOR 75 ON NO-GO	NO-GO IF GTC003* =1
	4	F66.NGG	NO CIU CLK MODE DEFINE NCU TEST TAPE	
			INDICATORS: NCU — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A19	BVN022 S01
			INDICATORS: SELF TEST FLASH — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A17,22,25,28	CIU CLK MODE INACTIVE
23 74	3	F66.NN	SLMA FF NOT RESET STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 252000000001 — REPLACE ASSEMBLIES: 1A1A2A(19,20)	
			DISPLAY: — REPLACE ASSEMBLIES: 1A1A3A(1,3,7)	
23 75	4	F66.NGN	SIIC LATCH NOT RESET STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 4000000 — REPLACE ASSEMBLIES: 1A1A2A(10,11,16)	
23 76			SPARE	
23 77 23 78	1	T67	TEST RESET OF "CLK CONTROL FF" WITH RCNU INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCJ CLOCK MODE (GTC003*) ENABLE CONTINUOUS HIGH LEVEL ON GTC001* LOAD A REGISTER WITH A999 ENABLE CONTROLLED TIMING PULSE INTERVAL 999 ON GTC001*	SET UP BIT PATTERN FOR TST1 FOLLOWING, MTW1->INMX
	2	F67.1	FAULT LOC WITHIN TEST T67, NOT A PROGRAMMED STOP- FAULT IN "CLK COUNTER" INDICATORS: TEST SET FAULT — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 1A1A3A(6,7,8,9,10)	
	1	T67(CONT)	INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A000000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 79 ON NO-GO BRANCH TO MAJOR 23 MINOR 81	MTW1 -> IN MUX NO-GO FOR GTC001* = 1
23 79	2	T67.2	TEST RCNC GEN PULSE ON GTC001* ENABLE LOW LEVEL ON GTC001* SERIALLY LOAD THE B REGISTER WITH A03 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4F8FFE077F ENABLE CONTROLLED TIMING PULSE INTERVAL 14 CONDITIONALLY ON GTC001*	SET UP CM1 DATA EN LD CM, EN CLK RUN TAPE STOP, EN B->ROM, EN POSFIX PULSE TEST
	3	F67.2.1	FAULT LOC WITHIN TEST T67.2- PULSE ON GTC001* OF INCORRECT WIDTH INDICATORS: NONE — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A06	NO PULSE PRESENT
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(6,7,8,9,10)	
23 80	3	F67.2.2	FAULT IN "NORMAL CLK STP",OR RCNU IBT OR LATCH SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 300 — REPLACE ASSEMBLIES: 1A1A2A19, 1A1A3A(4,6,7,8)	
23 81 23 82	1	T68	TEST SET OF COMPUTER RESET FLAG, GTC000* ENABLE COMPUTER RESET (GTC000*) INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OF9FFFOFFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 23 MINOR 83 ON NO-GO BRANCH TO MAJOR 23 MINOR 85	MTW1 -> IN MUX NO-GO FOR GTC000* = 1
23 83	2	F68.N	FAULT IN RSET IBT OR LATCH, OR GTC000* -> MTW1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000 — REPLACE ASSEMBLIES: 1A1A2A(11,12,15), 1A1A4A05	
23 84			SPARE	
23 85 23 86	1	T69	TEST RESET OF RSET FF, GTC000* = 1, WITH RCNC LOAD A REGISTER WITH AFFF ENABLE CONTROLLED TIMING PULSE INTERVAL 10 CONDITIONALLY ON GTC001*	
	2	F69.1	FAULT LOC WITHIN TEST T69 - LOAD CLK COUNTER BEFORE END OF DATA	
			INDICATORS: TEST SET FAULT — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 1A1A1A09, 1A1A3A06	INPUT TO IKF113* OPEN
	1	T69(CONT)	INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OF9FFFOFFF COMPARE THE B RECISTER TO A0002 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 23 MINOR 87 ON NO-GO BRANCH TO MAJOR 23 MINOR 93	MTW1 -> IN MUX NO-GO IF GTC001* = 0
23 87 23 88	2	T69.2	CHECK RCNC RESET OF GTC001* TO 0 ENABLE CONTINUOUS HIGH LEVEL ON GTC001* ENABLE CONTROLLED TIMING PULSE INTERVAL 10 CONDITIONALLY ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A000000C - RESULT IN B & C REGISTER	NO-GO IF GTC001* = 1 & RCM1

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				IBT ACTIVE
			BRANCH TO MAJOR 23 MINOR 90 ON NO-GO	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OF9FFFOFFF	MTW1 -> IN MUX
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER	NO-GO FOR GTC001* = 1
			BRANCH TO MAJOR 23 MINOR 91 ON NO-GO	
	3	F69.2.N	FAULT IN "COMP CLK INH" RESET OF RSET FF, OR BIT OF MTW1 REC	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(11,12), 1A1A4A05	
23 89			SPARE	
23 90	3	F69.2.1	FAULT IN RCNC IBT OR LATCH	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 20000 / REPLACE ASSEMBLIES: 1A1A2A19, 1A1A3A07	
23 91	3	F69.2.2	FAULT IN LCU INST DECODE MATRIX	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 20000 / REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
23 92			SPARE	
23 93	1	T70	TEST "CONDITIONAL CLK STP" WITH RCNC UNABLE TO RESET GTC001* TO 0	
23 94			SERIALLY LOAD THE B REGISTER WITH A03	SET UP CM1 DATA
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4F9FFF07FF	EN LD CM, EN B->ROM, MTW1->INMX
			ENABLE CONTINUOUS HIGH LEVEL ON GTC001*	
			RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*)	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 20 CONDITIONALLY ON GTC001*	
			INITIATE SELF TEST MODE 1-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG.	
			COMPARE THE B REGISTER TO A000000	
			LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	NO-GO FOR GTC001* = 0
			ENABLE LOW LEVEL ON GTC001*	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 23 MINOR 95 ON NO-GO BRANCH TO MAJOR 23 MINOR 96	
23 95	2	F70.N	CONDITIONAL CC CLK STOP LATCH NOT RESET STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 3001 — REPLACE ASSEMBLIES: 1A1A3A(6,7)	
23 96	1	T71	TEST GEN OF PULSE ON GTC001* WITH RCNU & RCNC- PULSE MEASURED AT POSFIX RECEIVER SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCJ CLOCK MODE (GTC003*) INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFE0F7F PUNCH TAPE CODES - /8 /4 #F #6 #0 #0 &C	EN CLK RUN TAPE STOP, EN POSFIX PULSE TEST RCNU 005F - TEST SHORT DATA EN
	2	F71.1	FAULT LOC WITHIN TEST T71- INCORRECT PULSE WIDTH	
			INDICATORS: NONE — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
			INDICATORS: TEST SET FAULT — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 1A1A3A(5,7), 2A1A1A28	IAR111* S@1
23 97	1	T71(CONT)	SERIALLY LOAD THE B REGISTER WITH A03 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4FBFFE077F ENABLE CONTROLLED TIMING PULSE INTERVAL 16 CONDITIONALLY ON GTC001*	SET UP DATA FOR CM1 EN LD CM, EN CLK RUN TAPE STOP, EN B->ROM, EN POSFIX PULSE TEST
	2	F71.2	FAULT LOC WITHIN TEST T71- FAULT IN "CONDITIONAL CC CLK STP	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
	1	T71(CONT)	SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
23 98	1	T72	TEST OF INPUT TO MBC061 ENABLE VERTICAL PARITY CHECK BRANCH TO MAJOR 25 MINOR 1	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
23	99		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
24 00			BRANCH TO MAJOR 24 MINOR 3	
24 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
24 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
24 03			END OF MAJOR TEST	

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|TEST|DECISION | TEST/FAULT |                    SELF-TEST PROGRAM                    |          REMARKS          |
| NO.|  LEVEL  |   NUMBER   |                                                         |                           |

            ***************************************************************************************************
            *                                                                                                 *
            *                        EXTERNAL DATA PATHS TESTS- MAJORS 25, 26, 27, 28, 29                     *
            *                                                                                                 *
            *                             TESTS FOR LOGICAL FAULTS  T74 - T111                                *
            *                             TESTS FOR SHORTS  T112 - T121                                       *
            *                                                                                                 *
            ***************************************************************************************************


25 00                       INITIALIZE
                              DEFINE SELF TEST TAPE
                              SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCJ CLOCK MODE
                                (GTC003*)
                              ENABLE LOW LEVEL ON GTC001*
                              BRANCH TO MAJOR 25 MINOR 3


25 01                       INITIALIZE
                              DEFINE SELF TEST TAPE
                              SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCJ CLOCK MODE
                                (GTC003*)
                              ENABLE LOW LEVEL ON GTC001*
                              BRANCH TO MAJOR 25 MINOR 3


25 02   2       31.2        B8C537* S@1
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
                                    |  INDICATORS  | DISPLAY |        REPLACE ASSEMBLIES        |
                                    | NO GO       |  BLANK  | 1A1A1A23                         |


            ***************************************************************************************************
            *                                                                                                 *
            *           TEST FOR LOGICAL FAULTS IN EXTERNAL DATA PATHS- MAJORS 25 - 28 & 29 MINORS3 - 75      *
            *                                                                                                 *
            ***************************************************************************************************


25 03   1       T74         TEST MB DR -> JEP, ROM = AFFFFFFF BUT DR NOT ENABLED => 0->QUB(001-028)
                            PREVIOUS TEST = (23)T72
25 04                         LOAD A REGISTER WITH AFFFFFFF
                              INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 08BFFF0FFF       JEB->INMX
                              COMPARE THE B REGISTER TO A
                              BRANCH TO MAJOR 25 MINOR 5  ON NO-GO
                              BRANCH TO MAJOR 25 MINOR 20
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
25 05 25 06	2	T74.N	TEST MB DR -> WD1 REC, ROM = AFFFFFFF BUT DR NOT ENABLED => 0 -> WD1 LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0EBFFF0FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 25 MINOR 11 ON NO-GO	WD1 REC->INMX
25 07	3	F74.NG	SINGLE BIT OF EB REC SA1. SET UP ERROR BIT- BIT DSPL GIVES QUBOXX SA1 LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0BBFFF0FFF COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	JEB->INMX

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000 11A1A4A11	
NO GO	4000000000 11A1A4A11	
NO GO	2000000000 11A1A4A10	
NO GO	1000000000 11A1A4A10	
NO GO	4000000011A1A4A10	
NO GO	2000000011A1A4A09	
NO GO	1000000011A1A4A09	
NO GO	4000000011A1A4A09	
NO GO	2000000011A1A4A08	
NO GO	1000000011A1A4A08	
NO GO	4000000 11A1A4A08	
NO GO	2000000 11A1A4A07	
NO GO	1000000 11A1A4A07	
NO GO	4000011A1A4A07	
NO GO	2000011A1A4A05	
NO GO	1000011A1A4A05	
NO GO	X000 11A1A4A04	
NO GO	X00 11A1A4A03	
NO GO	X0 11A1A4A02	
NO GO	X1 1A1A4A01	

25 08 25 09 25 10			SPARE SPARE SPARE	
25 11	3	T74.NN	TEST FOR MB DR EN SA1 COMPARE THE B REGISTER TO AFF8 BRANCH TO MAJOR 25 MINOR 12 ON NO-GO	
	4	F74.NNG	FAULT IN EN OF MB DR STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
25 12	4	T74.NNN	TEST FOR MB DR EN S@1 COMPARE THE B REGISTER TO A07FC BRANCH TO MAJOR 25 MINOR 13 ON NO-GO	
	5	F74.NNNC	FAULT IN EN OF MB DR STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
25 13	5	T74.NNNN	TEST FOR MB OR EN S@1 COMPARE THE B REGISTER TO A00003FF BRANCH TO MAJOR 25 MINOR 14 ON NO-GO	
	6	F74.NNNNG	FAULT IN EN OF MB DR STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
25 14	6	T74.NNNNN	TEST FOR MB DR EN S@1 COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 25 MINOR 16 ON NO-GO	
	7	F74.NNNNNG	TOTAL MB DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(4,13,21); 1A1A3A02	
25 15			SPARE	
25 16	7	F74.NNNNNN	SINGLE BIT OF MB DR ACTIVE. SET UP ERROR BIT- BIT DSPL GIVES OTBOXX SIGNAL AFFECTED COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A2A(4,6)
NO GO	XX00000001	1A1A2A(6,7)
NO GO	4000000	1A1A2A(6,7)
NO GO	2000000	1A1A2A(5,7)
NO GO	1000000	1A1A2A(3,5)
NO GO	XXXX001	1A1A2A(3,5)
NO GO	401	1A1A2A(3,5)
NO GO	201	1A1A2A(3,5)
NO GO	101	1A1A2A(2,3)
NO GO	X11	1A1A2A(2,3)

25 17			SPARE	
25 18			SPARE	
25 19			SPARE	
25 20	1	T75	TEST MB DR -> JEB, ROM=AFFFFFFF & DR ENABLED => 1->QUB(001-028)	
25 21			LOAD A REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 28BFFFOFFF	ROM->MB, JEB->INMX
			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 25 MINOR 22 ON NO-GO	
			BRANCH TO MAJOR 25 MINOR 44	
25 22	2	T75.N	TEST MB DR -> WD1 REC, ROM=AFFFFFFF & DR ENABLED => 1-> WD1	
25 23			LOAD A REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2EBFFFOFFF	ROM->MB, WD1 REC->INMX
			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 25 MINOR 27 ON NO-GO	
			BRANCH TO MAJOR 25 MINOR 34	
25 24			SPARE	
25 25			SPARE	
25 26			SPARE	
25 27	3	T75.NN	TEST FOR MB DR EN S@0	
			COMPARE THE B REGISTER TO A007FFFF	
			BRANCH TO MAJOR 25 MINOR 28 ON NO-GO	
	4	F75.NNG	FAULT IN EN OF MP DR	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A04	
25 28	4	T75.NNN	TEST FOR MB DR EN S@O COMPARE THE B REGISTER TO AFF803FF BRANCH TO MAJOR 25 MINOR 29 ON NO-GO	
	5	F75.NNNG	FAULT IN EN OF MB DR STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A04	
25 29	5	T75.NNNN	TEST FOR MB DR EN S@O COMPARE THE B REGISTER TO AFFFFC BRANCH TO MAJOR 25 MINOR 30 ON NO-GO	
	6	F75.NNNNG	FAULT IN EN OF MB DR STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A04	
25 30	6	T75.NNNNN	TEST FOR MB DR EN S@O COMPARE THE B REGISTER TO A BRANCH TO MAJOR 25 MINOR 32 ON NO-GO	
	7	F75.NNNNNG	TOTAL MB DR EN S@O STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A14,19,21	
25 31			SPARE	
25 32	7	F75.NNNNNN	SINGLE BIT OF MB DR INACTIVE. SET UP ERROR BIT- BIT DSPL GIVES OTBOXX SIGNAL AFFECTED COMPARE THE B REGISTER TO AFFFFFFF STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A2A(4,6)
NO GO	XX00000001	1A1A2A(6,7)
NO GO	4000000	1A1A2A(6,7)
NO GO	2000000	1A1A2A(5,7)
NO GO	1000000	1A1A2A(3,5)
NO GO	XXXX001	1A1A2A(3,5)
NO GO	401	1A1A2A(3,5)
NO GO	201	1A1A2A(3,5)
NO GO	101	1A1A2A(2,3)
NO GO	X[	1A1A2A(2,3)

25 33 SPARE

25 34 3 T75.NG FAULT IN EB REC. REPEAT T75 TO SET UP FAULT BIT PATTERN. LOOK FOR EN S@0
25 35 LOAD A REGISTEP WITH AFFFFFFF
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF ROM->MB, JEB->INMX
COMPARE THE B REGISTER TO A01FFFFF
BRANCH TO MAJOR 25 MINOR 36 ON NO-GO

4 F75.NGG FAULT IN EB REC EN- S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

25 36 4 T75.NGN TEST FOR EB REC EN S@0
COMPARE THE B REGISTER TO AFE03FFF
BRANCH TO MAJOR 25 MINOR 37 ON NO-GO

5 F75.NGNG FAULT IN EB REC EN- S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

25 37 5 T75.NGNN TEST FOR EB REC EN S@0
COMPARE THE B REGISTER TO AFFFC07F
BRANCH TO MAJOR 25 MINOR 38 ON NO-GO

6 F75.NGNNG FAULT IN EB REC EN- S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

25 38 6 T75.NGNNN

TEST FOR EB REC EN S@O
COMPARE THE B REGISTER TO AFFFFF8
BRANCH TO MAJOR 25 MINOR 39 ON NO-GO

7 F75.NGNNNG

FAULT IN EB REC EN- S@O
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

25 39 7 T75.NGNNNN

TEST FOR EB REC EN S@O
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 25 MINOR 41 ON NO-GO

8 F75.NGNNNN
--->G

TOTAL EB REC EN S@O
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A21
		1A1A4A19

25 40

SPARE

25 41 8 F75.NGNNNN
--->N

SINGLE BIT OF EB REC S@O. SET UP ERROR BIT- BIT DSPL GIVES QUBOXX SIGNAL AFFECTED
COMPARE THE B REGISTER TO AFFFFFFF
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A11
NO GO	4000000000	1A1A4A11
NO GO	2000000000	1A1A4A10
NO GO	1000000000	1A1A4A10
NO GO	400000000	1A1A4A10
NO GO	200000000	1A1A4A09
NO GO	100000000	1A1A4A09

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

TABLE CONTINUED FROM PRECEEDING PAGE

NO GO		40000011A1A4A09	
NO GO		20000011A1A4A08	
NO GO		10000011A1A4A08	
NO GO		40000011A1A4A08	
NO GO		20000011A1A4A07	
NO GO		10000011A1A4A07	
NO GO		40000011A1A4A07	
NO GO		20000011A1A4A05	
NO GO		10000011A1A4A05	
NO GO		X0001A1A4A04	
NO GO		X001A1A4A03	
NO GO		X011A1A4A02	
NO GO		X11A1A4A01	

25 42 SPARE

25 43 SPARE

25 44 1 T76 TEST MB -> JEB, ROM = A0000000 & DR ENABLED => CHECK DATA INPUTS TO MB DP FOR S@1 FAULT

25 45 LOAD A REGISTER WITH A0000000
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFF0FFF ROM->MB, JEB->INMX
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 25 MINOR 46 ON NO-GO
BRANCH TO MAJOR 25 MINOR 55

25 46 2 T76.N CHECK FOR FAULT IN BIT 28

25 47 COMPARE THE B REGISTER TO A8
BRANCH TO MAJOR 25 MINOR 48 ON NO-GO

3 F76.NG DATA INPUT TO 28TH BIT OF MB DR S@1
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A04

25 48 3 T76.NN CHECK FOR FAULT IN BIT 20 - 27 OF MB DR

25 49 LOGICALLY 'AND' C REGISTER AND A7F8 - RESULT IN B & C REGISTER
BRANCH TO MAJOR 25 MINOR 51 ON NO-GO

4 F76.NNG DATA INPUT TO BIT 1 - 19 OF MB DR S@1.
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A03

25 50 SPARE

25 51 4 F76.NNN DATA INPUT TO BIT 20 - 27 OF MB DR SAL. DSPL BIT GIVES MB OUTPUT SIGNAL-OTBOXX
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXXXX	1A1A2A07

25 52 SPARE
25 53 SPARE
25 54 SPARE

25 55 1 T77 TEST MB DR -> WD1 REC, DR INACTIVE => 0->WD1 REC
25 56 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0EBFFF0FFF — WD1 REC->INMX
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 25 MINOR 57 ON NO-GO
BRANCH TO MAJOR 25 MINOR 61

25 57 2 F77.N SINGLE BIT OF WD1 REC SAL. DSPL BIT GIVES SIGNAL- 1-3 QUA00(1-3), 4-8 QUE00(1-5), 9-13 QUI00(1-5), 14-28 QUP(01-15)
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A11
NO GO	4000000000	1A1A4A11
NO GO	2000000000	1A1A4A10
NO GO	1000000000	1A1A4A10
NO GO	4000000000	1A1A4A10
NO GO	2000000000	1A1A4A09
NO GO	1000000000	1A1A4A09
NO GO	4000000000	1A1A4A09
NO GO	2000000000	1A1A4A08
NO GO	1000000000	1A1A4A08
NO GO	4000000000	1A1A4A08
NO GO	2000000000	1A1A4A07
NO GO	1000000000	1A1A4A07
NO GO	4000000000	1A1A4A07
NO GO	2000000000	1A1A4A05

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO | 1000011A1A4A05	
			NO GO | X000011A1A4A04	
			NO GO | XX0011A1A4A03	
			NO GO | XX011A1A4A02	
			NO GO | XX11A1A4A01	
25 58			SPARE	
25 59			SPARE	
25 60			SPARE	
25 61 25 62	1	T78	TEST MB DR -> WD1 REC, ROM = AFFFFFFF & DR ENABLED => 1->WD1 REC LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2EBFFF0FFF COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 25 MINOR 66 ON NO-GO BRANCH TO MAJOR 25 MINOR 76	ROM->MB, WD1 REC->INMX
25 63			SPARE	
25 64			SPARE	
25 65			SPARE	
25 66	2	T78.N	TEST FOR WD1 REC EN S@0 COMPARE THE B REGISTER TO A01FFFFF BRANCH TO MAJOR 25 MINOR 67 ON NO-GO	
	3	F78.NG	FAULT IN WD1 REC, EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | 1A1A4A17	
25 67	3	T78.NN	TEST FOR WD1 REC EN S@0 COMPARE THE B REGISTER TO AFE01FFF BRANCH TO MAJOR 25 MINOR 68 ON NO-GO	
	4	F78.NNG	FAULT IN WD1 REC, EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A4A17	
25 68	4	T78.NNN	TEST FOR WD1 REC EN S@O COMPARE THE B REGISTER TO AFFFE0FF BRANCH TO MAJOR 25 MINOR 69 ON NO-GO	
	5	F78.NNNG	FAULT IN WD1 REC, EN S@O STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A4A17	
25 69	5	T78.NNNN	TEST FOR WD1 REC EN S@O COMPARE THE B REGISTER TO AFFFFF07 BRANCH TO MAJOR 25 MINOR 70 ON NO-GO	
	6	F78.NNNNG	FAULT IN WD1 REC, EN S@O STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A4A16	
25 70	6	T78.NNNNN	TEST FOR WD1 REC EN S@O COMPARE THE B REGISTER TO AFFFFFF8 BRANCH TO MAJOR 25 MINOR 71 ON NO-GO	
	7	F78.NNNNNG	FAULT IN WD1 REC, EN S@O STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A4A16	
25 71	7	T78.NNNNNN	TEST FOR WD1 REC EN S@O COMPARE THE B REGISTER TO A BRANCH TO MAJOR 25 MINOR 72 ON NO-GO	
	8	F78.NNNNNN --->G	TOTAL WD1 REC EN S@O STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A(19,21)

25 72 8 F78.NNNNNN ---->N

SINGLE BIT OF WD1 REC S01. DSPL BIT GIVES SIGNAL- 1-3 QUA00(1-3), 4-8 QUE00(1-5), 9-13 QUI00(1-5),
14-28 QUP0(01-15)
COMPARE THE B REGISTER TO AFFFFFFF
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A11
NO GO	4000000000	1A1A4A11
NO GO	2000000000	1A1A4A(10,12)
NO GO	1000000000	1A1A4A10
NO GO	4000000000	1A1A4A10
NO GO	2000000000	1A1A4A(9,12)
NO GO	1000000000	1A1A4A09
NO GO	4000000000	1A1A4A09
NO GO	2000000000	1A1A4A(8,12)
NO GO	1000000000	1A1A4A08
NO GO	4000000000	1A1A4A08
NO GO	2000000000	1A1A4A(7,12)
NO GO	1000000000	1A1A4A07
NO GO	4000000000	1A1A4A07
NO GO	2000000000	1A1A4A05
NO GO	1000000000	1A1A4A05
NO GO	4000000000	1A1A4A(4,6)
NO GO	2000000000	1A1A4A04
NO GO	1000000000	1A1A4A04
NO GO	4000000000	1A1A4A(3,6)
NO GO	2000000000	1A1A4A03
NO GO	1000000000	1A1A4A03
NO GO	4000000000	1A1A4A(2,6)
NO GO	2000000000	1A1A4A02
NO GO	1000000000	1A1A4A02
NO GO	4000000000	1A1A4A(1,6)
NO GO	2000000000	1A1A4A01
NO GO	1000000000	1A1A4A01

25 73 SPARE
25 74 SPARE
25 75 SPARE

25 76 1 T79 TEST WD1* DR -> NAD*, ROM = AFFFFFFF BUT DR NOT ENABLED => 1->NAD*
25 77 LOAD A REGISTER WITH AFFFFFFF
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH D7BFFF0FFF NAD->INMX
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 25 MINOR 78 ON NO-GO

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 25 MINOR 98	
25 78 25 79	2	T79.N	TEST WD1* DR -> PJB, ROM = AFFFFFFF BUT DR NOT ENABLED => 1->PJB LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FF7 COMPARE THE B REGISTER TO AFFFFFFF LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 25 MINOR 83 ON NO-GO	PJB->RIM FAULT BIT PATTERN -> BREG
25 80	3	F79.NG	SINGLE BIT OF NAD* REC ACTIVE. REPEAT T79 TO SET UP ERROR BIT- DSPL BIT GIVES BIT OF REC AT FAULT LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 07BFFF0FFF COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	NAD->INMX

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000011A1A4A(9,11)	
NO GO	4000000000011A1A4A(9,11)	
NO GO	2000000000011A1A4A(9,10)	
NO GO	1000000000011A1A4A(9,10)	
NO GO	400000000011A1A4A10	
NO GO	200000000011A1A4A(9,10)	
NO GO	100000000011A1A4A(9,10)	
NO GO	40000000011A1A4A(9,10)	
NO GO	20000000011A1A4A(8,17)	
NO GO	10000000011A1A4A(8,17)	
NO GO	4000000011A1A4A(8,17)	
NO GO	2000000011A1A4A(7,17)	
NO GO	1000000011A1A4A(7,17)	
NO GO	400000011A1A4A(7,17)	
NO GO	200000011A1A4A(5,17)	
NO GO	100000011A1A4A(5,17)	
NO GO	X00011A1A4A(4,17)	
NO GO	4001 1A1A4A(3,17)	
NO GO	2001 1A1A4A(3,20)	
NO GO	1001 1A1A4A(3,20)	
NO GO	X011A1A4A(2,20)	
NO GO	X11A1A4A(1,20)	

25 81 25 82			SPARE SPARE
25 83	3	T79.NN	TEST FOR WD1 DR EN S@1 COMPARE THE B REGISTER TO AF8 BRANCH TO MAJOR 25 MINOR 84 ON NO-GO
	4	F79.NNG	WD1 DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A08	
25 84	4	T79.NNN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO A07C BRANCH TO MAJOR 25 MINOR 85 ON NO-GO	
	5	F79.NNNG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A08	
25 85	5	T79.NNNN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO A003E BRANCH TO MAJOR 25 MINOR 86 ON NO-GO	
	6	F79.NNNNG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A04	
25 86	6	T79.NNNNN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO AFFFE BRANCH TO MAJOR 25 MINOR 87 ON NO-GO	
	7	F79.NNNNNG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(4,13); 1A1A3A01	
25 87	7	T79.NNNNNN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO A0001F BRANCH TO MAJOR 25 MINOR 88 ON NO-GO	
	8	F79.NNNNNN --->G	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(9,13)	
25 88	8	T79.NNNNNN --->N	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO A00000F8 BRANCH TO MAJOR 25 MINOR 89 ON NO-GO	
	9	F79.NNNNNN --->NG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(9,13)	
25 89	9	T79.NNNNNN --->NN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO A0000007 BRANCH TO MAJOR 25 MINOR 90 ON NO-GO	
	10	F79.NNNNNN --->NNG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(9,13)	
25 90	10	T79.NNNNNN --->NNN	TEST FOR WD1 OR EN S@1 COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 25 MINOR 92 ON NO-GO	
	11	F79.NNNNNN --->NNNG	WD1 OR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(4,12,16,21)	
25 91			SPARE	
25 92	11	T79.NNNNNN --->NNNN	SINGLE BIT OF WD1* OR S@0, CHECK FOR FAULT AT BIT 14-28	
25 93			COMPARE THE B REGISTER TO A	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOGICALLY 'AND' C REGISTER AND AFFFE - RESULT IN B & C REGISTER BRANCH TO MAJOR 25 MINOR 94 ON NO-GO	
	12	F79.NNNNNN --->NNNNG	SINGLE BIT 1-13 OF WD1* OR S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A09

25 94	12	F79.NNNNNN --->NNNNN	SINGLE BIT 14-28 OF WD1* OR S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXX0000	1A1A2A08

25 95			SPARE	
25 96			SPARE	
25 97			SPARE	
25 98			ENABLE VERTICAL PARITY CHECK	
25 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
26 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 26 MINOR 3	
26 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
26 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
26 03	2	T80	TEST WD1* DR -> NAD*, ROM = AFFFFFFF & DR ENABLED => 0->NAD* = 1->B REG	
26 04			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 26 MINOR 5 ON NO-GO BRANCH TO MAJOR 26 MINOR 34	ROM->WD1 DR, NAD->INMX
26 05	2	T80.N	TEST WD1* DR -> PJB, ROM = AFFFFFFF & DR ENABLED => 0-> PJB, 0->B REG	
26 06			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 11 ON NO-GO BRANCH TO MAJOR 26 MINOR 24	ROM->WD1 DR, PJB->RIM
26 07			SPARE	
26 08			SPARE	
26 09			SPARE	
26 10			SPARE	
26 11	3	T80.NN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO AF8 BRANCH TO MAJOR 26 MINOR 12 ON NO-GO	
	4	F80.NNG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
26 12	4	T80.NNN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO A07C BRANCH TO MAJOR 26 MINOR 13 ON NO-GO	
	5	F80.NNNG	WD1* DR EN S@0	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	11A1A2A08

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A08	
26 13	5	T80.NNNN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO A003E BRANCH TO MAJOR 26 MINOR 14 ON NO-GO	
	6	F80.NNNNG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A04	
26 14	6	T80.NNNNN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO AFFFE BRANCH TO MAJOR 26 MINOR 15 ON NO-GO	
	7	F80.NNNNNG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A04	
26 15	7	T80.NNNNNN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO A0001F BRANCH TO MAJOR 26 MINOR 16 ON NO-GO	
	8	T80.NNNNNN --->G	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A09	
26 16	8	T80.NNNNNN --->N	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO A00000F8 BRANCH TO MAJOR 26 MINOR 17 ON NO-GO	
	9	F80.NNNNNN --->NG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: A1 A2 A09	
26 17	9	T80.NNNNNN --->NN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO A0000007 BRANCH TO MAJOR 26 MINOR 18 ON NO-GO	
	10	F80.NNNNNN --->NNG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: A1 A2 A09	
26 18	10	T80.NNNNNN --->NNN	TEST FOR WD1* DR EN S@0 COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 26 MINOR 20 ON NO-GO	
	11	F80.NNNNNN --->NNNG	WD1* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: A1 A2 A(4,16,21)	
26 19			SPARE	
26 20	11	T80.NNNNNN --->NNNN	SINGLE BIT OF WD1* DR S@1- CHECK FOR FAULT AT BIT 14-28	
26 21			COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AFFFE - RESULT IN B & C REGISTER BRANCH TO MAJOR 22 ON NO-GO	
	12	F80.NNNNNN --->NNNNG	SINGLE BIT OF WD1* DR S@1, BIT 1-13 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A09	
26 22	12	F80.NNNNNN --->NNNNN	SINGLE BIT OF WD1* DR S@1,BIT 14-28 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A2A08	
26 23			SPARE	
26 24	3	T80.NG	FAULT IN NAD* REC, REPEAT T80 TO SET UP FAULT BIT PATTERN. TEST FOR NAD* REC EN S@0	
26 25			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 878FFF0FFF COMPARE THE B REGISTER TO A003FFFF BRANCH TO MAJOR 26 MINOR 26 ON NO-GO	ROM->WD1 DR, NAD->INMX
	4	F80.NGG	NAD* REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A16	
26 26	4	T80.NGN	TEST FOR NAD* REC EN S@0 COMPARE THE B REGISTER TO AFFC01FF BRANCH TO MAJOR 26 MINOR 27 ON NO-GO	
	5	F80.NGNG	NAD* REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A16	
26 27	5	T80.NGNN	TEST FOR NAD* REC EN S@0 COMPARE THE B REGISTER TO AFFFFE BRANCH TO MAJOR 26 MINOR 28 ON NO-GO	
	6	F80.NGNNG	NAD* REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A16

26 28 6 T80.NGNNN

TEST FOR NAD* REC EN S@0
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 26 MINOR 30 ON NO-GO

7 F80.NGNNNG

TOTAL NAD* REC S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A21
		1A1A4A16

26 29

SPARE

26 30 7 F80.NGNNNN

SINGLE BIT OF NAD* REC INACTIVE, SET UP ERROR BIT- DSPL BIT GIVES BIT OF REC INACTIVE
COMPARE THE B REGISTER TO AFFFFFFF
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A(9,11)
NO GO	4000000000	1A1A4A(9,11)
NO GO	2000000000	1A1A4A(9,10)
NO GO	1000000000	1A1A4A(9,10)
NO GO	400000000	1A1A4A10
NO GO	200000000	1A1A4A(9,10)
NO GO	100000000	1A1A4A(9,10)
NO GO	40000000	1A1A4A(9,10)
NO GO	20000000	1A1A4A(8,17)
NO GO	10000000	1A1A4A(8,17)
NO GO	4000000	1A1A4A(8,17)
NO GO	2000000	1A1A4A(7,17)
NO GO	1000000	1A1A4A(7,17)
NO GO	400000	1A1A4A(7,17)
NO GO	200000	1A1A4A(5,17)
NO GO	100000	1A1A4A(5,17)
NO GO	X00000	1A1A4A(4,17)
NO GO	40011	1A1A4A(3,17)
NO GO	20011	1A1A4A(3,20)
NO GO	10011	1A1A4A(3,20)

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO — X011A1A4A4(2,20)	
			NO GO — X11A1A4A4(1,20)	
26 31			SPARE	
26 32			SPARE	
26 33			SPARE	
26 34	1	T81	TEST WD1* DR -> NAD*, ROM = A0000000 & DR ENABLED, TESTS FOR DATA INPUTS TO DR S@1	
26 35			LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 26 MINOR 36 ON NO-GO BRANCH TO MAJOR 26 MINOR 42	ROM->WD1 DR, NAD->INMX
26 36	2	T81.N	TEST FOR INPUT TO DR S@1 AT BIT 14-28	
26 37			LOGICALLY 'AND' C REGISTER AND AFFFE - RESULT IN B & C REGISTER BRANCH TO MAJOR 26 MINOR 38 ON NO-GO	
	3	F81.NG	DATA INPUT TO BIT 1-13 OF WD1* DR S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A09	
26 38	3	F81.NN	DATA INPUT TO BIT 14-28 OF WD1* DR S@1- DSPL BIT GIVES DR BIT AFFECTED STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A2A08	
26 39			SPARE	
26 40			SPARE	
26 41			SPARE	
26 42	1	T82	TEST WD1* DR -> PJB, DRIVER INACTIVE => 1->PJB, 1->B REG	
26 43			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FF7 COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 26 MINOR 47 ON NO-GO BRANCH TO MAJOR 26 MINOR 57	PJB->RIM
26 44			SPARE	
26 45			SPARE	
26 46			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
26 47	2	T82.N	TEST FOR PJB REC EN S@0 COMPARE THE B REGISTER TO A01FFFFF BRANCH TO MAJOR 26 MINOR 48 ON NO-GO	
	3	F82.NG	PJB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A09	
26 48	3	T82.NN	TEST FOR PJB REC EN S@0 COMPARE THE B REGISTER TO AFE03FFF BRANCH TO MAJOR 26 MINOR 49 ON NO-GO	
	4	F82.NNG	PJB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A09	
26 49	4	T82.NNN	TEST FOR PJB REC EN S@0 COMPARE THE B REGISTER TO AFFFC07F BRANCH TO MAJOR 26 MINOR 50 ON NO-GO	
	5	F82.NNNG	PJB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A09	
26 50	5	T82.NNNN	TEST FOR PJB REC EN S@0 COMPARE THE B REGISTER TO AFFFFF8 BRANCH TO MAJOR 26 MINOR 51 ON NO-GO	
	6	F82.NNNNG	PJB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A09	
26 51	6	T82.NNNNN	TEST FOR PJB REC EN S@0 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 53 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	7	F82.NNNNNG	TOTAL PJB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A1A07
		2A1A2A09

26 52			SPARE	
26 53	7	F82.NNNNNN	SINGLE BIT OF PJB REC S@0. SET UP ERROR BIT- DSPL BIT GIVES BIT OF REC S@0 COMPARE THE B REGISTER TO AFFFFFFF STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000000002	2A1A2A25
NO GO	X0000000002	2A1A2A25
NO GO	XX000000002	2A1A2A24
NO GO	XXX00000002	2A1A2A23
NO GO	XXXX0000002	2A1A2A22
NO GO	XXXXX000002	2A1A2A21

26 54			SPARE	
26 55			SPARE	
26 56			SPARE	
26 57	1	T83	TEST WD1* -> PJB, ROM = AFFFFFFF & DR ENABLED => 0->PJB, 0->B REG	
26 58			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFFOFF7 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 59 ON NO-GO BRANCH TO MAJOR 26 MINOR 62	ROM->WD1 DR, PJB->RIM
26 59	2	T83.N	SINGLE BIT OF PJB REC S@1 WHEN EN- DSPL BIT GIVES BIT OF REC S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000000002	2A1A2A25
NO GO	X0000000002	2A1A2A25
NO GO	XX000000002	2A1A2A24
NO GO	XXX00000002	2A1A2A23
NO GO	XXXX0000002	2A1A2A22
NO GO	XXXXX000002	2A1A2A21

26 60			SPARE	
26 61			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
26 62	1	T84	TEST XMB* DR -> XMB* REC, ROM = AFFFFFFF BUT DR NOT ENABLED => 1->XMB*->0->B REG	
26 63			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBDFFOFFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 64 ON NO-GO BRANCH TO MAJOR 26 MINOR 78	XMB->INMX
26 64	2	T84.N	TEST XMB* DR -> FMB, ROM = AFFFFFFF BUT DR NOT ENABLED => 1->FMB, 1->B REG	
26 65			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBBFFOFFF COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 26 MINOR 69 ON NO-GO	FMB->INMX
26 66	3	F84.NG	SINGLE BIT OF XMB* REC ACTIVE WHEN EN. REPEAT T84 TO SET UP ERROR BIT-DSPL BIT = ACTIVE REC BIT INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBDFFOFFF COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	XMB->INMX

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A2A03 1A1A4A12
NO GO	XXX000000	1A1A2A04 1A1A4A12
NO GO	400000	1A1A2A03 1A1A4A12
NO GO	200000	1A1A2A03 1A1A4A12
NO GO	100000	1A1A2A03 1A1A4A06
NO GO	XXXXX	1A1A2A03 1A1A4A06

26 67			SPARE	
26 68			SPARE	
26 69	3	T84.NN	TEST FOR XMB* DR EN S@1 COMPARE THE B REGISTER TO A007FFFF BRANCH TO MAJOR 26 MINOR 70 ON NO-GO	
	4	F84.NNG	XMB* DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
26 70	4	T84.NNN	TEST FOR XMB* DR EN S@1 COMPARE THE B REGISTER TO AFF803FF BRANCH TO MAJOR 26 MINOR 71 ON NO-GO	
	5	F84.NNNG	XMB* DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
26 71	5	T84.NNNN	TEST FOR XMB* DR EN S@1 COMPARE THE B REGISTER TO AFFFFC BRANCH TO MAJOR 26 MINOR 72 ON NO-GO	
	6	F84.NNNNG	XMB* DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A04	
26 72	6	T84.NNNNN	TEST FOR XMB* DR EN S@1 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 74 ON NO-GO	
	7	F84.NNNNNG	TOTAL XMB* DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(4,13,16,21)	
26 73			SPARE	
26 74	7	T84.NNNNNN	SINGLE BIT OF XMB* DR ACTIVE, TEST FOR FAULT AT BIT 17-28 COMPARE THE B REGISTER TO AFFFFFFF LOGICALLY 'AND' C REGISTER AND AFFF - RESULT IN B & C REGISTER BRANCH TO MAJOR 26 MINOR 75 ON NO-GO	
	8	F84.NNNNNN --->G	SINGLE BIT OF BIT 1-16,XMB* DR,ACTIVE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 11A1A2A04	
26 86	4	T85.NNN	TEST FOR XMB* DR EN S@0 COMPARE THE B REGISTER TO A007FC BRANCH TO MAJOR 26 MINOR 87 ON NO-GO	
	5	F85.NNNG	XMB* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 11A1A2A04	
26 87	5	T85.NNNN	TEST FOR XMB* DR EN S@0 COMPARE THE B REGISTER TO A00003FF BRANCH TO MAJOR 26 MINOR 88 ON NO-GO	
	6	F85.NNNNG	XMB* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 11A1A2A04	
26 88	6	T85.NNNNN	TEST FOR XMB* DR EN S@0 COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 26 MINOR 90 ON NO-GO	
	7	F85.NNNNNG	TOTAL XMB* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 11A1A2A(4,16,21)	
26 89			SPARE	
26 90	7	F85.NNNNNN	SINGLE BIT OF XMB* DR INACTIVE. SET UP ERROR BIT- DSPL BIT = INACTIVE BIT OF DR COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A01	
26 75	8	F84.NNNNNN --->N	SINGLE BIT OF XMB* DR ACTIVE, BIT 17-28- DSPL BIT GIVES ACTIVE DR BIT STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A2A02	
26 76			SPARE	
26 77			SPARE	
26 78	1	T85	TEST XMB* DR -> XMB* REC, ROM = AFFFFFFF & DR ENABLED => 0->XMB* REC->1->B REG	
26 79			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 26 MINOR 80 ON NO-GO BRANCH TO MAJOR 26 MINOR 98	ROM->XMB DR, XMB REC->INMX
26 80	2	T85.N	TEST XMB* DR -> FMB, ROM = AFFFFFFF & DR EN => 0->FMB->0->B REG	
26 81			LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 26 MINOR 85 ON NO-GO BRANCH TO MAJOR 26 MINOR 94	ROM->XMB* DR, FMB->INMX
26 82			SPARE	
26 83			SPARE	
26 84			SPARE	
26 85	3	T85.NN	TEST FOR XMB* DR EN S@0 COMPARE THE B REGISTER TO AFF8 BRANCH TO MAJOR 26 MINOR 86 ON NO-GO	
	4	F85.NNG	XMB* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A2A02
NO GO	XXX0000000	1A1A2A02
NO GO	400000	1A1A2A02
NO GO	200000	1A1A2A02
NO GO	100000	1A1A2A01
NO GO	XXXXX	1A1A2A01

26 91 SPARE
26 92 SPARE
26 93 SPARE

26 94 3 T85.NG FAULT IN XMB* REC. REPEAT T85 TO SET UP FAULT BIT PATTERN. TEST FOR XMB* REC EN S@0
26 95 LOAD A REGISTER WITH AFFFFFFF
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFF0FFF ROM->XMB DR, XMB REC->INMX
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 26 MINOR 96 ON NO-GO

4 F85.NGG TOTAL XMB* DR EN S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A21
		1A1A4A18

26 96 4 T85.NGN SINGLE BIT OF XMB* REC INACTIVE. SET UP ERROR BIT- DSPL BIT = INACTIVE BITOF XMB* REC
COMPARE THE B REGISTER TO AFFFFFFF
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A2A03
		1A1A4A12
NO GO	XXX0000000	1A1A2A04
		1A1A4A12
NO GO	400000	1A1A2A03
		1A1A4A12
NO GO	200000	1A1A2A03
		1A1A4A12
NO GO	100000	1A1A2A03
		1A1A4A06

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
		NO GO	XXXXX 1A1A2A03	
			1A1A4A06	
26 97			SPARE	
26 98			ENABLE VERTICAL PARITY CHECK	
26 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
27 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 27 MINOR 3	
27 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
27 02	2	F30.3	FAULT IN 4SB OF MABC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A1A(21,22)

27 03	1	T86	TEST XMB* DR -> XMB* REC, ROM = A0000000, TEST FOR DATA INPUT TO XMB* DR S@1	
27 04			LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFF0FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 27 MINOR 5 ON NO-GO BRANCH TO MAJOR 27 MINOR 11	ROM->XMB DR, XMB REC->INMX
27 05 27 06	2	T86.N	TEST FOR FAULT AT BIT 17-28 LOGICALLY 'AND' C REGISTER AND AFFFF - RESULT IN B & C REGISTER BRANCH TO MAJOR 27 MINOR 7 ON NO-GO	
	3	F86.NG	DATA INPUT TO XMB* DR,BIT 1-16, S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A01

27 07	3	F86.NN	DATA INPUT TO XMB* DR, BIT 17-28 S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXXX	1A1A2A02

27 08			SPARE	
27 09			SPARE	
27 10			SPARE	

27 11	1	T87	TEST XMB* DR -> FMB, DR INACTIVE => 1->FMB->1->B REG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
27 12			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBBFF0FFF COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 27 MINOR 16 ON NO-GO BRANCH TO MAJOR 27 MINOR 26	FMB->IVMX
27 13			SPARE	
27 14			SPARE	
27 15			SPARE	
27 16	2	T87.N	TEST FOR FMB REC EN S@0 COMPARE THE B REGISTER TO A01FFFFF BRANCH TO MAJOR 27 MINOR 17 ON NO-GO	
	3	F87.NG	FMB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	11A1A4A20

27 17	3	T87.NN	TEST FOR FMB REC EN S@0 COMPARE THE B REGISTER TO AFE03FFF BRANCH TO MAJOR 27 MINOR 18 ON NO-GO	
	4	F87.NNG	FMB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	11A1A4A20

27 18	4	T87.NNN	TEST FOR FMB REC EN S@0 COMPARE THE B REGISTER TO AFFFC07F BRANCH TO MAJOR 27 MINOR 19 ON NO-GO	
	5	F87.NNNG	FMB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	11A1A4A20

27 19	5	T87.NNNN	TEST FOR FMB REC EN S@0 COMPARE THE B REGISTER TO AFFFFF8 BRANCH TO MAJOR 27 MINOR 20 ON NO-GO	
	6	F87.NNNNG	FMB REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

27 20 | 6 | T87.NNNNN | TEST FOR FMB REC EN S@0
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 27 MINOR 22 ON NO-GO

7 | F87.NNNNNG | TOTAL FMB REC EN S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A21
		1A1A4A20

27 21 | SPARE

27 22 | 7 | F87.NNNNNN | SINGLE BIT OF FMB REC S@0. SET UP ERROR BIT- DSPL BIT = BIT OF FMB REC S@0
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000	1A1A4A11
NO GO	4000000000	1A1A4A11
NO GO	2000000000	1A1A4A10
NO GO	1000000000	1A1A4A10
NO GO	4000000000	1A1A4A10
NO GO	2000000000	1A1A4A09
NO GO	1000000000	1A1A4A09
NO GO	4000000000	1A1A4A09
NO GO	2000000000	1A1A4A08
NO GO	1000000000	1A1A4A08
NO GO	4000000000	1A1A4A08
NO GO	2000000000	1A1A4A07
NO GO	1000000000	1A1A4A07
NO GO	4000000000	1A1A4A07
NO GO	2000000000	1A1A4A05
NO GO	1000000000	1A1A4A05
NO GO	X000000000	1A1A4A04
NO GO	X000000000	1A1A4A03
NO GO	X000000000	1A1A4A02
NO GO	X000000000	1A1A4A01

27 23 | SPARE
27 24 | SPARE
27 25 | SPARE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
27 26 27 27	1	T88	TEST XMB* DR -> FMB, ROM = AFFFFFFF & DR ENABLED => 0->FMB->0->B REG LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 27 MINOR 28 ON NO-GO BRANCH TO MAJOR 27 MINOR 32	ROM->XMB* DR, FMB->INMX
27 28	2	F88.N	SINGLE BIT OF FMR REC S@1, DSPL BIT = BIT OF FMB REC S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000000 11A1A4A11	
NO GO	4000000000 11A1A4A11	
NO GO	2000000000 11A1A4A10	
NO GO	1000000000 11A1A4A10	
NO GO	4000000011A1A4A10	
NO GO	2000000011A1A4A09	
NO GO	1000000011A1A4A09	
NO GO	4000000 11A1A4A09	
NO GO	2000000 11A1A4A08	
NO GO	1000000 11A1A4A08	
NO GO	4000000 11A1A4A08	
NO GO	2000000 11A1A4A07	
NO GO	1000000 11A1A4A07	
NO GO	4000000 11A1A4A07	
NO GO	2000000 11A1A4A05	
NO GO	1000000 11A1A4A05	
NO GO	X000000 11A1A4A04	
NO GO	X000000 11A1A4A03	
NO GO	X000000 11A1A4A02	
NO GO	X000000 11A1A4A01	

27 29			SPARE	
27 30			SPARE	
27 31			SPARE	
27 32 27 33	1	T89	TEST XMB* DR -> JMA , DR INACTIVE => 1->JMA->1->B REG INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0DBFFFOFFF COMPARE THE B REGISTER TO A007FFF BRANCH TO MAJOR 27 MINOR 37 ON NO-GO BRANCH TO MAJOR 27 MINOR 45	JMA->INMX
27 34			SPARE	
27 35			SPARE	
27 36			SPARE	
27 37	2	T89.N	TEST FOR JMA REC EN S@0 COMPARE THE B REGISTER TO A0000FF BRANCH TO MAJOR 27 MINOR 38 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	3	F89.NG	JMA REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A17

27 38	3	T89.NN	TEST FOR JMA REC EN S@0 COMPARE THE B REGISTER TO A007F BRANCH TO MAJOR 27 MINOR 39 ON NO-GO	
	4	F89.NNG	JMA REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A17

27 39	4	T89.NNN	TEST FOR JMA REC EN S@0 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 27 MINOR 41 ON NO-GO	
	5	F89.NNNG	TOTAL JMA REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A21

27 40			SPARE	
27 41	5	T89.NNNN	SINGLE BIT OF JMA REC S@0. SET UP ERROR BIT- DSPL BIT GIVES SIGNAL QUA0XX (XX=BIT+6) AFFECTED COMPARE THE B REGISTER TO A007FFF STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000011	A1A4A08
NO GO	40000011	A1A4A08
NO GO	20000011	A1A4A07
NO GO	10000011	A1A4A07
NO GO	4000011	A1A4A07
NO GO	2000011	A1A4A05
NO GO	1000011	A1A4A05
NO GO	X0011	A1A4A04
NO GO	X0011	A1A4A03

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

TABLE CONTINUED FROM PRECEEDING PAGE

NO GO	4011A1A4A02
NO GO	2011A1A4A02

27 42 SPARE
27 43 SPARE
27 44 SPARE

27 45 1 T90 TEST XMB* DR -> JMA, ROM = A007FFF0 & DR ENABLED => 0->JMA->0->B REG
27 46 LOAD A REGISTER WITH A007FFF0
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1DBFFF0FFF — ROM->XMB* DR, JMA->INMX
COMPARE THE B PEGISTER TO A
BRANCH TO MAJOR 27 MINOR 47 ON NO-GO
BRANCH TO MAJOR 27 MINOR 51

27 47 2 T90.N SINGLE BIT OF JMA REC S@1- DSPL BIT GIVES SIGNAL QUAOXX (XX=BIT+6)
AFFECTED
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000	11A1A4A08
NO GO	400000	11A1A4A08
NO GO	200000	11A1A4A07
NO GO	100000	11A1A4A07
NO GO	40000	11A1A4A07
NO GO	20000	11A1A4A05
NO GO	10000	11A1A4A05
NO GO	X000	11A1A4A04
NO GO	X00	11A1A4A03
NO GO	40	11A1A4A02
NO GO	20	11A1A4A02

27 48 SPARE
27 49 SPARE
27 50 SPARE

27 51 1 T91 TEST CM* DR -> JCM*, ROM = AFF80000 BUT DR NOT ENABLED => 1->JCM*->0->B
REG
27 52 LOAD A REGISTER WITH AFF80000
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FAFFF0FFF — JCM->INMX
COMPARE THE B PEGISTER TO A
BRANCH TO MAJOR 27 MINOR 53 ON NO-GO
BRANCH TO MAJOR 27 MINOR 68

27 53 2 T91.N TEST CM* DR -> WD3 REC & EXMW REC, ROM = AFF80000 BUT DR NOT ENABLED =>
1->WD3&EXMW->1->B REG

SIGNAL ROUTING:

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			XTM000* -> QUM046 XTM000(1*-4*) -> QUS00(1-4) XTM000(5*-8*) -> QUI00(1-4)	
27 54			LOAD A REGISTER WITH AFF80000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO AFF001 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 27 MINOR 59 ON NO-GO	WD3&JEA&EXMW->INMX MASK OFF OTHER REC INPUTS
27 55	3	F91.NG	SINGLE BIT OF JCM* REC ACTIVE. SET UP ERROR BIT BY REPEATING T91 LOAD A REGISTER WITH AFF80000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFAFFFOFFF COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	JCM->INMX

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	1A1A4A(1,11)	IUM108
NO GO	4000000000	1A1A4A(1,11)	IUM107
NO GO	2000000000	1A1A4A(1,10)	IUM106
NO GO	1000000000	1A1A4A(2,10)	IUM105
NO GO	4000000000	1A1A4A(2,10)	IUM104
NO GO	2000000000	1A1A4A(2,9)	IUM103
NO GO	1000000000	1A1A4A(2,9)	IUM102
NO GO	4000000000	1A1A4A(4,9)	IUM101
NO GO	2000000000	1A1A4A(4,8)	IUM100

27 56			SPARE	
27 57			SPARE	
27 58			SPARE	
27 59	3	T91.NN	TEST FOR CM* DR EN SA1 COMPARE THE B REGISTER TO AF8 BRANCH TO MAJOR 27 MINOR 60 ON NO-GO	
	4	F91.NNG	CM* DR EN SA0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A07

27 60	4	T91.NNN	TEST FOR CM* DR EN SA1 COMPARE THE B REGISTER TO A0F001 BRANCH TO MAJOR 27 MINOR 61 ON NO-GO	
	5	F91.NNNG	CM* DR EN SA0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A07	
27 61	5	T91.NNNN	TEST FOR CM* DR EN S@1 COMPARE THE B REGISTER TO AFF001 BRANCH TO MAJOR 27 MINOR 62 ON NO-GO	
	6	F91.NNNNG	TOTAL CM* DR EN S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(13,21)	
27 62	6	T91.NNNNN	TEST FOR CM* DR EN S@1 COMPARE THE B REGISTER TO A80001 BRANCH TO MAJOR 27 MINOR 64 ON NO-GO	
	7	F91.NNNNNG	CM* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A3A01	
27 63			SPARE	
27 64	7	F91.NNNNNN	SINGLE BIT OF CM* DR S@0. SET UP ERROR BIT- DSPL BIT GIVES SIGNAL S@0, XTMOXX* (XX=BIT-20) COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: XXXXXXXXXXXX / REPLACE ASSEMBLIES: 1A1A2A07	
27 65			SPARE	
27 66			SPARE	
27 67			SPARE	
27 68 27 69	1	T92	TEST CM* DR -> JCM*, ROM = AFF80000 & DR ENABLED => 0->JCM*->1->B REG LOAD A REGISTER WITH AFF80000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF COMPARE THE B REGISTER TO AFF8 BRANCH TO MAJOR 27 MINOR 70 ON NO-GO BRANCH TO MAJOR 27 MINOR 89	ROM->CM DR, JCM->INMX

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
27 70	2	T92.N	TEST CM* DR -> WD3 REC & EXMW REC, ROM = AFF80000 & DR EN => 0->WD3&EXMW->0->B REG SIGNAL ROUTING: XTM000* -> QUM046 XTM000(1*-4*) -> QUS00(1-4) XTM000(5*-8*) -> QUI00(1-4)	
27 71			LOAD A REGISTER WITH AFF80000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AFF001 - RESULT IN B & C REGISTER BRANCH TO MAJOR 27 MINOR 76 ON NO-GO BRANCH TO MAJOR 27 MINOR 83	ROM->CM DR, WD3&EXMW&JMA->INMX MASK OFF OTHER REC INPUTS
27 72			SPARE	
27 73			SPARE	
27 74			SPARE	
27 75			SPARE	
27 76	3	T92.NN	TEST FOR CM* DR EN S@0 COMPARE THE B REGISTER TO AF8 BRANCH TO MAJOR 27 MINOR 77 ON NO-GO	
	4	F92.NNG	CM* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
27 77	4	T92.NNN	TEST FOR CM* DR EN S@0 COMPARE THE B REGISTER TO A0F001 BRANCH TO MAJOR 27 MINOR 78 ON NO-GO	
	5	F92.NNNG	CM* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
27 78	5	T92.NNNN	TEST FOR CM* DR EN S@0 COMPARE THE B REGISTER TO AFF001 BRANCH TO MAJOR 27 MINOR 80 ON NO-GO	
	6	F92.NNNNG	TOTAL CM* DR EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	11A1A2A07

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A17,21

27 79 SPARE

27 80 6 F92.NNNNN
SINGLE BIT OF CM* DR S@1. SET UP ERROR BIT- DSPL BIT GIVES SIGNAL AFFECTED, XTMOXX* (XX=BIT-20)
COMPARE THE B REGISTER TO A
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXXX	1A1A2A07

27 81 SPARE
27 82 SPARE

27 83 3 T92.NG
FAULT IN JCM* REC. REPEAT T92 TO SET UP FAULT BIT PATTERN, TEST FOR JCM* EV S@0
27 84 LOAD A REGISTER WITH AFF80000
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF — ROM->CM DR, JCM->INMX
COMPARE THE B REGISTER TO A
BRANCH TO MAJOR 27 MINOR 85 ON NO-GO

4 F92.NNG
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A17

27 85 4 F92.NNN
SINGLE BIT OF JCM* REC INACTIVE. SET UP ERROR BIT
COMPARE THE B REGISTER TO AFF8
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	1A1A4A(1,11)	IUM108
NO GO	4000000000	1A1A4A(1,11)	IUM107
NO GO	2000000000	1A1A4A(1,10)	IUM106
NO GO	1000000000	1A1A4A(2,10)	IUM105
NO GO	4000000000	1A1A4A(2,10)	IUM104
NO GO	2000000000	1A1A4A(2,9)	IUM103
NO GO	1000000000	1A1A4A(2,9)	IUM102

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO | 40000001 1A1A4A(4,9)	IUM101
			NO GO | 20000001 1A1A4A(4,8)	IUM100
27 86			SPARE	
27 87			SPARE	
27 88			SPARE	
27 89	1	T93	TEST DATA INPUT TO CM* DR FOR S@1. CM* DR -> JCM*, ROM = A0000000 & DR EN	
27 90			LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFF0FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 27 MINOR 92 ON NO-GO BRANCH TO MAJOR 27 MINOR 98	ROM->CM* DR, JCM*->INMX
27 91			SPARE	
27 92	2	F93.N	DATA INPUT TO CM* DR S@1- OSPL BIT GIVES SIGNAL AFFECTED XTMOXX (XX=BIT-20) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | 1A1A2A07	
27 93			SPARE	
27 94			SPARE	
27 95			SPARE	
27 96			SPARE	
27 97			SPARE	
27 98			ENABLE VERTICAL PARITY CHECK	
27 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 28 MINOR 3	
28 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
28 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
28 03	1	T94	TEST CM* DR & QTD DR -> WD3 REC & EXMW REC, DR INACTIVE => 1->B REG SIGNAL ROUTING: XTM000* -> QUM046 XTM000(1*-4*) -> QUS00(1-4) XTM000(5*-8*) -> QUI00(1-4) XTD101 -> QUM041 XTD102 -> QUM045 XTD103 -> QUM044 XTD104* -> QUM047	
28 04			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO AFF003 LOGICALLY 'AND' C REGISTER AND AFF003C8 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 5 ON NO-GO BRANCH TO MAJOR 28 MINOR 25	WD3&JEA&EXMW->INMX MASK OFF OTHER REC INPUTS
28 05	2	T94.N	TEST QTD(101-103) DR -> DOWD, DR INACTIVE SIGNAL ROUTING: XTD101 -> QUD007* XTD102 -> QUD011* XTD103 -> QUD010*	
28 06			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A32 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 28 MINOR 12 ON NO-GO	DOWD & MDPL -> RIM MASK OFF OTHER REC INPUTS
28 07	3	T94.NG	TEST QTD104* DR -> MTW2 REC, DR INACTIVE SIGNAL ROUTING: XTD104* -> QUT021	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO A00008 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 28 MINOR 14 ON NO-GO BRANCH TO MAJOR 28 MINOR 16	MTW2->RIM MASK OFF OTHER REC INPUTS

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 08			SPARE	
28 09			SPARE	
28 10			SPARE	
28 11			SPARE	
28 12	3	F94.NN	SINGLE BIT OF QTD DR S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 2000000001(A1A4A19	XTD102
			INDICATORS: NO GO — DISPLAY: 1000000001(A1A4A19	XTD103
			INDICATORS: NO GO — DISPLAY: 1000000011A1A4A19	XTD101
28 13			SPARE	
28 14	4	F94.NGN	QTD104* DR S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 4000(1A1A4A(19,20)	XTD104*
28 15			SPARE	
28 16	4	T94.NGG	FAULT IN WD3 REC OR EXMW REC. REPEAT T94 TO SET UP FAULT BIT PATTERN, TESTFOR WD3 REC EN S@0	
28 17			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF	WD3&JEA&EXMW->IN4X
			COMPARE THE B REGISTER TO AFF003	
			LOGICALLY 'AND' C REGISTER AND AFF003C8 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			COMPARE THE B REGISTER TO AF	
			BRANCH TO MAJOR 28 MINOR 18 ON NO-GO	
	5	F94.NGGG	WD3 REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — 1(A1A4A19	
28 18	5	T94.NGGN	TEST FOR WD3 REC EN S@0	
			COMPARE THE B REGISTER TO A0F	
			BRANCH TO MAJOR 28 MINOR 19 ON NO-GO	
	6	F94.NGGNG	WD3 REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A19	
28 19	6	T94.NGGNN	TEST FOR WD3 REC EN S@0 COMPARE THE B REGISTER TO AFF BRANCH TO MAJOR 28 MINOR 20 ON NO-GO	
	7	F94.NGGNNG	WD3 REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A19	
28 20	7	T94.NGGNNN	TEST FOR EXMW REC EN S@0 COMPARE THE B REGISTER TO A00003 BRANCH TO MAJOR 28 MINOR 22 ON NO-GO	
	8	F94.NGGNNN --->G	TOTAL EXMW REC EN S@0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A20	
28 21			SPARE	
28 22	8	F94.NGGNNN --->N	SINGLE BIT FAULT IN WD3 REC OR EXMW REC. SET UP ERROR BIT COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1000000000 — REPLACE ASSEMBLIES: 1A1A4A11	QUI014
			INDICATORS: NO GO — DISPLAY: 0400000000 — REPLACE ASSEMBLIES: 1A1A4A11	QUI013
			INDICATORS: NO GO — DISPLAY: 0200000000 — REPLACE ASSEMBLIES: 1A1A4A10	QUI012
			INDICATORS: NO GO — DISPLAY: 0100000000 — REPLACE ASSEMBLIES: 1A1A4A10	QUI011
			INDICATORS: NO GO — DISPLAY: 0040000000 — REPLACE ASSEMBLIES: 1A1A4A10	QUS004
			INDICATORS: NO GO — DISPLAY: 0020000000 — REPLACE ASSEMBLIES: 1A1A4A09	QUS003
			INDICATORS: NO GO — DISPLAY: 0010000000 — REPLACE ASSEMBLIES: 1A1A4A09	QUS002
			INDICATORS: NO GO — DISPLAY: 0004000000 — REPLACE ASSEMBLIES: 1A1A4A09	QUS001
			INDICATORS: NO GO — DISPLAY: 0000100011 — REPLACE ASSEMBLIES: 1A1A4A04	QUM047

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO / 40011A1A4A03	QUM046
			NO GO / 20011A1A4A03	QUM045
			NO GO / 10011A1A4A03	QUM044
			NO GO / 1011A1A4A02	QUM041
28 23			SPARE	
28 24			SPARE	
28 25	1	T95	CM* DR & QTD DR -> WD3 REC & EXMW REC, DR ACTIVE	
			SIGNAL ROUTING:	
			XTM000* -> QUM046	
			XTM000(1*-4*) -> QUS00(1-4)	
			XTM000(5*-8*) -> QUI00(1-4)	
			XTD101 -> QUM041	
			XTD102 -> QUM045	
			XTD103 -> QUM044	
			XTD104* -> QUM047	
28 26			LOAD A REGISTER WITH AFF8	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFF0FFF	ROM->CM DR, WD3&EXMW&JEA->INMX
			COMPARE THE B REGISTER TO A00000C8	
			LOGICALLY 'AND' C REGISTER AND AFF003C8 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 27 ON NO-GO	
			BRANCH TO MAJOR 28 MINOR 37	
28 27	2	T95.N	QTD(101-103) DR -> DOWD REC, DR ACTIVE	
			SIGNAL ROUTING:	
			XTD101 -> QUD007*	
			XTD102 -> QUD011*	
			XTD103 -> QUD010*	
28 28			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBFFF0FDF	EN QTD, DOWD->RIM
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A32 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 31 ON NO-GO	
28 29	3	T95.NG	TEST QTD104* DR -> MTW2 REC, DR ACTIVE	
			SIGNAL ROUTING:	
			XTD104* -> QUT021	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBFFF0FEF	EN QTD, MTW2->RIM
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 33 ON NO-GO	
28 30	4	F95.NGG	SINGLE BIT OF WD3 REC OR EXMW REC AT FAULT. REPEAT T95 TO SET UP ERROR BIT	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK SERIALLY LOAD THE B REGISTER WITH AFF8 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4F8EFF0FFF	ROM->CM DR, WD3&EXMW&JEA->IVMX
			COMPARE THE B REGISTER TO A000000C8 LOGICALLY 'AND' C REGISTER AND AFF003C8 - RESULT IN B & C REGISTER STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	MASK OFF OTHER REC INPUTS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000011A1A4A11		QUI014
NO GO	0100000000011A1A4A11		QUI013
NO GO	0010000000011A1A4A10		QUI012
NO GO	0001000000011A1A4A10		QUI011
NO GO	0000100000011A1A4A10		QUS004
NO GO	0000010000011A1A4A09		QUS003
NO GO	0000001000011A1A4A09		QUS002
NO GO	0000000100011A1A4A09		QUS001
NO GO	0000000010011A1A4A04		QUM047
NO GO	0000000001011A1A4A03		QUM046
NO GO	0000000000111A1A4A03		QUM045
NO GO	0000000000101A1A4A03		QUM044
NO GO	0000000000011A1A4A02		QUM041

28 31	3	F95.NN	SINGLE QTD DR S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	0010000000011A1A4A19		XTD102
NO GO	0001000000011A1A4A19		XTD103
NO GO	0000100000011A1A4A19		XTD101

28 32			SPARE	
28 33	4	F95.NGN	QTD104* DR S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	0000011A1A4A(19,20)		XTD104*

28 34			SPARE	
28 35			SPARE	
28 36			SPARE	
28 37	1	T96	TEST QTD DR -> DOWD REC, DR INACTIVE SIGNAL ROUTING:	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			XTD101 -> QUD007*	
			XTD102 -> QUD011*	
			XTD103 -> QUD010*	
28 38			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF	DOWD & MDPL -> RIM
			COMPARE THE B REGISTER TO A32	
			LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 39 ON NO-GO	
			BRANCH TO MAJOR 28 MINOR 45	
28 39	2	T96.N	TEST FOR DOWD REC EN S@0	
28 40			COMPARE THE B REGISTER TO A32	
			LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 41 ON NO-GO	
28 41	3	F96.NN	SINGLE BIT OF DOWD INACTIVE. SET UP ERROR BIT	
			ENABLE VERTICAL PARITY CHECK	
			COMPARE THE B REGISTER TO A	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	20000000	2A1A2A(19,25)	QUD011*
		2A1A3A30	
NO GO	10000000	2A1A2A(19,25)	QUD010*
		2A1A3A29	
NO GO	10000000	2A1A2A(19,24)	QUD007*
		2A1A3A26	

28 42			SPARE	
28 43			SPARE	
28 44			SPARE	
28 45	1	T97	TEST QTD DR -> DOWD REC, DR ACTIVE	
			SIGNAL ROUTING:	
			XTD101 -> QUD007*	
			XTD102 -> QUD011*	
			XTD103 -> QUD010*	
28 46			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBFFFOFDF	EN QTD, DOWD->RIM
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A32 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 47 ON NO-GO	
			BRANCH TO MAJOR 28 MINOR 51	
28 47	2	F97.N	SINGLE BIT OF DOWD REC ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: 200000000 / REPLACE ASSEMBLIES: 2A1A2A(19,25), 2A1A3A30	QUD011*
			INDICATORS: NO GO / DISPLAY: 100000000 / REPLACE ASSEMBLIES: 2A1A2A(19,25), 2A1A3A29	QUD010*
			INDICATORS: NO GO / DISPLAY: 10000000 / REPLACE ASSEMBLIES: 2A1A2A(19,24), 2A1A3A26	OUD007*
28 48			SPARE	
28 49			SPARE	
28 50			SPARE	
28 51	1	T98	TEST QTD DR -> MTW2 REG, DR ACTIVE	
			SIGNAL ROUTING: XTD104* -> QUT021	
28 52			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBFFFOFEF	EN QTD, MTW2->RIM
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER	MASK OFF OTHER REC INPUTS
			BRANCH TO MAJOR 28 MINOR 53 ON NO-GO	
			BRANCH TO MAJOR 28 MINOR 57	
28 53	2	F98.N	MTW2 BIT 12 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 4000 / REPLACE ASSEMBLIES: 2A1A2A22	QUT021 S@1
28 54			SPARE	
28 55			SPARE	
28 56			SPARE	
28 57	1	T99	TEST DIHR* DR & CFLG* DR & QTD*DR -> MTW2 REG, DR INACTIVE => 1->MTW2->1->B REG	
			SIGNAL ROUTING: XTD(001-018)* -> QUT(037-022)&QUC030; GTC012* -> QUR000; XTD104* -> QUT021	
28 58			LOAD A REGISTER WITH AFFF7800	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF	MTW2->RIM
			COMPARE THE B REGISTER TO AFFFFE	
			BRANCH TO MAJOR 28 MINOR 59 ON NO-GO	
			BRANCH TO MAJOR 28 MINOR 85	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 59 28 60	2	T99.N	TEST DIHR* DR -> DOWD REC, DR INACTIVE LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A0018 LOGICALLY 'AND' C REGISTER AND A0138 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 67 ON NO-GO	DOWD & MDPL -> RIM MASK OFF OTHER REC INPUTS
			TEST DIHR* DR -> JEA*, DR INACTIVE	
			SIGNAL ROUTING: XTD(001-009,018,011)* -> QUA(040-031)* LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 67 ON NO-GO	JEA->RIM MASK OFF OTHER REC
28 61			SPARE	
28 62	4	T99.NGG	TEST CFLG* DR -> MTW1 REC, DR INACTIVE	
			SIGNAL ROUTING: GTC012* -> QUT011 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OF9FFFOFFF COMPARE THE B REGISTER TO A002 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 28 MINOR 76 ON NO-GO	MTW1->INMX MASK OFF OTHER REC INPUTS
28 63	5	T99.NGGG	TEST FOR EN TO,DIHR SINGLE BIT OR PAIR,S@1 LOAD A REGISTER WITH AFFF7800 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A0018 LOGICALLY 'AND' C REGISTER AND A0178 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 79 ON NO-GO LOAD A REGISTER WITH AFFF78 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 79 ON NO-GO	DOWD & MDPL -> RIM MASK OFF OTHER REC INPUTS JEA->RIM MASK OFF OTHER REC
28 64	6	F99.NGGGG	FAULT IN MTW2 REC. REPEAT T99 TO SET UP FAULT BIT PATTERN ENABLE VERTICAL PARITY CHECK LOAD A REGISTER WITH A0000000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AFFFFE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	MTW2->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1777776000	2A1A1A07	AAE051A S@0 OR AAE051B S@0
		2A1A2A09	OR FYR551* S@1
NO GO	1000000000	2A1A2A25	QUT037
NO GO	400000000	2A1A2A25	QUT036
NO GO	200000000	2A1A2A25	QUT035
NO GO	100000000	2A1A2A25	QUT034
NO GO	40000000	2A1A2A24	QUT033
NO GO	20000000	2A1A2A24	QUT032
NO GO	10000000	2A1A2A24	QUT031
NO GO	4000000	2A1A2A24	QUT030
NO GO	2000000	2A1A2A24	QUT029
NO GO	1000000	2A1A2A24	QUT028
NO GO	400000	2A1A2A23	QUT027
NO GO	200000	2A1A2A23	QUT026
NO GO	100000	2A1A2A23	QUT025
NO GO	40000	2A1A2A23	QUT024
NO GO	20000	2A1A2A23	QUT023
NO GO	10000	2A1A2A23	QUT022
NO GO	4000	2A1A2A22	QUT021
NO GO	2000	2A1A2A22	QUC030
NO GO	1000	2A1A2A22	QUB000

28 65 SPARE

28 66 SPARE

28 67 3 T99.NN SINGLE BIT OF DIHR* DR S@0. REPEAT T99 FOR FAULT PATTERN,CHECK SCU SECTIONOF DIHR

28 68
- LOAD A REGISTER WITH A0000000
- INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF — MTW2->RIM
- COMPARE THE B REGISTER TO AFFFFE
- LOGICALLY 'AND' C REGISTER AND A00D7 - RESULT IN B & C REGISTER
- BRANCH TO MAJOR 28 MINOR 69 ON NO-GO
- BRANCH TO MAJOR 28 MINOR 71

28 69 4 F99.NNN SINGLE BIT OF DIHR* DR, SCU SECTION, S@0
- ENABLE VERTICAL PARITY CHECK
- STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXXXX	2A1A2A(7,26)

28 70 SPARE

28 71 4 T99.NNG SINGLE BIT OF LCU SECTION OF DIHR* DR S@0, CHECK BITS 25-28

28 72
- LOAD A REGISTER WITH A0000000
- INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF — MTW2->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO AFFFFE LOGICALLY 'AND' C REGISTER AND AF - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 73 ON NO-GO	
	5	F99.NNGG	SINGLE BIT OF DIHR* OR XTD(006-009,011,018)* S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK | 1A1A2A(18,23) BRANCH TO MAJOR 28 MINOR 93 ON NO-GO	
28 73	5	F99.NNGN	SINGLE BIT OF DIHR* DR XTD(001-004)* S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | XX000000000 | 1A1A2A(17,23)	
28 74			SPARE	
28 75			SPARE	
28 76	5	F99.NGGN	CFLG* OR GTC012* ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | 1000 | 2A1A2A(2,17,20,22,23,24)	
28 77			SPARE	
28 78			SPARE	
28 79 28 80	6	T99.NGGGN	ISOLATE FAULT IN EN DIHR BETWEEN LCU & SCU LOAD A REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AFFFFE LOGICALLY 'AND' C REGISTER AND A00D7 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 81 ON NO-GO	MTW2->RIM
	7	F99.NGGGNG	FAULT IN EN DIHR, LCU SECTION, SINGLE OR PAIR EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A23	
28 81	7	F99.NGGGNN	FAULT IN EN DIHR, SCU SECTION, SINGLE OR PAIR EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX00001 — REPLACE ASSEMBLIES: 2A1A2A07	
28 82			SPARE	
28 83			SPARE	
28 84			SPARE	
28 85 28 86	1	T100	TEST DIHR* DR -> MTW2 REC, DR ACTIVE LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFF78	
	2	F100.1	FAULT LOC WITHIN TEST T100, NOT A PROGRAMMED STOP- CAN NOT RESET KRD031	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000 — REPLACE ASSEMBLIES: 2A1A2A(7,26)	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 87 ON NO-GO BRANCH TO MAJOR 28 MINOR 98	MTW2->RIM
28 87 28 88	2	T100.2	TEST DIHR* DR -> DOWD REC, DR ACTIVE LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFF78 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A016 LOGICALLY 'AND' C REGISTER AND A0138 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 89 ON NO-GO	DOWD & MDPL -> RIM MASK OFF OTHER REC INPUTS
			TEST DIHR* DR -> JEA*, DR ACTIVE INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A00FFC LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 28 MINOR 89 ON NO-GO	JEA->RIM MASK OFF OTHER REC
	3	F100.2.G	SINGLE BIT OF MTW2 REC SOL. REPEAT T100 TO SET UP ERROR BIT ENABLE VERTICAL PARITY CHECK INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AFFFF4 - RESULT IN B & C REGISTER	MTW2->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	12A1A2A25	QUT037
NO GO	4000000000	12A1A2A25	QUT036
NO GO	2000000000	12A1A2A25	QUT035
NO GO	1000000000	12A1A2A25	QUT034
NO GO	400000000	12A1A2A24	QUT033
NO GO	200000000	12A1A2A24	QUT032
NO GO	100000000	12A1A2A24	QUT031
NO GO	40000000	12A1A2A24	QUT030
NO GO	20000000	12A1A2A24	QUT029
NO GO	10000000	12A1A2A24	QUT028
NO GO	4000000	12A1A2A23	QUT027
NO GO	2000000	12A1A2A23	QUT026
NO GO	1000000	12A1A2A23	QUT025
NO GO	400000	12A1A2A23	QUT024
NO GO	200000	12A1A2A23	QUT023
NO GO	100000	12A1A2A23	QUT022
NO GO	40000	12A1A2A22	QUT021
NO GO	20000	12A1A2A22	QUC030
NO GO	10000	12A1A2A22	QUB000

28 89 28 90	3	T100.2.N	TEST FOR DIHR EN S@0. REPEAT T100 TO SET UP FAULT BIT PATTERN INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AFF284 LOGICALLY 'AND' C REGISTER AND AFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 91 ON NO-GO	MTW2->RIM
	4	T100.2.NG	EN OF LCU SECTION OF DIHR S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A19
		12A1A2A26

28 91	4	T100.2.NN	TEST FOR ALL BITS OF DIHR* DR INACTIVE COMPARE THE B REGISTER TO AFFFFE BRANCH TO MAJOR 28 MINOR 95 ON NO-GO	
28 92	5	T100.2.NNG	TEST FOR LDSI -> CLEAR A REG SERIALLY LOAD THE B REGISTER WITH FFFF7800 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFF78 COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 28 MINOR 93 ON NO-GO	
	6	F100.2.NNG --->G	TOTAL EN OF DIHR S@0	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A2A26

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 93	6	F100.2.NNG --->N	FAULT IN LDSI IBT OR FF OR INPUT TO"CL A REG *1" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	377	2A1A1A(1,2) 2A1A2A(7,13) OR PROCEED PER PARAGRAPH 3.6D

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 94			SPARE	
28 95	5	T100.2.NNN	SINGLE BIT OF DIHR* DR S@1, ISOLATE BETWEEN LCU & SCU COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AFF284 - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 96 ON NO-GO	
	6	F100.2.NNN --->G	SINGLE BIT OF SCU SECTION OF DIHR* DR S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A2A(7,26)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
28 96	6	T100.2.NNN --->N	CHECK XTD(001-004)* FOR S@1 LOGICALLY 'AND' C REGISTER AND AF - RESULT IN B & C REGISTER BRANCH TO MAJOR 28 MINOR 97 ON NO-GO	
	7	F100.2.NNN --->NG	SINGLE BIT OF DIHR* DR S@1, XTD(005-009,011,018)* ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(18,23)	
28 97	7	F100.2.NNN --->NN	SINGLE BIT OF XTO(001-004)* Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: XX0000000001 / REPLACE ASSEMBLIES: 1A1A2A(17,23)	
28 98			ENABLE VERTICAL PARITY CHECK	
28 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
29 00	2	F30.4 F154.1	FAULT IN 4SB OF MABC OR BBC738* INPUT TO MBC061 Sa1	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT |2100000000001|A1A1A1A(21,22)	
			PUNCH TAPE LEADER 12 INCHES LONG	
			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 29 MINOR 3	
29 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 02	2	F31.3	CBC436* Sa1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK |1A1A1A(21,23)	
29 03 29 04	1	T101	TEST DATA INPUT TO DIHR FOR Sa1, ROM=A0000000->DIHR* DR->MTW2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AFFFFE BRANCH TO MAJOR 29 MINOR 5 ON NO-GO BRANCH TO MAJOR 29 MINOR 8	MTW2->RIM
29 05 29 06	2	T101.N	ISOLATE FAULT IN DATA INPUT TO DIHR BETWEEN LCU & SCU LOGICALLY 'AND' C REGISTER AND A00D7 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 7 ON NO-GO	
	3	F101.NG	DATA INPUT TO LCU SECTION OF DIHR Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A23	
29 07	3	F101.NN	DATA INPUT TO SCU SECTION OF DIHR Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XX000001 — REPLACE ASSEMBLIES: 2A1A2A07	
29 08	1	T102	TEST CFLG* DR -> MTW2, DR ACTIVE	
			SIGNAL ROUTING: GTC012* -> QU8000	
29 09			SET THE SERIAL INPUT DATA FLAG (GTC012*) INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FEF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 10 ON NO-GO BRANCH TO MAJOR 29 MINOR 13	MTW2->RIM MASK OFF OTHER REC INPUTS
29 10	2	T102.N	TEST GTC012* -> MTW1 (QUT011)	
29 11			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 12 ON NO-GO	MTW1->INMX
	3	F102.NG	QU8000 OF MTW2 REC IS Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A22	
29 12	3	F102.NN	FAULT IN SSID IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 40000012 — REPLACE ASSEMBLIES: 2A1A2A(2,12,17,20,24)	
29 13	1	T103	TEST RESET OF GTC012* WITH RSID	
29 14			RESET THE SERIAL INPUT DATA FLAG (GTC012*) INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0FEF COMPARE THE B REGISTER TO A00002 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	MTW2->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 29 MINOR 15 ON NO-GO BRANCH TO MAJOR 29 MINOR 16	
29 15	2	F103.N	RSID CAN NOT RESET GTC012* TO 1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000	2A1A2A(12,24)

29 16 29 17	1	T104	TEST DIHR* DR -> DOWD, OR INACTIVE LOAD A REGISTER WITH AFFFFF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A0018 LOGICALLY 'AND' C REGISTER AND ACD88F - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 18 ON NO-GO BRANCH TO MAJOR 29 MINOR 23	DOWD & MDPL -> RIM TEST ONLY XTD->QUD&IOD
29 18 29 19	2	T104.N	TEST FOR FAULT IN 28V->LEVEL CONVERTERS FROM WTD013 COMPARE THE B REGISTER TO ACC80F BRANCH TO MAJOR 29 MINOR 20 ON NO-GO	
	3	F104.NG	28V SWITCH WTD013 ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A2A07
		2A1A3A26

29 20	3	F104.NN	SINGLE BIT FAULT IN DOWD REC, IODXXX ACTIVE OR QUD00(1,2) INACTIVE. SET UPERROR BIT COMPARE THE B REGISTER TO A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	2A1A2A(19,25) 2A1A3A26	IOD121
NO GO	400000000	2A1A2A(19,25) 2A1A3A26	IOD021
NO GO	40000000	2A1A2A(19,24) 2A1A3A26	IOD009
NO GO	20000000	2A1A2A(19,24) 2A1A3A26	IOD008

TABLE CONTINUED ON FOLLOWING PAGE

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO | 4000000 | 2A1A2A(19,24)	IOD006
			NO GO | 2000000 | 2A1A2A(19,24) 2A1A3A26	IOD005
			NO GO | 1000000 | 2A1A2A(19,24)	IOD004
			NO GO | 400000 | 2A1A2A(19,23)	IOD003
			NO GO | 200000 | 2A1A2A23	QUD002
			NO GO | 100000 | 2A1A2A23	QUD001
			NO GO | 4000 | 2A1A2A22 2A1A3A29	QUM904
			NO GO | 2000 | 2A1A2A22 2A1A3A29	QUM903
			NO GO | 1000 | 2A1A2A22 2A1A3A30	QUM902
			NO GO | 400 | 2A1A2A22 2A1A3A30	QUM901
29 21			SPARE	
29 22			SPARE	
29 23 29 24	1	T105	TEST DIHR* DR -> DOWD REC , OR ACTIVE LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFFF8 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO ACDEOF LOGICALLY 'AND' C REGISTER AND ACD88F - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 25 ON NO-GO BRANCH TO MAJOR 29 MINOR 31	DOWD & MDPL -> RIM TEST ONLY XTD->QUD&IOD
29 25 29 26	2	T105.N	TEST FOR INACTIVE 28V SWITCH LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFFF8 COMPARE THE B REGISTER TO ACDEOF LOGICALLY 'AND' C REGISTER AND ACD88F - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 27 ON NO-GO	TEST ONLY XTD->QUD&IOD
	3	F105.NG	28V SWITCH WTD013 INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO | DISPLAY: BLANK | REPLACE ASSEMBLIES: 2A1A2A07 / 2A1A3A26 / OR / POWER SUPPLY (PARA 3-21)	
29 27	3	F105.NN	SINGLE BIT FAULT IN DOWD REC, IODXXX INACTIVE OR QUD00(1,2) ACTIVE. SET UP ERROR BIT ENABLE VERTICAL PARITY CHECK INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO ACDEOF	DOWD&MDPL->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOGICALLY 'AND' C REGISTER AND ACDB8F - RESULT IN B & C REGISTER STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	2A1A2A(19,25) 2A1A3A26	IOD121
NO GO	400000000	2A1A2A(19,25) 2A1A3A26	IOD021
NO GO	40000000	2A1A2A(19,24) 2A1A3A26	IOD009
NO GO	20000000	2A1A2A(19,24) 2A1A3A26	IOD008
NO GO	4000000	2A1A2A(19,24)	IOD006
NO GO	2000000	2A1A2A(19,24) 2A1A3A26	IOD005
NO GO	1000000	2A1A2A(19,24)	IOD004
NO GO	400000	2A1A2A(19,23)	IOD003
NO GO	200000	2A1A2A23	QUD002
NO GO	100000	2A1A2A23	QUD001
NO GO	4000	2A1A2A22 2A1A3A29	QUM904
NO GO	2000	2A1A2A22 2A1A3A29	QUM903
NO GO	1000	2A1A2A22 2A1A3A30	QUM902
NO GO	400	2A1A2A22 2A1A3A30	QUM901

29 28			SPARE	
29 29			SPARE	
29 30			SPARE	
29 31	1	T106	TEST DIHR* DR -> JEA*, DR ACTIVE	
29 32			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF	JEA->RIM
			COMPARE THE B REGISTER TO A00FFC	
			LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	MASK OFF OTHER REC
			BRANCH TO MAJOR 29 MINOR 33 ON NO-GO	
			BRANCH TO MAJOR 29 MINOR 39	
29 33	2	T106.N	TEST FOR JEA* REC EN S@0	
29 34			COMPARE THE B REGISTER TO A00FFC	
			BRANCH TO MAJOR 29 MINOR 35 ON NO-GO	
	3	F106.NG	JEA* REC EN S@0	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A18	
29 35	3	F106.NN	SINGLE BIT OF JEA* REC INACTIVE, SET UP ERROR BIT ENABLE VERTICAL PARITY CHECK COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA140
			INDICATORS: NO GO — DISPLAY: 10000001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA139
			INDICATORS: NO GO — DISPLAY: 4000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA138
			INDICATORS: NO GO — DISPLAY: 2000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA137
			INDICATORS: NO GO — DISPLAY: 1000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA136
			INDICATORS: NO GO — DISPLAY: 400001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA135
			INDICATORS: NO GO — DISPLAY: 200001 — REPLACE ASSEMBLIES: 1A1A4A(5,8)	IUA134
			INDICATORS: NO GO — DISPLAY: 100001 — REPLACE ASSEMBLIES: 1A1A4A(5,8)	IUA133
			INDICATORS: NO GO — DISPLAY: 40001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA132
			INDICATORS: NO GO — DISPLAY: 20001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA131
29 36			SPARE	
29 37			SPARE	
29 38			SPARE	
29 39	1	T107	TEST DIHR* DR -> JEA*, DR INACTIVE	
29 40			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00000 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 41 ON NO-GO BRANCH TO MAJOR 29 MINOR 44	JEA->RIM
29 41	2	F107.N	SINGLE BIT OF JEA* REC ACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA140
			INDICATORS: NO GO — DISPLAY: 10000001 — REPLACE ASSEMBLIES: 1A1A4A(4,8)	IUA139
			INDICATORS: NO GO — DISPLAY: 4000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA138
			INDICATORS: NO GO — DISPLAY: 2000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA137
			INDICATORS: NO GO — DISPLAY: 1000001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA136
			INDICATORS: NO GO — DISPLAY: 400001 — REPLACE ASSEMBLIES: 1A1A4A07	IUA135

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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
			NO GO | 20000 | A1A4A(5,8)	IUA134
			NO GO | 10000 | A1A4A(5,8)	IUA133
			NO GO | 4000 | A1A4A(4,8)	IUA132
			NO GO | 2000 | A1A4A(4,8)	IUA131
29 42			SPARE	
29 43			SPARE	
29 44 29 45	1	T108	CFLG* DR -> MTW1 REC, DR INACTIVE RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) LOAD A REGISTER WITH AF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0F9FFF0FFF COMPARE THE B REGISTER TO AFFFFF2 SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) BRANCH TO MAJOR 29 MINOR 46 ON NO-GO BRANCH TO MAJOR 29 MINOR 56	MTW1->INMX
29 46	2	T108.N	TEST FOR MTW1 REC EN S@0 COMPARE THE B REGISTER TO A03FFF2 BRANCH TO MAJOR 29 MINOR 47 ON NO-GO	
	3	F108.NG	MTW1 REC EN S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK | 1A1A4A20	
29 47	3	T108.NN	TEST FOR MTW1 REC EN S@0 COMPARE THE B REGISTER TO AFC0FF BRANCH TO MAJOR 29 MINOR 48 ON NO-GO	
	4	F108.NNG	MTW1 REC EN S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK | 1A1A4A20	
29 48	4	T108.NNN	TEST FOR MTW1 REC EN S@0 COMPARE THE B REGISTER TO AFFF002 BRANCH TO MAJOR 29 MINOR 49 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	5	F108.NNNG	MTW1 REC EN S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A20

29 49	5	T108.NNNN	TEST FOR CFLG* OR EN S@1 COMPARE THE B REGISTER TO A1FFFF2 BRANCH TO MAJOR 29 MINOR 50 ON NO-GO	
	6	F108.NNNNG	ITW151 S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A16,17

29 50	6	T108.NNNNN	TEST FOR CFLG* OR EN S@1 COMPARE THE B REGISTER TO A1FFBF2 BRANCH TO MAJOR 29 MINOR 51 ON NO-GO	
	7	F108.NNNNN --->G	KMV011* S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A3A06

29 51	7	T108.NNNNN --->N	TEST FOR CFLG* OR EN S@1 COMPARE THE B REGISTER TO AFFFFC2 BRANCH TO MAJOR 29 MINOR 52 ON NO-GO	
	8	F108.NNNNN --->NG	CTW114* S@0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A04

29 52 8 T108.NNNNN
--->NN

CHECK FOR FAULT IN GTC021*->QUT016
COMPARE THE B REGISTER TO AFFFEF2
BRANCH TO MAJOR 29 MINOR 53 ON NO-GO

9 F108.NNNNN
--->NNG

ENABLE VERTICAL PARITY CHECK
FAULT IN GTC021*->QUT016. TEST FOR ACTIVE CMA145
SERIALLY LOAD THE B REGISTER WITH AFFFFFFF
INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F1FOFFF — MTW1->INMX->BREG ON BMA165*
SINGLE READ MEMORY MODE-READ MB LINES-ADDRESS 0
COMPARE THE B REGISTER TO A04
LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	BLANK	1A1A2A(9,10,11,16)	CMA145 NOT AT FAULT
		1A1A3A03	
		1A1A4A05	
NO GO	20000000	1A1A3A(1,3)	CMA145 ACTIVE

29 53 9 F108.NNNNN
--->NNN

SINGLE BIT OF CFLG* DR ACTIVE OR MTW1 REC INACTIVE. SET UP ERROR BIT
ENABLE VERTICAL PARITY CHECK
COMPARE THE B REGISTER TO AFFFFF2
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	1A1A2A(12,13)	GTA000* OR QUT001 S@0
		1A1A4A11	
NO GO	400000000	1A1A2A(12,13)	GTE000* OR QUT002 S@0
		1A1A4A11	
NO GO	200000000	1A1A2A(12,13)	GTI000* OR QUT003 S@0
		1A1A4A10	
NO GO	140000000	1A1A3A01	KMA051* S@0
NO GO	100000000	1A1A2A(12,13,19)	GTP000* OR QUT004 S@0
		1A1A4A10	
NO GO	40000000	1A1A2A(13,15,19)	GTM010* OR QUT005 S@0
		1A1A4A10	
NO GO	20000000	1A1A2A(10,11,13)	GTB000* OR QUT006 S@0
		1A1A4A09	

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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			TABLE CONTINUED FROM PRECEEDING PAGE	
		NO GO / 10000000	1A1A2A(9,10,16) 1A1A4A09	GTC002* OR QUT007 Sa0
		NO GO / 4000000	1A1A2A10 1A1A4A09	GTC003* OR QUT008 Sa0
		NO GO / 2000000	1A1A4A08 2A1A2A17	GTC010* OR QUT009 Sa0
		NO GO / 1000000	PROCEED PER PARAGRAPH 3-12D	GTC011* ACTIVE OR QUT010 Sa0
		NO GO / 400000	1A1A4A08	QUT011 Sa0
		NO GO / 200000	1A1A3A(2,9) 1A1A4A07	GTC013* OR QUT012 Sa0
		NO GO / 100000	1A1A2A(6,11,12,16) 1A1A4A07	GTC014* OR QUT013 Sa0
		NO GO / 40000	1A1A2A(11,14,16) 1A1A4A07	GTC020* OR QUT014 Sa0
		NO GO / 4000	1A1A2A(10,11,17) 1A1A3A03 1A1A4A04	GTC022* OR QUT017 Sa0
		NO GO / 2000	1A1A3A02 1A1A4A04	GTW001* OR QUT018 Sa0
		NO GO / 1000	1A1A2A(10,14) 1A1A4A04 OR 1A1A2A04	XTW135* OR QUT019 Sa0
		NO GO / 400	1A1A2A(10,14) 1A1A4A03 OR 1A1A2A04	XTW136* OR QUT020 Sa0

29 54 SPARE

29 55 SPARE

29 56 1 T109 TEST QJD DR -> EXMW REC, ROM = A0000000 & DR INACTIVE

SIGNAL ROUTING:
XTQ021 -> QUM043
XTQ022 -> QUM042
XTQ023 -> QUM040

29 57
LOAD A REGISTER WITH A0
RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*)
INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF — WD3&JEA&EXMW->INMX
COMPARE THE B REGISTER TO A
LOGICALLY 'AND' C REGISTER AND A0000034 - RESULT IN B & C REGISTER
BRANCH TO MAJOR 29 MINOR 58 ON NO-GO
BRANCH TO MAJOR 29 MINOR 62

29 58 2 T109.N TEST FOR QJD DR EN Sa1
29 59
COMPARE THE B REGISTER TO A0000034
BRANCH TO MAJOR 29 MINOR 60 ON NO-GO

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	3	F109.NG	QJD DR EN Sa1 SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A1A07	
29 60	3	F109.NN	SINGLE BIT OF XTQ -> QUM Sa1. SET UP ERROR BIT ENABLE VERTICAL PARITY CHECK SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 40 — REPLACE ASSEMBLIES: 1A1A4A02, 2A1A2A(13,26)	XTQ021 OR QUM043
			INDICATORS: NO GO — DISPLAY: 20 — REPLACE ASSEMBLIES: 1A1A4A02, 2A1A2A(13,26)	XTQ022 OR QUM042
			INDICATORS: NO GO — DISPLAY: 4 — REPLACE ASSEMBLIES: 1A1A4A01, 2A1A2A(13,26)	XTQ023 OR QUM040
29 61			SPARE	
29 62 29 63	1	T110	TEST FOR QJD HOLDING REG EN Sa1 LOAD A REGISTER WITH AF INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0000034 - RESULT IN B & C REGISTER SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) BRANCH TO MAJOR 29 MINOR 64 ON NO-GO BRANCH TO MAJOR 29 MINOR 68	WD3&JEA&EXMW->INMX
29 64	2	F110.N	FAULT IN QJD HOLDING REG DATA DEPENDENT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XX — REPLACE ASSEMBLIES: 2A1A2A13	
29 65			SPARE	
29 66			SPARE	
29 67			SPARE	
29 68	1	T111	TEST QJD DR -> EXMW REC, DR ACTIVE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			SIGNAL ROUTING: XTQ021 -> QUM043 XTQ022 -> QUM042 XTQ023 -> QUM040	
29 69			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBEFF8FFF COMPARE THE B REGISTER TO A0000034 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 29 MINOR 70 ON NO-GO BRANCH TO MAJOR 29 MINOR 76	1->QJD, EXMW->INMX
29 70 29 71	2	T111.N	TEST FOR QJD OR EN SA0 COMPARE THE B REGISTER TO A0000034 BRANCH TO MAJOR 29 MINOR 72 ON NO-GO	
	3	F111.NG	QJD OR EN SA0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 72	3	F111.NN	SINGLE BIT OF XTQ -> QUM SA0. SET UP ERROR BIT ENABLE VERTICAL PARITY CHECK COMPARE THE B REGISTER TO A STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 73 29 74 29 75			SPARE SPARE SPARE	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	40	1A1A4A02 2A1A2A26	XTQ021 OR QUM043
NO GO	20	1A1A4A02 2A1A2A26	XTQ022 OR QUM042
NO GO	4	1A1A4A01 2A1A2A26	XTQ023 OR QUM040

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A1A07

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*****************************************************************************************************
*                                                                                                   *
*                  TEST FOR SHORTS IN EXTERNAL DATA PATHES  T112 - T121  MINOR 76 - 98              *
*                                                                                                   *
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29 76	1	T112	TEST FOR SHORT IN WD1* -> PJB LOAD A REGISTER WITH A8888888 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7	ROM->WD1, PJB->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A7777777 BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	
			LOAD A REGISTER WITH A4444444 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO A8888888 BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
			LOAD A REGISTER WITH A2222222 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO ADDDDDDD BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
			LOAD A REGISTER WITH A1111111 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO AEEEEEEE BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
			LOAD A REGISTER WITH A5A5A5A5 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO AA5A5A5A BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
			LOAD A REGISTER WITH AFF00FF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO A00FF00F BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
			LOAD A REGISTER WITH A00FFFF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 8FBFFF0FF7 COMPARE THE B REGISTER TO AFF0000F BRANCH TO MAJOR 29 MINOR 87 ON NO-GO	ROM->WD1, PJB->RIM
29 77	1	T113	TEST FOR SHORT IN WD1* -> NAD* LOAD A REGISTER WITH A8888888 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO A8888888 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
			LOAD A REGISTER WITH A4444444 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO A4444444 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
			LOAD A REGISTER WITH A2222222 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO A2222222 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
			LOAD A REGISTER WITH A1111111 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFF0FFF COMPARE THE B REGISTER TO A1111111 BRANCH TO MAJOR MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD A REGISTER WITH A5A5A5A5 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFFOFFF COMPARE THE B REGISTER TO A5A5A5A5 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
			LOAD A REGISTER WITH AFF00FF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFFOFFF COMPARE THE B REGISTER TO AFF00FF0 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
			LOAD A REGISTER WITH A00FFFF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 87BFFFOFFF COMPARE THE B REGISTER TO A00FFFF0 BRANCH TO MAJOR 29 MINOR 88 ON NO-GO	ROM->WD1, NAD->INMX
29 78	1	T114	TEST FOR SHORT IN MB -> JEB LOAD A REGISTER WITH A8888888 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A8888888 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH A4444444 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A4444444 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH A2222222 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A2222222 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH A1111111 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A1111111 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH A5A5A5A5 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A5A5A5A5 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH AFF00FF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO AFF00FF0 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
			LOAD A REGISTER WITH A00FFFF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 2BBFFFOFFF COMPARE THE B REGISTER TO A00FFFF0 BRANCH TO MAJOR 29 MINOR 89 ON NO-GO	ROM->MB, JEB->INMX
29 79	1	T115	TEST FOR SHORT IN XMB* -> FMB	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD A REGISTER WITH A8888888	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO A7777777	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH A4444444	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO ABBBBBBB	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH A2222222	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO ADDDDDDD	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH A1111111	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO AEEEEEEE	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH A5A5A5A5	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO AA5A5A5A	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH AFF00FF0	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO A00FF00F	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
			LOAD A REGISTER WITH A00FFFF0	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBBFFOFFF	ROM->XMB, FMB->INMX
			COMPARE THE B REGISTER TO AFF0000F	
			BRANCH TO MAJOR 29 MINOR 90 ON NO-GO	
29 80	1	T116	TEST FOR SHORT IN XMB* -> XMB*	
			LOAD A REGISTER WITH A8888888	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF	ROM->XMB, XMB->INMX
			COMPARE THE B REGISTER TO A8888888	
			BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	
			LOAD A REGISTER WITH A4444444	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF	ROM->XMB, XMB->INMX
			COMPARE THE B REGISTER TO A4444444	
			BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	
			LOAD A REGISTER WITH A2222222	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF	ROM->XMB, XMB->INMX
			COMPARE THE B REGISTER TO A2222222	
			BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	
			LOAD A REGISTER WITH A1111111	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF	ROM->XMB, XMB->INMX

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A1111111 BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	
			LOAD A REGISTER WITH A5A5A5A5 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF COMPARE THE B REGISTER TO A5A5A5A5 BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	ROM->XMB, XMB->INMX
			LOAD A REGISTER WITH AFF00FF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF COMPARE THE B REGISTER TO AFF00FF0 BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	ROM->XMB, XMB->INMX
			LOAD A REGISTER WITH A00FFFF0 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 1FBDFFOFFF COMPARE THE B REGISTER TO A00FFFF0 BRANCH TO MAJOR 29 MINOR 91 ON NO-GO	ROM->XMB, XMB->INMX
29 81	1	T117	TEST FOR SHORT DIHR* -> MTW2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A88840 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO A77774 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A44420 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO ABBBB4 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A22210 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO ADDDD0 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A11108 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AEEEE4 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A48220 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AB7DB0 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A84118 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO A78EC4 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER	MTW2->RIM

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A12800 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AEDF74 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A21440 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO ADE3F4 LOGICALLY 'AND' C REGISTER AND FFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 92 ON NO-GO	MTW2->RIM
29 82	1	T118	TEST FOR SHORT IN INVERTED DOWD LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A0010 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A01 LOGICALLY 'AND' C REGISTER AND A016 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 93 ON NO-GO	DOWD->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A0004 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A004 LOGICALLY 'AND' C REGISTER AND A016 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 93 ON NO-GO	DOWD->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A0002 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFDF COMPARE THE B REGISTER TO A002 LOGICALLY 'AND' C REGISTER AND A016 - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 93 ON NO-GO	DOWD->RIM
29 83	1	T119	TEST FOR SHORT IN IUAXXX OF JEA REC LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A924 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A00924 LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	JEA->INMX
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A490 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A00490 LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	JEA->INMX
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A248 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF COMPARE THE B REGISTER TO A00248 LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	JEA->INMX

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A2A0	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF	JEA->INMX
			COMPARE THE B REGISTER TO A002A0	
			LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A508	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF	JEA->INMX
			COMPARE THE B REGISTER TO A00508	
			LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A850	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBEFFOFFF	JEA->INMX
			COMPARE THE B REGISTER TO A00850	
			LOGICALLY 'AND' C REGISTER AND A00FFC - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 94 ON NO-GO	
29 84	1	T120	TEST FOR SHORT IN CM* -> WD3 & EXMW	
			LOAD A REGISTER WITH AA50	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFFOFFF	ROM->CM, WD3&EXMW->INMX
			COMPARE THE B REGISTER TO A5A001	
			LOGICALLY 'AND' C REGISTER AND AFF001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 95 ON NO-GO	
			LOAD A REGISTER WITH A5A0	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFFOFFF	ROM->CM, WD3&EXMW->INMX
			COMPARE THE B REGISTER TO AA5001	
			LOGICALLY 'AND' C REGISTER AND AFF001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 95 ON NO-GO	
			LOAD A REGISTER WITH A990	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFFOFFF	ROM->CM, WD3&EXMW->INMX
			COMPARE THE B REGISTER TO A66001	
			LOGICALLY 'AND' C REGISTER AND AFF001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 95 ON NO-GO	
			LOAD A REGISTER WITH A008	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FBEFFOFFF	ROM->CM, WD3&EXMW->INMX
			COMPARE THE B REGISTER TO AFF	
			LOGICALLY 'AND' C REGISTER AND AFF001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 29 MINOR 95 ON NO-GO	
29 85	1	T121	TEST FOR SHORT IN IUMXXX OF JCM* REC	
			LOAD A REGISTER WITH AA50	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF	ROM->CM, JCM->INMX
			COMPARE THE B REGISTER TO AA5	
			BRANCH TO MAJOR 29 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH A5A0	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF	ROM->CM, JCM->INMX
			COMPARE THE B REGISTER TO A5A	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 29 MINOR 96 ON NO-GO	
			LOAD A REGISTER WITH A990 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF COMPARE THE B REGISTER TO A99 BRANCH TO MAJOR 29 MINOR 96 ON NO-GO	ROM->CM, JCM->INMX
			LOAD A REGISTER WITH A008 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 4FAFFFOFFF COMPARE THE B REGISTER TO A008 BRANCH TO MAJOR 29 MINOR 96 ON NO-GO	ROM->CM, JCM->INMX
			BRANCH TO MAJOR 29 MINOR 98	
29 86			SPARE	
29 87	2	F112.N	SHORT IN WD1* -> PJB STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 88	2	F113.N	SHORT IN IUD(131-158) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 89	2	F114.N	SHORT IN MB -> JEB STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 90	2	F115.N	SHORT IN XMB* -> FMB STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 91	2	F116.N	SHORT IN ITB(141- 168) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 92	2	F117.N	SHORT IN DIHR* -> MTW2 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 93	2	F118.N	SHORT IN IODXXX OF DOWD REC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 94	2	F119.N	SHORT IN IUAXXX OF JEA* REC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 95	2	F120.N	SHORT IN CM* -> WD3 & EXMW STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
29 96	2	F121.N	SHORT IN IUMXXX OF JCM* REC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
29 97			SPARE	
29 98			ENABLE VERTICAL PARITY CHECK	
29 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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*****************************************************************************************
*                                                                                       *
*                                COMPUTER LOAD CONTROL TESTS                            *
*                                                                                       *
*                                     MAJOR 30 AND 31                                   *
*                                                                                       *
*****************************************************************************************

30 00                       INITIALIZE
                              DEFINE SELF TEST TAPE
                              ENABLE LOW LEVEL ON GTC001*
                              BRANCH TO MAJOR 30 MINOR 3

30 01                         STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

30 02   2       T30.5       FAULT IN ENABLE OF ROM
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
                                    ---------------------------------------------
                                    | INDICATORS | DISPLAY |  REPLACE ASSEMBLIES |
                                    | NO GO      | BLANK   | 2A1A1A19            |
                                    ---------------------------------------------

30 03   1       T125        TEST RESET OF TST2 WITH LQJD
                            PREVIOUS TEST = (29)T121
30 04                         RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE
                                (GTC003*)
                              SERIALLY LOAD THE B REGISTER WITH AFFFFFFF
                              INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF      SIM NO-GO
                              ENABLE AF TO THE QJD LINES

        2       F125.1      FAULT LOC WITHIN TEST T125, NOT A PROGRAMMED STOP- LQJD LATCH NOT RESET
                                    ---------------------------------------------
                                    | INDICATORS | DISPLAY |  REPLACE ASSEMBLIES |
                                    | TEST SET FAULT | 10000 | PROCEED PER PARAGRAPH 3-12D |
                                    ---------------------------------------------

        1       T125(CONT)            BRANCH TO MAJOR 30 MINOR 6  ON NO-GO
                                      BRANCH TO MAJOR 30 MINOR 10

30 05                       SPARE

30 06   2       F125.2      FAULT IN LQJD IBT OR LATCH, OR RESET OF TST2
                              ENABLE VERTICAL PARITY CHECK
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(1,12,13) 2A1A3A16	
30 07			SPARE	
30 08			SPARE	
30 09			SPARE	
30 10 30 11	1	T126	TEST FOR LOAD OF B REG COMPARE THE B REGISTER TO A BRANCH TO MAJOR 30 MINOR 13 ON NO-GO BRANCH TO MAJOR 30 MINOR 17	
30 12			SPARE	
30 13	2	F126.N	INPUT TO GYR742 S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 17777777777 / REPLACE ASSEMBLIES: 2A1A3A15	
30 14			SPARE	
30 15			SPARE	
30 16			SPARE	
30 17 30 18	1	T127	TEST LOAD OF QJD HOLDING REG INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBEFFOFFF ENABLE AF TO THE QJD LINES COMPARE THE B REGISTER TO A0000034 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 30 MINOR 20 ON NO-GO BRANCH TO MAJOR 30 MINOR 24	EXMW->INMX, INMX->BREG ON RESET QJD
30 19			SPARE	
30 20	2	F127.N	FAULT IN QJD HOLDING REG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: XX12A1A2A13 — REPLACE ASSEMBLIES	
30 21			SPARE	
30 22			SPARE	
30 23			SPARE	
30 24	1	T128	TEST FOR DATA INPUTS TO QJD HOLDING REG S@1	
30 25			ENABLE A TO THE QJD LINES COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0000034 - RESULT IN B & C REGISTER BRANCH TO MAJOR 30 MINOR 27 ON NO-GO BRANCH TO MAJOR 30 MINOR 31	
30 26			SPARE	
30 27	2	F128.N	DATA INPUT TO QJD HOLDING REG S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XX12A1A2A13 — REPLACE ASSEMBLIES	
30 28			SPARE	
30 29			SPARE	
30 30			SPARE	
30 31	1	T129	TEST "GEN LOAD" RESET OF TST2	
30 32			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 07BFFF4FFF	NAD->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) PULSE CA DRIVERS WITH 0000007	
	2	F129.1	FAULT LOC WITHIN TEST T129, NOT A PROGRAMMED FAULT- LDCA LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000000 — REPLACE ASSEMBLIES: 1A1A2A(11,12,25) 1A1A3A23	
	1	T129(CONT)	BRANCH TO MAJOR 30 MINOR 33 ON NO-GO BRANCH TO MAJOR 30 MINOR 41	
30 33	2	T129.2	TEST LXMB => GEN LOAD RESET OF TST2	
30 34			PULSE THE XMB DRIVERS WITH THE A REGISTER	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 30 MINOR 35 ON NO-GO	
	3	F129.2.G	FAULT IN LDCA IBT, LATCH, OR GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(10,12,13,17)	
30 35 30 36	3	T129.2.N	TEST CLEAR EN RESET OF TST2 SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3FFF4FFF PULSE CA DRIVERS WITH THE A REGISTER BRANCH TO MAJOR 30 MINOR 37 ON NO-GO	RESET TST2 SIM NO-GO, RESET TST2 ON CLEAR EN
	4	F129.2.NG	FAULT IN GEN LOAD RESET OF TST2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(19,21); 1A1A3A15	ATL521* S@1
30 37	4	F129.2.NN	ATL301* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A12	
30 38			SPARE	
30 39			SPARE	
30 40			SPARE	
30 41 30 42	1	T130	TEST LDCA CONTROL COMPARE THE B REGISTER TO A0000007 BRANCH TO MAJOR 30 MINOR 43 ON NO-GO BRANCH TO MAJOR 30 MINOR 51	
30 43 30 44	2	T130.N	TEST FOR FAULT IN "SHORT DATA EN" INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 078FFF0FFF PULSE CA DRIVERS WITH 00000007 COMPARE THE B REGISTER TO A0000007 BRANCH TO MAJOR 30 MINOR 47 ON NO-GO	NAD->INMX, INMX->BREG ON LOAD EN

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
30 45	3	T130.NG	TEST FOR NO CLEAR OF AREG LOAD A REGISTER WITH AFFFE INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 078FFFOFFF PULSE CP DRIVERS WITH F COMPARE THE B REGISTER TO AFFFE BRANCH TO MAJOR 30 MINOR 46 ON NO-GO	NAD->INMX, INMX->BREG ON LOAD EN
	4	F130.NGG	ITL211* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A3A24	
30 46	4	F130.NGN	INPUT TO BRA101 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: 77760001; REPLACE ASSEMBLIES: 1A1A3A07	
30 47	3	F130.NN	ATA103* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: 7; REPLACE ASSEMBLIES: 1A1A2A(9,13)	
30 48			SPARE	
30 49			SPARE	
30 50			SPARE	
30 51 30 52	1	T131	TEST CL CA => GTA000*->MTW1 SERIALLY LOAD THE B REGISTER WITH AF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1FFFOFFF PULSE CA DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A8 - RESULT IN B & C REGISTER BRANCH TO MAJOR 30 MINOR 53 ON NO-GO BRANCH TO MAJOR 30 MINOR 59	MTW1->INMX, INMX->BREG ON CLEAR EN
30 53 30 54	2	T131.N	TEST CL CE => GTE000*->MTW1 SERIALLY LOAD THE B REGISTER WITH AF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1FFFOFFF	MTW1->INMX, INMX->BREG ON CLEAR EN

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PULSE CE DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 30 MINOR 55 ON NO-GO	
	3	F131.NG	FAULT IN GTA000*->OUT001 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(12,13), 1A1A4A11	
30 55	3	F131.NN	ATL421* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 400000000 / REPLACE ASSEMBLIES: 1A1A2A(19,21), 1A1A3A15	
30 56			SPARE	
30 57			SPARE	
30 58			SPARE	
30 59 30 60	1	T132	TEST LOCE RESET TST2 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 07BFFF4FFF PULSE CE DRIVERS WITH 00000F8	NAD->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
	2	F132.1	FAULT LOC WITHIN TEST T132 , NOT A PROGRAMMED STOP- LOCE LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 100000000 / REPLACE ASSEMBLIES: 1A1A2A13	
	1	T132(CONT)	BRANCH TO MAJOR 30 MINOR 62 ON NO-GO BRANCH TO MAJOR 30 MINOR 66	
30 61			SPARE	
30 62	2	F132.2	LOCE IBT OR LATCH FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(10,13,17)	
30 63			SPARE	
30 64			SPARE	
30 65			SPARE	
30 66	1	T133	TEST LOCE CONTROL	
30 67			COMPARE THE B REGISTER TO A00000F8 BRANCH TO MAJOR 30 MINOR 69 ON NO-GO BRANCH TO MAJOR 30 MINOR 73	
30 68			SPARE	
30 69	2	F133.N	ATE103* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 370(1A1A2A(9,13)	
30 70			SPARE	
30 71			SPARE	
30 72			SPARE	
30 73	1	T134	TEST CL CE => GTE000*->QUT002(MTW1)	
30 74			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1FFF0FFF PULSE CE DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 30 MINOR 76 ON NO-GO BRANCH TO MAJOR 30 MINOR 79	MTW1->INMX, INMX->BREG ON CLEAR EN
30 75			SPARE	
30 76	2	F134.N	FAULT IN GTE000* -> QUT002 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 400000000 — REPLACE ASSEMBLIES: 1A1A2A(12,13) 1A1A4A11	
30 77			SPARE	
30 78			SPARE	
30 79	1	T135	TEST LDCI RESET OF TST2	
30 80			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 07BFFF4FFF	NAD->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			PULSE CI DRIVERS WITH 0001F00	
	2	F135.1	FAULT LOC WITHIN TEST T135 , NOT A PROGRAMMED STOP- LDCI LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 100000000 — REPLACE ASSEMBLIES: 1A1A2A13	
	1	T135(CONT)	BRANCH TO MAJOR 30 MINOR 82 ON NO-GO	
			BRANCH TO MAJOR 30 MINOR 85	
30 81			SPARE	
30 82	2	F135.2	LDCI IBT OR LATCH FAULT	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(10,13,16)	
30 83			SPARE	
30 84			SPARE	
30 85	1	T136	TEST LDCI CONTROL	
30 86			COMPARE THE B REGISTER TO A0001F	
			BRANCH TO MAJOR 30 MINOR 88 ON NO-GO	
			BRANCH TO MAJOR 30 MINOR 91	
30 87			SPARE	
30 88	2	F136.N	ATI103* sa1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: 17400 / REPLACE ASSEMBLIES: 1A1A2A(9,13)	
30 89			SPARE	
30 90			SPARE	
30 91	1	T137	TEST CL CI => GTI000*->QUT003(MTW1)	
30 92			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FFFOFFF	MTW1->INMX, INMX->BREG ON CLEAR EN
			PULSE CI DRIVERS WITH THE A REGISTER	
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A2 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 30 MINOR 94 ON NO-GO	
			BRANCH TO MAJOR 30 MINOR 98	
30 93			SPARE	
30 94	2	F137.N	FAULT IN GTI000*->QUT003	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 200000000 / REPLACE ASSEMBLIES: 1A1A2A(12,13) 1A1A4A10	
30 95			SPARE	
30 96			SPARE	
30 97			SPARE	
30 98			ENABLE VERTICAL PARITY CHECK	
30 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
31 00			INITIALIZE DEFINE SELF TEST TAPE ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 31 MINOR 3	
31 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
31 02	2	F31.4 F192.1	C8C335* Sa1 OR ABS115 Sa0 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
31 03 31 04	1	T138	TEST LOCP RESET OF TST2 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 07BFFF4FFF PULSE CP DRIVERS WITH FFFE	NAD->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
	2	F138.1	FAULT LOC WITHIN TEST T138 , NOT A PROGRAMMED STOP- LOCP LATCH NOT RESET	
	1	T138(CONT)	BRANCH TO MAJOR 31 MINOR 6 ON NO-GO BRANCH TO MAJOR 31 MINOR 9	
31 05			SPARE	
31 06	2	F138.2	FAULT IN LOCP IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
31 07 31 08			SPARE SPARE	
31 09 31 10	1	T139	TEST LOCP CONTROL COMPARE THE 8 REGISTER TO AFFFE BRANCH TO MAJOR 31 MINOR 12 ON NO-GO BRANCH TO MAJOR 31 MINOR 15	
31 11			SPARE	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A1A(21,22,23)

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SET FAULT	10000000	1A1A2A13

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A2A(10,13,17)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
31 12	2	F139.N	ATP103* Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 17777600001A1A2A(4,13)	
31 13			SPARE	
31 14			SPARE	
31 15 31 16	1	T140	TEST CLEAR OF AREG DURING GEN LOAD LOAD A REGISTER WITH AFFFE INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 078FFF0FFF PULSE CP DRIVERS WITH F COMPARE THE B REGISTER TO AF BRANCH TO MAJOR 31 MINOR 18 ON NO-GO BRANCH TO MAJOR 31 MINOR 21	NAD->INMX, INMX->BREG ON LOAD EN
31 17			SPARE	
31 18	2	F140.N	IAR029* Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 77760000 — REPLACE ASSEMBLIES: 1A1A3A(12,14) 12A1A2A17	
31 19			SPARE	
31 20			SPARE	
31 21 31 22	1	T141	TEST CL CP -> MTW1 => GTP000*->QUT004 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1FFF0FFF PULSE CP DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A1 - RESULT IN B & C REGISTER BRANCH TO MAJOR 31 MINOR 24 ON NO-GO BRANCH TO MAJOR 31 MINOR 27	MTW1->INMX, INMX->BREG ON CLEAR EN
31 23			SPARE	
31 24	2	F141.N	FAULT IN GTP000*->QUT004 ENABLE VERTICAL PARITY CHECK	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 100000000 / REPLACE ASSEMBLIES: 1A1A2A(12,13,19) 1A1A4A10	
31 25			SPARE	
31 26			SPARE	
31 27	1	T142	TEST LDCM RESET TST2	
31 28			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFAFFF4FFF	JCM->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			PULSE THE CM DRIVERS WITH FF8	
	2	F142.1	FAULT LOC WITHIN TEST T142 , NOT A PROGRAMMED STOP- LDCM LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 100000000 / REPLACE ASSEMBLIES: 1A1A2A13	
	1	T142(CONT)	BRANCH TO MAJOR 31 MINOR 30 ON NO-GO	
			BRANCH TO MAJOR 31 MINOR 33	
31 29			SPARE	
31 30	2	F142.2	FAULT IN LDCM IBT OR LATCH, OR GATING	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A(10,12,13,17)	
31 31			SPARE	
31 32			SPARE	
31 33	1	T143	TEST LDCM CONTROL	
31 34			COMPARE THE B REGISTER TO AFF8	
			BRANCH TO MAJOR 31 MINOR 35 ON NO-GO	
			BRANCH TO MAJOR 31 MINOR 40	
31 35	2	T143.N	TEST FOR CM DR EN SA0	
			COMPARE THE B REGISTER TO A0F8	
			BRANCH TO MAJOR 31 MINOR 36 ON NO-GO	
	3	F143.NG	FAULT IN CM DR EN	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A07	
31 36	3	T143.NN	TEST FOR CM DR EN S@0 COMPARE THE B REGISTER TO AF BRANCH TO MAJOR 31 MINOR 37 ON NO-GO	
	4	F143.NNG	FAULT IN CM DR EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A07	
31 37	4	F143.NNN	ATM103* S@1 ENABLE VERTICAL PARITY CHECK COMPARE THE B REGISTER TO AFF8 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1776000000 / REPLACE ASSEMBLIES: 1A1A2A13	
31 38			SPARE	
31 39			SPARE	
31 40	1	T144	TEST CL CM -> MTW1 => GTM010*->QUT005	
31 41			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1FFF0FFF PULSE THE CM DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A08 - RESULT IN B & C REGISTER BRANCH TO MAJOR 31 MINOR 43 ON NO-GO BRANCH TO MAJOR 31 MINOR 46	MTW1->INMX, INMX->BREG ON CLEAR EN
31 42			SPARE	
31 43	2	F144.N	FAULT IN GTM010* -> QUT005 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 40000000 — REPLACE ASSEMBLIES: 1A1A2A(13,15,19) 1A1A4A10	
31 44			SPARE	
31 45			SPARE	
31 46	1	T145	TEST LDMB RESET OF TST2	
31 47			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0EBFFF4FFF	WD1->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			PULSE THE MB DRIVERS WITH FFFFFFF	
	2	F145.1	FAULT LOC WITHIN TEST T145 , NOT A PROGRAMMED STOP- LDMB LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000000 — REPLACE ASSEMBLIES: 1A1A2A13	
	1	T145(CONT)	BRANCH TO MAJOR 31 MINOR 49 ON NO-GO	
			BRANCH TO MAJOR 31 MINOR 52	
31 48			SPARE	
31 49	2	F145.2	FAULT IN LDMB IBT OR LATCH, OR IN INST DECODE MATRIX	
			ENABLE VERTICAL PARITY CHECK	
			PUNCH TAPE CODES - /9 /E &C	INVALID INST = 3/5/1 OCTAL
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: TEST SET FAULT — DISPLAY: 40000000 — REPLACE ASSEMBLIES: 1A1A2A(10,13,17)	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-12D	
31 50			SPARE	
31 51			SPARE	
31 52	1	T146	TEST LDMB CONTROL	
31 53			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 31 MINOR 55 ON NO-GO	
			BRANCH TO MAJOR 31 MINOR 58	
31 54			SPARE	
31 55	2	F146.N	ATB203* S@1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A(4,13)	
31 56			SPARE	
31 57			SPARE	
31 58	1	T147	TEST CL MB -> MTW1 => GTB000*->QUT006	
31 59			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FFFOFFF	MTW1->INMX, INMX->BREG ON CLEAR EN
			PULSE THE MB DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A04 - RESULT IN B & C REGISTER BRANCH TO MAJOR 31 MINOR 61 ON NO-GO BRANCH TO MAJOR 31 MINOR 64	
31 60			SPARE	
31 61	2	F147.N	FAULT IN GTB000*->QUT006 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000000 — REPLACE ASSEMBLIES: 1A1A2A(10,11,13) 1A1A4A09	
31 62			SPARE	
31 63			SPARE	
31 64	1	T148	TEST LXMB RESET OF TST2	
31 65			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF8DFF4FFF	XMB->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			PULSE THE XMB DRIVERS WITH FFFFFFF	
	2	F148.1	FAULT LOC WITHIN TEST T148 , NOT A PROGRAMMED STOP- LDXM LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000000 — REPLACE ASSEMBLIES: 1A1A2A13	
			BRANCH TO MAJOR 31 MINOR 67 ON NO-GO	
	1	T148(CONT)	BRANCH TO MAJOR 31 MINOR 70	
31 66			SPARE	
31 67	2	F148.2	FAULT IN LXMB IBT OR LATCH	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A(10,13,17)	
31 68			SPARE	
31 69			SPARE	
31 70	1	T149	TEST LXMB CONTROL	
31 71			COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 31 MINOR 73 ON NO-GO BRANCH TO MAJOR 31 MINOR 76	
31 72			SPARE	
31 73	2	F149.N	ATX103* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A(4,13)	
31 74			SPARE	
31 75			SPARE	
31 76	1	T150	TEST LXMB => CL MB -> MTW1	
31 77			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FFFOFFF	MTW1->INMX, INMX->BREG ON CLEAR EN
			PULSE THE XMB DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A04 - RESULT IN B & C REGISTER BRANCH TO MAJOR 31 MINOR 79 ON NO-GO BRANCH TO MAJOR 31 MINOR 82	
31 78			SPARE	
31 79	2	F150.N	ATX102* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | 20000000 | 1A1A2A(10,13)	
31 80			SPARE	
31 81			SPARE	
31 82	1	T151	TEST LDW1 RESET OF TST2	
31 83			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 078FFF4FFF	NAD->INMX, INMX->BREG ON LOAD EN, SIM NO-GO
			PULSE THE WORD 1 DRIVERS WITH FFFFFFF	
	2	F151.1	FAULT LOC WITHIN TEST T151 , NOT A PROGRAMMED STOP- LDW1 LATCH NOT RESET	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 10000000 | 1A1A2A13	
	1	T151(CONT)	BRANCH TO MAJOR 31 MINOR 85 ON NO-GO BRANCH TO MAJOR 31 MINOR 87	
31 84			SPARE	
31 85	2	F151.2	FAULT IN LDW1 IBT OR LATCH, OR INST DECODE MATRIX ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /0 /E &C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	INVALID INST = OCTAL 3/4/0
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 40000000 | 1A1A2A(10,13,17) NO GO | BLANK | PROCEED PER PARAGRAPH 3-12D	
31 86			SPARE	
31 87	1	T152	TEST LDW1 CONTROL	
31 88			COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 31 MINOR 90 ON NO-GO BRANCH TO MAJOR 31 MINOR 92	
31 89			SPARE	
31 90	2	F152.N	ATW103* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 177777777711A1A2A(4,12) — REPLACE ASSEMBLIES	
31 91			SPARE	
31 92	1	T153	TEST CL WD1 -> MTW1	
31 93			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FFFOFFF	MTW1->INMX, INMX->BREG ON CLEAR EN
			PULSE THE WORD 1 DRIVERS WITH THE A REGISTER COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND AF - RESULT IN B & C REGISTER BRANCH TO MAJOR 31 MINOR 95 ON NO-GO BRANCH TO MAJOR 31 MINOR 98	
31 94			SPARE	
31 95	2	F153.N	FAULT IN CL WD1 EN OF CFLG DR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			NO GO — 170000000011A1A2A13	ATW102* Sa1
			NO GO — 160000000011A1A2A(6,17)	ITW151* Sa1
			NO GO — 100000000011A1A2A12	INPUT TO ATA100 Sa1
			NO GO — 400000000011A1A2A12	INPUT TO ATE100 Sa1
			NO GO — 200000000011A1A2A12	INPUT TO ATI100 Sa1
			NO GO — 100000000011A1A2A19	INPUT TO CTP100 Sa1
31 96			SPARE	
31 97			SPARE	
31 98			ENABLE VERTICAL PARITY CHECK	
31 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
32 00			BRANCH TO MAJOR 32 MINOR 3	
32 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
32 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
32 03	1	T154	TEST INPUT TO MBC061 FOR S@1 BRANCH TO MAJOR 33 MINOR 1	
32 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
33 00	2	F30.6	FAULT IN 6SB OF MABC	
			INDICATORS: TEST SET FAULT; DISPLAY: 210000000000; REPLACE ASSEMBLIES: 1A1A1A23	
			PUNCH TAPE LEADER 12 INCHES LONG	
			BRANCH TO MAJOR 33 MINOR 3	
33 01			BRANCH TO MAJOR 33 MINOR 3	
33 02	2	F30.7	FAULT IN 6SB OF MABC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A1A(22,23)	
33 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
34 00			BRANCH TO MAJOR 34 MINOR 3	
34 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
34 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
34 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			**********	
			* COMPUTER MONITOR CONTROL TESTS- TEST OF ALL"READ AND COMPARE"FUNCTIONS *	
			* MAJORS 35, 36, AND 37 *	
			**********	
35 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 35 MINOR 3	
35 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
35 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
35 03	1	T155	TEST RCAA, NO ITERATION PREVIOUS TEST = (32)T154	
35 04			SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFFOFFF READ & COMPARE THE NAD LINES WITH AFFFFFFF; PULSE XTD101	ROM->WD1 DR
	2	F155.1	FAULT LOC WITHIN TEST T155, NOT A PROGRAMMED STOP- IN PROCESS FAULT DETECTED	
			INDICATORS: TEST SET FAULT — DISPLAY: 1000000 — REPLACE ASSEMBLIES: 1A1A4A15 2A1A1A(1,14,17) INDICATORS: TEST SET FAULT — DISPLAY: 2000 — REPLACE ASSEMBLIES: 2A1A1A02	
	1	T155(CONT)	BRANCH TO MAJOR 35 MINOR 5 ON NO-GO BRANCH TO MAJOR 35 MINOR 11	
35 05	2	T155.2	TEST RCXM TO ISOLATE EN FAULT	
35 06			SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 1FBFFFOFFF READ & COMPARE THE XMB LINES WITH AFFFFFFF BRANCH TO MAJOR 35 MINOR 7 ON NO-GO	ROM->XMB DR
	3	F155.2.G	AAC212* Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A16	
35 07	3	F155.2.N	"NCU->STE B.T.*" INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 2A1A1A(2,3)	AAR065* S@1
35 08			SPARE	
35 09			SPARE	
35 10			SPARE	
35 11 35 12	1	T156	TEST RESULT OF RCAA COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 35 MINOR 13 ON NO-GO BRANCH TO MAJOR 35 MINOR 21	
35 13 35 14	2	T156.N	TEST R&C GATING WITH RCXM SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 1FBFFFOFFF READ & COMPARE THE XMB LINES WITH AFFFFFFF COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 35 MINOR 17 ON NO-GO	ROM->XMB DR
35 15	3	T156.NG	TEST R&C GATING FURTHER WITH RCW1 SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFFOFFF READ & COMPARE WORD 1 WITH AFFFFFFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 35 MINOR 16 ON NO-GO	ROM->WD1 DR
	4	F156.NGG	FAULT IN RCAA IBT OR LATCH, OR INST DECODE MATRIX ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /6 /F &C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT — DISPLAY: 40000000 — REPLACE ASSEMBLIES: 1A1A2A17, 1A1A4A(15,16)	
			INDICATORS: NO GO — DISPLAY: BLANK — PROCEED PER PARAGRAPH 3-12D	INST DECODE MATRIX
35 16	4	F156.NGN	FAULT IN LCU R&C GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 17777777771 — REPLACE ASSEMBLIES: 1A1A4A(16,19)	IAC112* Sa1
35 17 35 18	3	T156.NN	ISOLATE R&C FAULT BETWEEN LCU & SCU SERIALLY LOAD THE B REGISTER WITH A READ & COMPARE PJB LINES WITH AFFFFFFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 35 MINOR 19 ON NO-GO	
	4	F156.NNG	FAULT IN LCU->SCU R&C GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A19, 2A1A1A01	IAC330* Sa1
35 19	4	F156.NNN	FAULT IN SCU R&C GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 17777777772 — REPLACE ASSEMBLIES: 2A1A1A(1,2)	IAR025* Sa1
35 20			SPARE	
35 21 35 22	1	T157	TEST "DISPLAY AA" => XTD101->QUM041 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBEFFOFFF READ & COMPARE THE NAD LINES WITH A0000008; PULSE XTD101 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 35 MINOR 24 ON NO-GO BRANCH TO MAJOR 35 MINOR 26	EXMW->INMX
35 23			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
35 24	2	F157.N	FAULT IN EN "DISPLAY AA" STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 10 / REPLACE ASSEMBLIES: 1A1A4A(16,19)	
35 25			SPARE	
35 26 35 27	1	T158	TEST RCAA, WITH ITERATION SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF07FF READ & COMPARE THE NAD LINES WITH A; PULSE XTD101	BREG->ROM, ROM->WD1 DR SHOULD RESULT IN NO-GO, CREG=0FFFFFFF
	2	F158.1	FAULT LOC WITHIN TEST T158, NOT A PROGRAMMED STOP- IN PROCESS FAULT DETECTED	
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 2A1A1A(5,9,10,13,14,17)	
			INDICATORS: TEST SET FAULT / DISPLAY: 400 / REPLACE ASSEMBLIES: 2A1A1A(9,10,13,14,17)	
	1	T158(CONT)	BRANCH TO MAJOR 35 MINOR 31 ON NO-GO BRANCH TO MAJOR 35 MINOR 29	
35 28			SPARE	
35 29	2	F158.2	FAULT IN ITERATION CONTROL ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A(13,14,17)	
35 30			SPARE	
35 31 35 32	1	T159	TEST RCAM, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF07FF READ & COMPARE THE NAD LINES WITH A; PULSE XTD102	BREG->ROM, ROM->WD1 DR
	2	F159.1	FAULT LOC WITHIN TEST 159, NOT A PROGRAMMED STOP- RCAM LATCH NOT RESET	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A15	
	1	T159(CONT)	BRANCH TO MAJOR 35 MINOR 38 ON NO-GO BRANCH TO MAJOR 35 MINOR 34	
35 33			SPARE	
35 34	2	F159.2	FAULT IN RCAM IBT, LATCH, ETC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
35 35			SPARE	
35 36			SPARE	
35 37			SPARE	
35 38 35 39	1	T160	TEST "DISPLAY AM" => XTD102->QUM045 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBEFF0FFF READ & COMPARE THE NAD LINES WITH A000008; PULSE XTD102 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 35 MINOR 41 ON NO-GO BRANCH TO MAJOR 35 MINOR 43	EXMW->INMX
35 40			SPARE	
35 41	2	F160.N	FAULT IN EN "DISPLAY AM" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 200 / REPLACE ASSEMBLIES: 1A1A4A(16,19)	
35 42			SPARE	
35 43 35 44	1	T161	TEST RCAQ, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF07FF READ & COMPARE THE NAD LINES WITH A; PULSE XTD103	BREG->ROM, ROM->WD1 DR

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	2	F161.1	FAULT LOC WITHIN TEST 161, NOT A PROGRAMMED STOP- RCAQ LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A15	
	1	T161(CONT)	BRANCH TO MAJOR 35 MINOR 51 ON NO-GO BRANCH TO MAJOR 35 MINOR 46	
35 45			SPARE	
35 46	2	F161.2	FAULT IN RCAQ IBT, LATCH, ETC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
35 47			SPARE	
35 48			SPARE	
35 49			SPARE	
35 50			SPARE	
35 51	1	T162	TEST "DISPLAY AQ" => XTD103->QUM044	
35 52			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBEFFOFFF READ & COMPARE THE NAD LINES WITH A000004; PULSE XTD103 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 35 MINOR 54 ON NO-GO BRANCH TO MAJOR 35 MINOR 56	EXMW->INMX
35 53			SPARE	
35 54	2	F162.N	FAULT IN EN "DISPLAY AQ" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 100 / REPLACE ASSEMBLIES: 1A1A4A(16,19)	
35 55			SPARE	
35 56	1	T163	TEST RCMB, COMPARE => NO-GO	
35 57			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF07FF	BREG->ROM, ROM->WD1 DR

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	2	F163.1	FAULT LOC WITHIN TEST 163, NOT A PROGRAMMED STOP- RCMB LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A15	
	1	T163(CONT)	READ & COMPARE THE NAD LINES WITH A; PULSE XTD104* BRANCH TO MAJOR 35 MINOR 64 ON NO-GO BRANCH TO MAJOR 35 MINOR 59	
35 58			SPARE	
35 59	2	F163.2	FAULT IN RCMB IBT, LATCH, ETC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
35 60			SPARE	
35 61			SPARE	
35 62			SPARE	
35 63			SPARE	
35 64	1	T164	TEST "DISPLAY MB" => XTD104*->QUM047	
35 65			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBEFFOFFF READ & COMPARE THE NAD LINES WITH A; PULSE XTD104* LOGICALLY 'AND' C REGISTER AND A00002 - RESULT IN B & C REGISTER BRANCH TO MAJOR 35 MINOR 67 ON NO-GO BRANCH TO MAJOR 35 MINOR 71	EXMW->INMX
35 66			SPARE	
35 67	2	F164.N	FAULT IN EN "DISPLAY MB" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1000 / REPLACE ASSEMBLIES: 1A1A4A(16,19)	
35 68			SPARE	
35 69			SPARE	
35 70			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
35 71 35 72	1	T165	TEST RCCA, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF READ & COMPARE THE CA LINES WITH A	BREG->ROM, ROM->MB
	2	F165.1	FAULT LOC WITHIN TEST 165, NOT A PROGRAMMED STOP- RCCA LATCH NOT RESET INDICATORS: TEST SET FAULT; DISPLAY: 10000001; REPLACE ASSEMBLIES: 1A1A4A15	
	1	T165(CONT)	BRANCH TO MAJOR 35 MINOR 84 ON NO-GO	
35 73	2	T165.2	TEST FOR READ CA EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 35 MINOR 75 ON NO-GO	
35 74	3	F165.2.G	READ CA FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A4A[15,16]	AAC022* S@1
35 75 35 76	3	T165.2.N	TEST LOAD OF BREG COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 35 MINOR 80 ON NO-GO	
35 77	4	T165.2.NG	TEST R&C GATING READ & COMPARE THE MA LINES WITH A007FFF COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 35 MINOR 78 ON NO-GO	
	5	F165.2.NGG	FAULT RCCA IBT, LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A[15,16]	
35 78	5	F165.2.NGN	FAULT IN R&C GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777760 — REPLACE ASSEMBLIES: 1A1A4A(16,19)	
35 79			SPARE	
35 80	4	F165.2.NN	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-13	
35 81			SPARE	
35 82			SPARE	
35 83			SPARE	
35 84 35 85	1	T166	TEST RCCE, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF READ & COMPARE THE CE LINES WITH A	BREG->ROM, ROM->MB
	2	F166.1	FAULT LOC WITHIN TEST 166, NOT A PROGRAMMED STOP- RCCE LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 1000000 — REPLACE ASSEMBLIES: 1A1A4A15	
	1	T166(CONT)	BRANCH TO MAJOR 35 MINOR 90 ON NO-GO	
35 86	2	T166.2	TEST FOR READ CE EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 35 MINOR 88 ON NO-GO	
35 87	3	F166.2.G	READ CE FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A(15,16)	AAC019* S@1
35 88	3	F166.2.N	FAULT IN RCCE IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
35 89			SPARE	
35 90 35 91	1	T167	TEST RCCI, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF READ & COMPARE THE CI LINES WITH A	BREG->ROM, ROM->MB
	2	F167.1	FAULT LOC WITHIN TEST 167, NOT A PROGRAMMED STOP- RCCI LATCH NOT RESET INDICATORS: TEST SET FAULT — DISPLAY: 10000000 — REPLACE ASSEMBLIES: 1A1A4A15	
	1	T167(CONT)	BRANCH TO MAJOR 35 MINOR 98 ON NO-GO	
35 92	2	T167.2	TEST FOR READ CI EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 35 MINOR 94 ON NO-GO	
35 93	3	F167.2.G	READ CI FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A(15,17)	AAC021* S@1
35 94	3	F167.2.N	FAULT IN RCCI IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
35 95			SPARE	
35 96			SPARE	
35 97			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
35 98			ENABLE VERTICAL PARITY CHECK	
35 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
36 00	2	F30.8	FAULT IN LSB OF MABC	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 2100000000011A1A1A23	
			PUNCH TAPE LEADER 12 INCHES LONG	
			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 36 MINOR 3	
36 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
36 02	2	F30.9	FAULT IN LSB OF MABC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES NO GO | BLANK | 1A1A1A23	
36 03 36 04	1	T168	TEST RCCP, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFE INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF READ & COMPARE THE CP LINES WITH A	BREG->ROM, ROM->MB
	2	F168.1	FAULT LOC WITHIN TEST 168, NOT A PROGRAMMED STOP- RCCP LATCH NOT RESET	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 10000001A1A4A15	
	1	T168(CONT)	BRANCH TO MAJOR 36 MINOR 8 ON NO-GO	
36 05	2	T168.2	TEST FOR READ CP EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 7 ON NO-GO	
36 06	3	F168.2.G	READ CP FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A(15,18,19)	IAE226* Sal
36 07	3	F168.2.N	FAULT IN RCCP IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777760000 — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
36 08 36 09	1	T169	TEST FOR FAULT IN PART OF EN CP COMPARE THE B REGISTER TO AFFFE BRANCH TO MAJOR 36 MINOR 10 ON NO-GO BRANCH TO MAJOR 36 MINOR 13	
36 10	2	F169.N	FAULT IN PART OF EN CP ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXX0000 — REPLACE ASSEMBLIES: 1A1A4A17	
36 11 36 12			SPARE SPARE	
36 13 36 14	1	T170	TEST RCCM, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFF8 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4FBFFF07FF READ & COMPARE THE CM LINES WITH A	BREG->ROM, ROM->CM DR
	2	F170.1	FAULT LOC WITHIN TEST 170, NOT A PROGRAMMED STOP- RCCM LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 1000000 — REPLACE ASSEMBLIES: 1A1A4A15	
	1	T170(CONT)	BRANCH TO MAJOR 36 MINOR 18 ON NO-GO	
36 15	2	T170.2	TEST FOR READ CM EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 17 ON NO-GO	
36 16	3	F170.2.G	READ CM FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A(15,17)	AAC018* S@1
36 17	3	F170.2.N	FAULT IN RCCM IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 17760000000 / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A(15,16)	
36 18 36 19	1	T171	TEST RCEA, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFC LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFFE00 READ & COMPARE THE EA LINES WITH A	
	2	F171.1	FAULT LOC WITHIN TEST 171, NOT A PROGRAMMED STOP- RCEA LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 10000000 / REPLACE ASSEMBLIES: 1A1A4A18	
	1	T171(CONT)	BRANCH TO MAJOR 36 MINOR 30 ON NO-GO	
36 20	2	T171.2	TEST FOR FAULT IN READ EA EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 22 ON NO-GO	
36 21	3	F171.2.G	READ EA FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A(18,20)	AAC026* S@1
36 22 36 23	3	T171.2.N	TEST FOR NO LOAD OF BREG COMPARE THE B REGISTER TO AFFFFC BRANCH TO MAJOR 36 MINOR 26 ON NO-GO	
36 24	4	T171.2.NG	TEST R&C GATING READ & COMPARE THE EB LINES WITH AFFFFFFF BRANCH TO MAJOR 36 MINOR 25 ON NO-GO	
	5	F171.2.NGG	FAULT IN R&C GATING ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A4A(18,19)

36 25	5	F171.2.NGN	FAULT IN RCEA IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXX	1A1A2A18
		1A1A4A18

36 26	4	F171.2.NN	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXXXXXXXXX	PROCEED PER PARAGRAPH 3-13

36 27			SPARE
36 28			SPARE
36 29			SPARE
36 30	1	T172	TEST RCEB, COMPARE => NO-GO
36 31			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF — BREG->ROM, ROM->MB READ & COMPARE THE EB LINES WITH A
	2	F172.1	FAULT LOC WITHIN TEST 172, NOT A PROGRAMMED STOP- RCEB LATCH NOT RESET

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SET FAULT	1000000	1A1A4A18

	1	T172(CONT)	BRANCH TO MAJOR 36 MINOR 38 ON NO-GO
36 32	2	T172.2	TEST FOR FAULT IN READ EB EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 34 ON NO-GO
36 33	3	F172.2.G	READ EB FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A(19,20)	AAC001* S@1
36 34	3	F172.2.N	FAULT IN RCEB IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A18 1A1A4A18	
36 35			SPARE	
36 36			SPARE	
36 37			SPARE	
36 38 36 39	1	T173	TEST RCFM, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF READ & COMPARE THE FMB LINES WITH A	
	2	F173.1	FAULT LOC WITHIN TEST 173, NOT A PROGRAMMED STOP- RCFM LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000001 — REPLACE ASSEMBLIES: 1A1A4A18	
	1	T173(CONT)	BRANCH TO MAJOR 36 MINOR 45 ON NO-GO	
36 40	2	T173.2	TEST FOR FAULT IN READ FMB EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 42 ON NO-GO	
36 41	3	F173.2.G	READ FMB FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A20	AAC036* S@1
36 42	3	F173.2.N	FAULT IN RCFM IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A18	
36 43			SPARE	
36 44			SPARE	
36 45	1	T174	TEST FOR FAULT IN PART OF READ FMB EN	
36 46			COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 36 MINOR 47 ON NO-GO BRANCH TO MAJOR 36 MINOR 51	
36 47	2	F174.N	PART OF READ FMB EN INACTIVE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A4A20	
36 48			SPARE	
36 49			SPARE	
36 50			SPARE	
36 51	1	T175	TEST RCMA, COMPARE => NO-GO	
36 52			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF READ & COMPARE THE MA LINES WITH A	
	2	F175.1	FAULT LOC WITHIN TEST 175, NOT A PROGRAMMED STOP- RCMA LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 1000000 — REPLACE ASSEMBLIES: 1A1A4A15	
	1	T175(CONT)	BRANCH TO MAJOR 36 MINOR 58 ON NO-GO	
36 53	2	T175.2	TEST FOR FAULT IN READ MA EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 55 ON NO-GO	
36 54	3	F175.2.G	READ MA FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A15	AAC017* S01
36 55	3	F175.2.F	FAULT IN RCMA IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1777777777 / REPLACE ASSEMBLIES: 1A1A2A18; 1A1A4A(15,16)	
36 56			SPARE	
36 57			SPARE	
36 58	1	T176	TEST FOR FAULT IN PART OF READ MA EN	
36 59			COMPARE THE B REGISTER TO A007FFF BRANCH TO MAJOR 36 MINOR 60 ON NO-GO BRANCH TO MAJOR 36 MINOR 64	
36 60	2	F176.N	FAULT IN PART OF READ MA ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXX011 / REPLACE ASSEMBLIES: 1A1A4A17	
36 61			SPARE	
36 62			SPARE	
36 63			SPARE	
36 64	1	T177	TEST RCXM, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 1FBFFF07FF READ & COMPARE THE XMB LINES WITH A	BREG->ROM, ROM->XMB DR
36 65		F177.1	FAULT LOC WITHIN TEST 177, NOT A PROGRAMMED STOP- RCXM LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A18	
	1	T177(CONT)	BRANCH TO MAJOR 36 MINOR 72 ON NO-GO	
36 66	2	T177.2	TEST FOR READ XMB EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 68 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
36 67	3	F177.2.G	READ XMB FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A1(16,18)	AAC103* Sa1
36 68	3	F177.2.N	FAULT IN RCXM IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1777777777 / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A18	
36 69				
36 70				
36 71				
36 72 36 73	1	T178	TEST RCW1, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2FBFFF07FF READ & COMPARE WORD 1 WITH A	BREG->ROM, ROM->MB
	2	F178.1	FAULT LOC WITHIN TEST 178, NOT A PROGRAMMED STOP- RCW1 LATCH NOT RESET	
			INDICATORS: TEST SEL FAULT / DISPLAY: 10000001 / REPLACE ASSEMBLIES: 1A1A4A15	
	1	T178(CONT)	BRANCH TO MAJOR 36 MINOR 79 ON NO-GO	
36 74	2	T178.2	TEST FOR READ W1 EN FAULT COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 76 ON NO-GO	
36 75	3	F178.2.G	READ W1 FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A15	AAE035* Sa1
36 76	3	F178.2.N	FAULT IN RCW1 IBT OR LATCH, OR INST DECODE MATRIX ENABLE VERTICAL PARITY CHECK PUNCH TAPE CODES - /E /D &C STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	INVALID INST = OCTAL 336

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT — DISPLAY: 40000000 — REPLACE ASSEMBLIES: 1A1A2A16, 1A1A4A(15,16)	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-120	INST DECODE MATRIX
36 77			SPARE	
36 78			SPARE	
36 79	1	T179	TEST FOR FAULT IN PART OF READ W1	
36 80			COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 36 MINOR 81 ON NO-GO BRANCH TO MAJOR 36 MINOR 86	
36 81	2	F179.N	FAULT IN PART OF READ W1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 7 — REPLACE ASSEMBLIES: 1A1A4A16	
			INDICATORS: NO GO — DISPLAY: 370 — REPLACE ASSEMBLIES: 1A1A4A16	
			INDICATORS: NO GO — DISPLAY: 17400 — REPLACE ASSEMBLIES: 1A1A4A17	
			INDICATORS: NO GO — DISPLAY: 3760000 — REPLACE ASSEMBLIES: 1A1A4A17	
			INDICATORS: NO GO — DISPLAY: 1774000000 — REPLACE ASSEMBLIES: 1A1A4A17	
36 82			SPARE	
36 83			SPARE	
36 84			SPARE	
36 85			SPARE	
36 86	1	T180	TEST RCW2, COMPARE => NO-GO	
36 87			SERIALLY LOAD THE B REGISTER WITH AFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 4FBFFF07FF READ & COMPARE WORD 2 WITH A	BREG->ROM, ROM->CM DR
	2	F180.1	FAULT LOC WITHIN TEST 180, NOT A PROGRAMMED STOP- RCW2 LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 1000000 — REPLACE ASSEMBLIES: 1A1A4A15	
	1	T180(CONT)	BRANCH TO MAJOR 36 MINOR 93 ON NO-GO	
36 88	2	T180.2	TEST FOR FAULT IN READ W1 EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 36 MINOR 90 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
36 89	3	F180.2.G	READ W2 FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A15	AAE036* Sa1
36 90	3	F180.2.N	FAULT IN RCW2 IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXX0 / REPLACE ASSEMBLIES: 1A1A2A14, 1A1A4A(15,16)	
36 91			SPARE	
36 92			SPARE	
36 93	1	T181	TEST FOR FAULT IN PART OF READ W2	
36 94			COMPARE THE B REGISTER TO AFFFFFF BRANCH TO MAJOR 36 MINOR 95 ON NO-GO BRANCH TO MAJOR 36 MINOR 98	
36 95	2	F181.N	FAULT IN PART OF READ W2 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXX0 / REPLACE ASSEMBLIES: 1A1A4A17	
36 96			SPARE	
36 97			SPARE	
36 98			ENABLE VERTICAL PARITY CHECK	
36 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
37 00			FAULT IN 5SB OR BBC738* INPUT TO MBC061	
	2	F192.2		
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT |2100000000001A1A1A(21,22)	
			PUNCH TAPE LEADER 12 INCHES LONG	
			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 37 MINOR 3	
37 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
37 02	1	T31	TEST OF TAPE SEARCH TO ADDR < PRESENT ADDR PREVIOUS TEST = (02)T30 BRANCH TO MAJOR 21 MINOR 2	
37 03 37 04	1	T182	TEST RCW3, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFF READ & COMPARE WORD 3 WITH A	
	2	F182.1	FAULT LOC WITHIN TEST 182, NOT A PROGRAMMED STOP- RCW3 LATCH NOT RESET	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES TEST SET FAULT | 1000000|A1A4A18	
	1	T182(CONT)	BRANCH TO MAJOR 37 MINOR 11 ON NO-GO	
37 05	2	T182.2	TEST FOR FAULT IN READ W3 EN COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 7 ON NO-GO	
37 06	3	F182.2.G	READ W3 FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A4A20	AAE038* Sa1
37 07	3	F182.2.N	FAULT IN RCW3 IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXX000000 — REPLACE ASSEMBLIES: 1A1A2A16, 1A1A4A18	
37 08			SPARE	
37 09			SPARE	
37 10			SPARE	
37 11	1	T183	TEST FOR FAULT IN PART OF READ W3	
37 12			COMPARE THE B REGISTER TO AFF BRANCH TO MAJOR 37 MINOR 13 ON NO-GO BRANCH TO MAJOR 37 MINOR 18	
37 13	2	F183.N	FAULT IN PART OF READ W3 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXX000000 — REPLACE ASSEMBLIES: 1A1A4A19	
37 14			SPARE	
37 15			SPARE	
37 16			SPARE	
37 17			SPARE	
37 18	1	T184	TEST RCEX, COMPARE => NO-GO	
37 19			SERIALLY LOAD THE B REGISTER WITH A0000300 READ & COMPARE THE EXTERNAL MEMORY WORD WITH A	
	2	F184.1	FAULT LOC WITHIN TEST 184, NOT A PROGRAMMED STOP- RCEX LATCH NOT RESET	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A18	
	1	T184(CONT)	BRANCH TO MAJOR 37 MINOR 26 ON NO-GO	
37 20	2	T184.2	TEST FOR FAULT IN READ EXMW COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 22 ON NO-GO	
37 21	3	F184.2.G	READ EXMW FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A20	AAC037* Sa1
37 22	3	F184.2.N	FAULT IN RCEX IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: 1400 / REPLACE ASSEMBLIES: 1A1A2A18, 1A1A4A18	
37 23			SPARE	
37 24			SPARE	
37 25			SPARE	
37 26 37 27	1	T185	TEST RCM1, COMPARE => NO-GO RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) SERIALLY LOAD THE B REGISTER WITH AFFFFFE READ & COMPARE MISCELLANEOUS WORD 1 WITH A	
	2	F185.1	FAULT LOC WITHIN TEST 185, NOT A PROGRAMMED STOP- RCM1 LATCH NOT RESET INDICATORS: TEST SET FAULT / DISPLAY: 1000000 / REPLACE ASSEMBLIES: 1A1A4A18	
	1	T185(CONT)	SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) BRANCH TO MAJOR 37 MINOR 34 ON NO-GO	
37 28	2	T185.2	TEST FOR FAULT IN READ MTW1 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 30 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
37 29	3	F185.2.G	READ MTW1 FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A20	AAC038* S@1
37 30	3	F185.2.N	FAULT IN RCM1 IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: 1777777740 / REPLACE ASSEMBLIES: 1A1A2A16, 1A1A4A18	
37 31			SPARE	
37 32			SPARE	
37 33			SPARE	
37 34 37 35	1	T186	TEST FOR FAULT IN PART OF READ MTW1 COMPARE THE B REGISTER TO AFFFFF2 BRANCH TO MAJOR 37 MINOR 36 ON NO-GO BRANCH TO MAJOR 37 MINOR 41	
37 36	2	F186.N	FAULT IN PART OF READ MTW1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: XXXXXXXXX0 / REPLACE ASSEMBLIES: 1A1A4A20	
37 37			SPARE	
37 38			SPARE	
37 39			SPARE	
37 40			SPARE	
37 41 37 42	1	T187	TEST RCPJ, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFFFF READ & COMPARE PJB LINES WITH A	
	2	F187.1	FAULT LOC WITHIN TEST 187, NOT A PROGRAMMED STOP- RCPJ LATCH NOT RESET	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: TEST SET FAULT — DISPLAY: 10000001 — REPLACE ASSEMBLIES: 2A1A2A09	
	1	T187(CONT)	BRANCH TO MAJOR 37 MINOR 49 ON NO-GO	
37 43	2	T187.2	TEST FOR FAULT IN READ PJB COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 45 ON NO-GO	
37 44	3	F187.2.G	READ PJB FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A09	AAC002* Sa1
37 45	3	F187.2.N	FAULT IN RCPJ IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 17777777777 — REPLACE ASSEMBLIES: 2A1A2A(2,9)	
37 46			SPARE	
37 47			SPARE	
37 48			SPARE	
37 49 37 50	1	T188	TEST RCM2, COMPARE => NO-GO SERIALLY LOAD THE B REGISTER WITH AFFFFE00 READ & COMPARE MISCELLANEOUS WORD 2 WITH A	
	2	F188.1	FAULT LOC WITHIN TEST 188, NOT A PROGRAMMED STOP- RCM2 LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 10000001 — REPLACE ASSEMBLIES: 2A1A2A07	
	1	T188(CONT)	BRANCH TO MAJOR 37 MINOR 57 ON NO-GO	
37 51	2	T188.2	TEST FOR FAULT IN READ MTW2 COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 53 ON NO-GO	
37 52	3	F188.2.G	READ MTW2 FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(7,9)	AAC003* Sa1
37 53	3	F188.2.N	FAULT IN RCM2 IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 17777770000 / REPLACE ASSEMBLIES: 2A1A2A(2,7)	
37 54			SPARE	
37 55			SPARE	
37 56			SPARE	
37 57	1	T189	TEST RCDW, COMPARE => NO-GO	
37 58			SERIALLY LOAD THE B REGISTER WITH A3218 READ & COMPARE DISCRETE WORD WITH A	
	2	F189.1	FAULT LOC WITHIN TEST 189, NOT A PROGRAMMED STOP- RCDW LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / DISPLAY: 10000000 / REPLACE ASSEMBLIES: 2A1A2A07	
			BRANCH TO MAJOR 37 MINOR 65 ON NO-GO	
37 59	2	T189.2	TEST FOR FAULT IN READ DOWD COMPARE THE B REGISTER TO A BRANCH TO MAJOR 37 MINOR 61 ON NO-GO	
37 60	3	F189.2.G	READ DOWD FAULT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(7,9)	AAC004* Sa1
37 61	3	F189.2.N	FAULT IN RCDW IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 310300000 — REPLACE ASSEMBLIES: 2A1A2A(2,7)	
37 62				
37 63				
37 64				
37 65	1	T190	TEST RMBA, MB->AREG PARALLEL, CREG -> WD1* DR -> NAD* REC -> AREG ON RMBA	
37 66			SERIALLY LOAD THE B REGISTER WITH A5555555 COMPARE THE B REGISTER TO F INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F8FFF0BFF LOAD A REGISTER WITH OFFFFFFF READ THE MB LINES INTO THE A REGISTER COMPARE THE B REGISTER TO THE A REGISTER BRANCH TO MAJOR 37 MINOR 69 ON NO-GO BRANCH TO MAJOR 37 MINOR 73	CREG=55555555 CREG->ROM, ROM->WD1 DR CREG=55555555->WD1 DR, MB(NAD)REC->AREG = A5555555
37 67			SPARE	
37 68			SPARE	
37 69	2	T190.N	FAULT IN RMBA OR MB->AREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 252525252 — REPLACE ASSEMBLIES: 2A1A1A04, 2A1A2A06	RMBA IBT OR AREG CLK EN
			INDICATORS: NO GO — DISPLAY: 425252525 — REPLACE ASSEMBLIES: 2A1A1A17	IAD204 Sa0
			INDICATORS: NO GO — DISPLAY: 425240000 — REPLACE ASSEMBLIES: 2A1A1A17	IRA055* Sa1
			INDICATORS: NO GO — DISPLAY: 25252 — REPLACE ASSEMBLIES: 2A1A1A17	IRA056* Sa1
			INDICATORS: NO GO — DISPLAY: 525252525 — REPLACE ASSEMBLIES: 1A1A4A16	INPUT TO GAC009 Sa1
			INDICATORS: NO GO — DISPLAY: 2400000000 — REPLACE ASSEMBLIES: 2A1A1A12	AREG PE
			INDICATORS: NO GO — DISPLAY: 500000000 — REPLACE ASSEMBLIES: 2A1A1A12	AREG PE
			INDICATORS: NO GO — DISPLAY: 240000000 — REPLACE ASSEMBLIES: 2A1A1A12	AREG PE
			INDICATORS: NO GO — DISPLAY: 12000000 — REPLACE ASSEMBLIES: 2A1A1A12	AREG PE
			INDICATORS: NO GO — DISPLAY: 5000000 — REPLACE ASSEMBLIES: 2A1A1A11	AREG PE
			INDICATORS: NO GO — DISPLAY: 2400000 — REPLACE ASSEMBLIES: 2A1A1A11	AREG PE
			INDICATORS: NO GO — DISPLAY: 120000 — REPLACE ASSEMBLIES: 2A1A1A11	AREG PE
			INDICATORS: NO GO — DISPLAY: 5000 — REPLACE ASSEMBLIES: 2A1A1A11	AREG PE
37 70			SPARE	
37 71			SPARE	
37 72			SPARE	
37 73	1	T191	TEST RMBA => XTD104*=0	
37 74			SERIALLY LOAD THE B REGISTER WITH A	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFEF	MTW2->RIM
			LOAD A REGISTER WITH A0000800	
			READ THE MB LINES INTO THE A REGISTER	
			COMPARE THE B REGISTER TO THE A REGISTER	
			LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 37 MINOR 77 ON NO-GO	
			BRANCH TO MAJOR 37 MINOR 98	
37 75			SPARE	
37 76			SPARE	
37 77	2	F191.N	INPUT TO CAC106 S@1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	4000 1A1A4A19	

37 78			SPARE	
37 79			SPARE	
37 80			SPARE	
37 81			SPARE	
37 82			SPARE	
37 83			SPARE	
37 84			SPARE	
37 85			SPARE	
37 86			SPARE	
37 87			SPARE	
37 88			SPARE	
37 89			SPARE	
37 90			SPARE	
37 91			SPARE	
37 92			SPARE	
37 93			SPARE	
37 94			SPARE	
37 95			SPARE	
37 96			SPARE	
37 97			SPARE	
37 98			ENABLE VERTICAL PARITY CHECK	
37 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
38 00	2	F30.10 F192.3	FAULT IN 6SB, 7SB, LSB OF MABC, OR CBC436* S@0	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SET FAULT	210000000001	A1A1A1(21,23)

			PUNCH TAPE LEADER 12 INCHES LONG BRANCH TO MAJOR 38 MINOR 3	
38 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
38 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
38 03	1	T192	TEST 5SB OF MABC & INPUT TO MBC061 BRANCH TO MAJOR 39 MINOR 2	
38 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
39 00	2	F30.11 F242.2 F282.1 F283.1	FAULT IN MABC	
			PUNCH TAPE LEADER 12 INCHES LONG	
			BRANCH TO MAJOR 39 MINOR 3	
39 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
39 02				
39 03			END OF MAJOR TEST	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
TEST SET FAULT	2100000000001	A1A1A1A(2),22,23)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
                ********************************************************************************************************
                *                                                                                                      *
                *                                    COMPUTER FLAGS CONTOL TESTS                                       *
                *                                                                                                      *
                ********************************************************************************************************

40 00                          INITIALIZE
                                 DEFINE SELF TEST TAPE
                                 SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                   (GTC003*)
                                 ENABLE LOW LEVEL ON GTC001*
                                 BRANCH TO MAJOR 40 MINOR 3

40 01                            STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
40 02                            STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

40 03   1      T195            TEST SET I/O COMPLETE, GTC010*=0 -> QUT009
                               PREVIOUS TEST = (38)T192
40 04                            SET THE I/O COMPLETE FLAG (GTC010*)
                                 READ & COMPARE MISCELLANEOUS WORD 1 WITH A
                                 LOGICALLY 'AND' C REGISTER AND A008 - RESULT IN B & C REGISTER
                                 BRANCH TO MAJOR 40 MINOR 5  ON NO-GO
                                 BRANCH TO MAJOR 40 MINOR 6

40 05   2      F195.N          FAULT IN SIOC
                                 ENABLE VERTICAL PARITY CHECK
                                 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	2000000	1A1A4A08
		2A1A2A(2,12,17,18)

```
40 06   1      T196            RESET I/O COMPLETE
40 07                            RESET THE I/O COMPLETE FLAG (GTC010*)
                                 READ & COMPARE MISCELLANEOUS WORD 1 WITH A008
                                 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS
                                 BRANCH TO MAJOR 40 MINOR 8  ON NO-GO
                                 BRANCH TO MAJOR 40 MINOR 12

40 08   2      F196.N          FAULT IN RIOC
                                 ENABLE VERTICAL PARITY CHECK
                                 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	2000000	2A1A2A(12,17)

```
40 09                       SPARE
40 10                       SPARE
40 11                       SPARE

40 12   1       T197        TEST SET SERIAL I/O CONTROL, GTC011*=0 -> QUT010
40 13                         SET THE SERIAL I/O CONTROL FLAG (GTC011*)
                              READ & COMPARE MISCELLANEOUS WORD 1 WITH A
                              LOGICALLY 'AND' C REGISTER AND A004 - RESULT IN B & C REGISTER
                              BRANCH TO MAJOR 40 MINOR 14 ON NO-GO
                              BRANCH TO MAJOR 40 MINOR 15

40 14   2       F197.N      FAULT IN SSIO
                              ENABLE VERTICAL PARITY CHECK
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000	1A1A4A08
		2A1A2A(2,17,20,22)

```
40 15   1       T198        TEST RESET SERIAL I/O CONTROL
40 16                         RESET THE SERIAL I/O CONTROL FLAG (GTC011*)
                              READ & COMPARE MISCELLANEOUS WORD 1 WITH A004
                              LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS
                              BRANCH TO MAJOR 40 MINOR 17 ON NO-GO
                              BRANCH TO MAJOR 40 MINOR 21

40 17   2       F198.N      FAULT IN RSIO
                              ENABLE VERTICAL PARITY CHECK
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000	2A1A2A(12,22)

```
40 18                       SPARE
40 19                       SPARE
40 20                       SPARE

40 21   1       T199        TEST SET SERIAL INPUT DATA, GTC012*=0 -> QUT011
40 22                         SET THE SERIAL INPUT DATA FLAG (GTC012*)
                              READ & COMPARE MISCELLANEOUS WORD 1 WITH A
                              LOGICALLY 'AND' C REGISTER AND A002 - RESULT IN B & C REGISTER
                              BRANCH TO MAJOR 40 MINOR 23 ON NO-GO
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 40 MINOR 24	
40 23	2	F199.N	FAULT IN SSID ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	400000	1A1A4A08
		2A1A2A(2,12,17,20,22)

40 24 40 25	1	T200	TEST RESET SERIAL INPUT DATA RESET THE SERIAL INPUT DATA FLAG (GTC012*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A002 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 40 MINOR 26 ON NO-GO BRANCH TO MAJOR 40 MINOR 30	
40 26	2	F200.N	FAULT IN RSID ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	400000	2A1A2A(12,24)

40 27 40 28 40 29			SPARE SPARE SPARE	
40 30 40 31	1	T201	TEST INHIBIT MEMORY CONTROL, GTC014*=0 -> QUT013 SET THE INHIBIT MEMORY CONTROL FLAG (GTC014*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A0008 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 32 ON NO-GO BRANCH TO MAJOR 40 MINOR 33	
40 32	2	F201.N	FAULT IN SINM ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	100000	1A1A4A07
		1A1A2A(6,11,12,16)

40 33 40 34	1	T202	RESET INHIBIT MEMORY CONTROL RESET THE INHIBIT MEMORY CONTROL FLAG (GTC014*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A0008 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 40 MINOR 35 ON NO-GO BRANCH TO MAJOR 40 MINOR 39	
40 35	2	F202.N	FAULT IN RINM ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
40 36			SPARE	
40 37			SPARE	
40 38			SPARE	
40 39	1	T203	SET INHIBIT PROCEED, GTC002*=0 -> QUT007	
40 40			SET THE INHIBIT PROCEED FLAG (GTC002*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A02 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 41 ON NO-GO BRANCH TO MAJOR 40 MINOR 42	
40 41	2	F203.N	FAULT IN SINP ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
40 42	1	T204	RESET INHIBIT PROCEED	
40 43			RESET THE INHIBIT PROCEED FLAG (GTC002*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A02 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 40 MINOR 44 ON NO-GO BRANCH TO MAJOR 40 MINOR 48	
40 44	2	F204.N	FAULT IN RINP ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	1000000	1A1A2A(11,16)

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000000	1A1A4A09
		1A1A2A(9,10,16)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000000	1A1A2A(10,16)

40 45 SPARE
40 46 SPARE
40 47 SPARE

40 48 1 T205 TEST SET CLEAR-WRITE MEMORY, GTC021*=0 -> QUT016
40 49 SET THE CLEAR WRITE MEMORY FLAG (GTC021*)
READ & COMPARE MISCELLANEOUS WORD 1 WITH A
LOGICALLY 'AND' C REGISTER AND A0001 - RESULT IN B & C REGISTER
BRANCH TO MAJOR 40 MINOR 50 ON NO-GO
BRANCH TO MAJOR 40 MINOR 51

40 50 2 F205.N FAULT IN SCWM
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000	1A1A4A05
		1A1A2A(9,10,11,16)

40 51 1 T206 TEST RESET CLEAR-WRITE MEMORY
40 52 RESET THE CLEAR WRITE MEMORY FLAG (GTC021*)
READ & COMPARE MISCELLANEOUS WORD 1 WITH A0001
LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS
BRANCH TO MAJOR 40 MINOR 53 ON NO-GO
BRANCH TO MAJOR 40 MINOR 57

40 53 2 F206.N FAULT IN RCWM
ENABLE VERTICAL PARITY CHECK
STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	10000	1A1A2A(11,16)

40 54 SPARE
40 55 SPARE
40 56 SPARE

40 57 1 T207 TEST SET INHIBIT INCREMENT CP,GTC003*=0 -> QUT008
40 58 SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
(GTC003*)
READ & COMPARE MISCELLANEOUS WORD 1 WITH A
LOGICALLY 'AND' C REGISTER AND A01 - RESULT IN B & C REGISTER

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 40 MINOR 59 ON NO-GO BRANCH TO MAJOR 40 MINOR 60	
40 59	2	F207.N	FAULT IN SIIC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	4000000	1A1A4A09 1A1A2A(10,11,16)

40 60 40 61	1	T208	TEST RESET INHIBIT INCREMENT CP RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A01 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 40 MINOR 62 ON NO-GO BRANCH TO MAJOR 40 MINOR 66	
40 62	2	F208.N	FAULT IN RIIC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	4000000	1A1A2A(11,16)

40 63 40 64 40 65			SPARE SPARE SPARE	
40 66 40 67	1	T209	TEST SET INITIATE INSTRUCTION CYCLE SET THE INITIATE INSTRUCTION CYCLE FLAG (GTC020*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A0004 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 68 ON NO-GO BRANCH TO MAJOR 40 MINOR 69	
40 68	2	F209.N	FAULT IN SINC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	40000	1A1A4A07
		1A1A2A(11,14,16)

40 69 40 70	1	T210	TEST RESET INITIATE INSTRUCTION CYCLE RESET THE INITIATE INSTRUCTION CYCLE FLAG (GTC020*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A0004 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 40 MINOR 71 ON NO-GO BRANCH TO MAJOR 40 MINOR 75
40 71	2	F210.N	FAULT IN RINC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	4000000	1A1A2A(14,16)

40 72			SPARE
40 73			SPARE
40 74			SPARE
40 75 40 76	1	T211	TEST SET INCREMENT CP, GTC022*=0 -> QUT017 SET THE INCREMENT CP FLAG (GTC022*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 77 ON NO-GO BRANCH TO MAJOR 40 MINOR 78
40 77	2	F211.N	FAULT IN SICP ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	4000	1A1A4A04
		1A1A2A(10,11,17)

40 78 40 79	1	T212	TEST RESET INCREMENT CP RESET THE INCREMENT CP FLAG (GTC022*) READ & COMPARE MISCELLANEOUS WORD 1 WITH A00008 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 40 MINOR 80 ON NO-GO BRANCH TO MAJOR 40 MINOR 84
40 80	2	F212.N	FAULT IN RICP

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 400 — REPLACE ASSEMBLIES: 1A1A2A(11,17)	
40 81			SPARE	
40 82			SPARE	
40 83			SPARE	
40 84	1	T213	TEST GENERATE COMPUTER INTERUPT XTW135*=0 -> QUT019 XTW136*=1 -> QUT020	
40 85			ENABLE COMPUTER RESET (GTC000*) GENERATE COMPUTER INTERRUPT WITH CODE OF 2 SIGNAL ON IS XTW136* READ & COMPARE MISCELLANEOUS WORD 1 WITH A00001 LOGICALLY 'AND' C REGISTER AND A00003 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 86 ON NO-GO BRANCH TO MAJOR 40 MINOR 87	
40 86	2	F213.N	FAULT IN GINT OR XTN135*->QUT019 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1000 — REPLACE ASSEMBLIES: 1A1A2A(4,10,12,13,14)	
			1A1A4A04	
			INDICATORS: NO GO — DISPLAY: 400 — REPLACE ASSEMBLIES: 1A1A2A(4,10)	KTW126
40 87	1	T214	TEST RESET OF INTERUPT REQUESTS	
40 88			SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A00003 LOGICALLY 'AND' C REGISTER AND A00003 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 89 ON NO-GO BRANCH TO MAJOR 40 MINOR 90	
40 89	2	F214.N	FAULT IN RESET OF INTERUPT REQUESTS ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: 1000 / REPLACE ASSEMBLIES: 1A1A2A(4,10,12)	KTW125
40 90	1	T215	TEST GENERATE COMPUTER INTERUPT XTW135*=1 -> QUT019 XTW136*=0 -> QUT020	
40 91			ENABLE COMPUTER RESET (GTC000*) GENERATE COMPUTER INTERRUPT WITH CODE OF 1 SIGNAL ON IS XTW135* READ & COMPARE MISCELLANEOUS WORD 1 WITH A00002 LOGICALLY 'AND' C REGISTER AND A00003 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 92 ON NO-GO BRANCH TO MAJOR 40 MINOR 93	
40 92	2	F215.N	FAULT IN XTW136*->QUT019 OR KTW125 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 1000 / REPLACE ASSEMBLIES: 1A1A2A(4,10)	KTW125
			INDICATORS: NO GO / DISPLAY: 400 / REPLACE ASSEMBLIES: 1A1A2A(4,10,14) 1A1A4A03	
40 93	1	T216	TEST RESET OF KTW126	
40 94			ENABLE CONTROLLED TIMING PULSE INTERVAL 10 ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH A00003 LOGICALLY 'AND' C REGISTER AND A00003 - RESULT IN B & C REGISTER BRANCH TO MAJOR 40 MINOR 95 ON NO-GO BRANCH TO MAJOR 40 MINOR 98	
40 95	2	F216.N	FAULT IN RESET OF KTW126 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 400 / REPLACE ASSEMBLIES: 1A1A2A10	
40 96			SPARE	
40 97			SPARE	
40 98			ENABLE VERTICAL PARITY CHECK	
40 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
41 00			BRANCH TO MAJOR 41 MINOR 3	
41 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
41 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
41 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
42 00			BRANCH TO MAJOR 42 MINOR 3	
42 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
42 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
42 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
43 00			BRANCH TO MAJOR 43 MINOR 3	
43 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
43 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
43 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
44 00			BRANCH TO MAJOR 44 MINOR 3	
44 01	1	T282	TEST INPUT TO MBC061 FOR Sa1 PREVIOUS TEST = (52)T281 BRANCH TO MAJOR 53 MINOR 2	
44 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
44 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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                ********************************************************************************************
                *                                                                                          *
                *                                TESTS OF EIP / EOP CONTROL - MAJORS 45 & 46               *
                *                                          TESTS T220 - T242                               *
                *                                                                                          *
                ********************************************************************************************

45 00                           INITIALIZE
                                  DEFINE SELF TEST TAPE
                                  SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                    (GTC003*)
                                  ENABLE LOW LEVEL ON GTC001*
                                  BRANCH TO MAJOR 45 MINOR 3

45 01   2       F281.1          BBC739* S@1
                                  STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
                                        ____________________________________________________
                                        |_INDICATORS_|_DISPLAY_|_____REPLACE ASSEMBLIES_____|
                                        |NO GO       |  BLANK  |1A1A1A(21,23)               |
                                        |____________|_________|____________________________|

45 02                             STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

45 03   1       T220            TEST EIP 1350 I/O CMPLT -> RESET TST2(SIM NO-GO), BREG -> E8 SERIAL
                                PREVIOUS TEST = (40)T216
45 04                             SERIALLY LOAD THE B REGISTER WITH AAAAAAAA
                                  INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF      SIM NO-GO
                                  LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABA200                    EA =1350
                                  LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABA000                    ACTIVATE I/O REQ
                                  BRANCH TO MAJOR 45 MINOR 5  ON NO-GO

        2       F220.1          FAULT LOC WITHIN TEST T220 - EIP/EOP CONTROL MALFUNCTION
                                        ____________________________________________________
                                        |_INDICATORS_|_DISPLAY_|_____REPLACE ASSEMBLIES_____|
                                        |TEST SET FAULT|400000|2A1A1A05                      | IEC147 S@0
                                        |TEST SET FAULT|200100|2A1A2A(12,13,17,18,20,21)     | AEC047
                                        |TEST SET FAULT|  100 |2A1A1A05                      | IEC272* S@1
                                        |              |      |2A1A2A(13,16,18,20)           |

        1       T220(CONT)        BRANCH TO MAJOR 45 MINOR 24

45 05   2       T220.2          TEST EOP 0370 I/O CMPLT -> RESET TST2(SIM NO-GO)
45 06                             LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E200                    EA = 0370
                                  LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E000                    ACTIVATE I/O REQ
                                  BRANCH TO MAJOR 45 MINOR 7  ON NO-GO
                                  BRANCH TO MAJOR 45 MINOR 11
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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
45 07	3	F220.2.N	FAULT IN EA DECODES OR SYNCHRONIZED I/O REQ ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(13,14,15,16)	CEC099 NOT ACTIVE
45 08			SPARE	
45 09			SPARE	
45 10			SPARE	
45 11			SPARE	
45 12	3	T220.2.G	TEST EOP 0351 I/O CMPLT -> RESET TST2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A400 BRANCH TO MAJOR 45 MINOR 13 ON NO-GO	EA=0351 ACTIVATE I/O REQ
	4	F220.2.GG	FAULT IN EIP 1350 DECODE OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(15,16,17,18)	AEC035* S@1 OR IEC046* S@1
45 13	4	T220.2.GN	TEST EOP 0352 I/O CMPLT -> RESET TST2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3AA00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A800 BRANCH TO MAJOR 45 MINOR 15 ON NO-GO	EA=0352 ACTIVATE I/O REQ
45 14				
	5	F220.2.GNG	FAULT IN AEC047->I/O CMPLT ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(12,16,18)	AEC491* S@1
45 15	5	F220.2.GNN	FAULT IN EA DECODE LOGIC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(14,15,16)	IED051 OR IED037
45 16			SPARE	
45 17			SPARE	
45 18			SPARE	
45 19			SPARE	
45 20			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
45 21			SPARE	
45 22			SPARE	
45 23			SPARE	
45 24	1	T221	TEST DATA TRANSFER OF EIP 1350 IN T220, SERIAL BREG->GTC012*->QUB000->BREG 28 BITS.	
45 25			COMPARE THE B REGISTER TO 05555555	TEST FOR 28 BITS INVERTED, MSHD NOT TRANSFERED
	2	F221.1	FAULT LOC WITHIN TEST T221- DATA SATURATED BREG	
			INDICATORS: TEST SET FAULT / DISPLAY: 2000 / REPLACE ASSEMBLIES: 2A1A1A20, 2A1A2A(17,20,23,24)	NRB121*
	1	T221(CONT)	BRANCH TO MAJOR 45 MINOR 26 ON NO-GO BRANCH TO MAJOR 45 MINOR 37	
45 26	2	T221.2	TEST FOR NO "END 28 BITS"	
45 27			COMPARE THE B REGISTER TO 55555555 BRANCH TO MAJOR 45 MINOR 28 ON NO-GO	
	3	F221.2.G	FAULT IN "END 28 BITS" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A05, 2A1A2A(17,18,20,21,23)	KEC232* S@1
45 28	3	T221.2.N	TEST FOR DATA TO EB S@1	
45 29			COMPARE THE B REGISTER TO OFFFFFFF BRANCH TO MAJOR 45 MINOR 30 ON NO-GO	
	4	F221.2.NG	FAULT IN BREG->GTC012*->QUB000->BREG, DATA S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A20, 2A1A2A(23,24)	QUB000 S@1
45 30	4	T221.2.NN	TEST FOR FAULT IN INHIBIT BREG END AROUND	
45 31			COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 45 MINOR 32 ON NO-GO	
	5	F221.2.NNG	NO INHIBIT OF BREG SHIFT END AROUND => BREG<-BREG+GTC012*	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A20, 2A1A2A16	AEC531* S@1
45 32 45 33	5	T221.2.NNN	TEST FOR NO CHANGE TO BREG DATA COMPARE THE B REGISTER TO AAAAAAAA BRANCH TO MAJOR 45 MINOR 34 ON NO-GO	
	6	F221.2.NNN --->G	FAULT IN SHIFT CLOCKS TO BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A03, 2A1A2A(16,20)	AEC226* S@1
45 34 45 35	6	T221.2.NNN --->N	TEST FOR FAULT IL "EOP MODE SER DATA EN" COMPARE THE B REGISTER TO F5555555 BRANCH TO MAJOR 45 MINOR 36 ON NO-GO	
	7	F221.2.NNN --->NG	KEC232* INPUT TO AEC214* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A20	
45 36	7	F221.2.NNN --->NN	NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXX / REPLACE ASSEMBLIES: 2A1A2A(1,8,13,16,17,21) OR 2A1A2A(12,18,20)	
45 37 45 38	1	T222	TEST EIP 1341 I/O CMPLT -> RESET TST2(SIM NO-GO), AREG(TAPE)->EB SERIAL INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF8FFF4FFF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A88600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A88400 LOAD EIP DATA FIELD 555555 INTO A REGISTER	SIM NO-GO EA=1341 ACTIVATE I/O REQ ONLY 6 DATA CHAR TO TEST

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				CLEAR OF AREG
	2	F222.1	FAULT LOC WITHIN TEST T222- EIP 1341 LATCH NOT RESET	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			TEST SET FAULT | 2001001 2A1A2A18	
			TEST SET FAULT | 1001 2A1A2A18	
	1	T222(CONT)	BRANCH TO MAJOR 45 MINOR 39 ON NO-GO BRANCH TO MAJOR 45 MINOR 46	
45 39 45 40	2	T222.2	TEST EIP 1340 I/O CMPLT -> RESET TST2(SIM NO-GO) LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AB8200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AB8000 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH B8200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH B8000 BRANCH TO MAJOR 45 MINOR 41 ON NO-GO	EA=1340 ACTIVATE I/O REQ EA = 1340 ASSUMING SRT DATA EN ACTIVE ACTIVATE I/O REQ
	3	F222.2.G	FAULT IN EIP 1341 DECODE OR LATCH, OR DEIP IBT OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | 2A1A2A(12,15,16,17,18)	AEC062* Sa1
45 41	3	F222.2.N	FAULT IN EA DECODE LOGIC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			NO GO | BLANK | 2A1A2A(14,15,16)	IED050
45 42 45 43 45 44 45 45			SPARE SPARE SPARE SPARE	
45 46	1	T223	TEST DATA TRANSFER OF EIP 1341 IN T222, SERIAL AREG->GTC012*->QUB000->BREG 28 BITS	
45 47			COMPARE THE B REGISTER TO 0AAAAAAF	TEST FOR 28 BITS FROM AREG INVERTED TO BREG
	2	F123.1	FAULT LOC WITHIN TEST T223- DATA TO BREG SATURATED	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			TEST SET FAULT / 2000 / 2A1A2A(18,23,24)	CEC238* Sa0
	1	T223(CONT)	BRANCH TO MAJOR 45 MINOR 48 ON NO-GO BRANCH TO MAJOR 45 MINOR 61	
45 48 45 49	2	T223.2	TEST FOR DATA -> EB Sa1 COMPARE THE B REGISTER TO OFFFFFFF BRANCH TO MAJOR 45 MINOR 50 ON NO-GO	
	3	F223.2.G	DATA -> EB Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / BLANK / 2A1A1A04	AEC215* OR CEC238* Sa1
			/ / 2A1A2A(20,23,24,)	
45 50 45 51	3	T223.2.N	TEST FOR NO CHANGE TO BREG DATA COMPARE THE B REGISTER TO 05555555 BRANCH TO MAJOR 45 MINOR 52 ON NO-GO	BIT PATTERN IN BREG AFTER T220
	4	F223.2.NG	FAULT IN EN OF BREG CLOCK ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / BLANK / 2A1A2A20	OPEN INPUT TO AEC216
45 52 45 53	4	T223.2.NN	TEST FOR NO CLEAR OF AREG COMPARE THE B REGISTER TO 0AAAAAA4 BRANCH TO MAJOR 45 MINOR 54 ON NO-GO	
	5	F223.2.NNG	FAULT IN "CLEAR A #3" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A17	INPUT TO CEC213 OPEN
45 54	5	F223.2.NNN	FAULT IN "EIP SHORT DATA EN" OR NOT A NORMAL FAULT LOCATION ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXX / REPLACE ASSEMBLIES: 2A1A1A04	
			REPLACE ASSEMBLIES: 2A1A2A(16,20,22,23,24)	
			INDICATORS: NO GO / REPLACE ASSEMBLIES: 12012A1A1A28	OPEN INPUT TO CRA121
45 55			SPARE	
45 56			SPARE	
45 57			SPARE	
45 58			SPARE	
45 59			SPARE	
45 60			SPARE	
45 61	1	T224	TEST EIP 1340 I/O CMPLT -> RESET TST2(SIM NO-GO), AREG -> E8 SERIAL	
45 62			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF	SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AB8200	EA=1340
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AB8000	ACTIVATE I/O REQ
			BRANCH TO MAJOR 45 MINOR 63 ON NO-GO	
	2	F224.1	FAULT LOC WITHIN TEST T224- EIP 1340 LATCH NOT RESET	
			INDICATORS: TEST SET FAULT / REPLACE ASSEMBLIES: 2001001 2A1A2A18	
			INDICATORS: TEST SET FAULT / REPLACE ASSEMBLIES: 10012A1A2A18	
	1	T224(CONT)	BRANCH TO MAJOR 45 MINOR 67	
45 63	2	F224.2	FAULT IN EIP 1340 DECODE OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(15,16,17,18)	AEC034* S01
45 64			SPARE	
45 65			SPARE	
45 66			SPARE	
45 67	1	T225	TEST DATA TRANSFER OF EIP 1340 IN T224, AREG->GTC012*->QU8000->BREG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
45 68			COMPARE THE B REGISTER TO 047FFFFF BRANCH TO MAJOR 45 MINOR 69 ON NO-GO BRANCH TO MAJOR 45 MINOR 73	TEST FOR INVERTED EA 1340 CODE FROM AREG
45 69	2	F225.N	FAULT IN DATA TRANSFER AREG->EB ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1340000000012A1A2A18 — REPLACE ASSEMBLIES	OPEN INPUT TO AEC044
45 70			SPARE	
45 71			SPARE	
45 72			SPARE	
45 73	1	T226	TEST EIP 1360 I/O CMPLT -> RESET TST2(SIM NO-GO), CREG -> EB SERIAL	
45 74			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF	SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABC200	EA=1360
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABC000	ACTIVATE I/O REQ
			BRANCH TO MAJOR 45 MINOR 75 ON NO-GO	
	2	F226.1	FAULT LOC WITHIN TEST T226- EIP 1360 LATCH NOT RESET	
			INDICATORS: TEST SET FAULT — DISPLAY: 200100(2A1A2A18	
			INDICATORS: TEST SET FAULT — DISPLAY: 10012A1A2A18	
	1	T226(CONT)	BRANCH TO MAJOR 45 MINOR 78	
45 75	2	F226.2	FAULT IN EIP 1360 DECODE OR LATCH ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — 2A1A2A(15,16,17,18)	AEC036* Sa1
45 76			SPARE	
45 77			SPARE	
45 78	1	T227	TEST DATA TRANSFER OF EIP 1360 IN T226, CREG->GTC012*->QUB000->BREG, 28 BITS ONLY	
45 79			SERIALLY LOAD THE B REGISTER WITH AAAAAAA0 COMPARE THE B REGISTER TO 0000000A	CREG = AAAAAAAA
			INITIATE SELF TEST MODE 2-RETAIN PREVIOUS BIT PATTERN IN SELF TEST REG.	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABC200	EA=1360
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH ABC000	ACTIVATE I/O REQ
			COMPARE THE B REGISTER TO 05555555	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	2	F227.1	FAULT LOC WITHIN TEST T227- DATA FROM CREG TO BREG SATURATED	
			INDICATORS: TEST SET FAULT — DISPLAY: 200012A1A2A22 — REPLACE ASSEMBLIES	CEC218* S@0
	1	T227(CONT)	BRANCH TO MAJOR 45 MINOR 80 ON NO-GO BRANCH TO MAJOR 45 MINOR 86	
45 80	2	F227.2	FAULT IN TRANSFER OF DATA CREG -> EB ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1252525252 — REPLACE ASSEMBLIES: 2A1A1A03; 2A1A2A(20,22,24)	AEC217* OR CEC218* S@1
45 81			SPARE	
45 82			SPARE	
45 83			SPARE	
45 84			SPARE	
45 85			SPARE	
45 86	1	T228	TEST EOP 0351 I/O CMPLT -> RESET TST2(SIM NO-GO), EB -> BREG SERIAL	
45 87			SET THE SERIAL INPUT DATA FLAG (GTC012*)	SIM EB = 0000000
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF8FFF4FFF	SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A600	EA = 0351
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A400	ACTIVATE I/O REQ
			BRANCH TO MAJOR 45 MINOR 88 ON NO-GO RESET THE SERIAL INPUT DATA FLAG (GTC012*)	
	2	F228.1	FAULT LOC WITHIN TEST T228- EOP 0351 RESET MALFUNCTION	
			INDICATORS: TEST SET FAULT — DISPLAY: 200100 — REPLACE ASSEMBLIES: 12A1A2A(1,8,16,18); 10012A1A2A(1,8,13,16,18,20)	BEC252* S@1
	1	T228(CONT)	BRANCH TO MAJOR 45 MINOR 92	
45 88	2	F228.2	FAULT IN EOP 0351 DECODE OR LATCH ENABLE VERTICAL PARITY CHECK RESET THE SERIAL INPUT DATA FLAG (GTC012*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(15,16,18)	AEC037* Sal
45 89			SPARE	
45 90			SPARE	
45 91			SPARE	
45 92	1	T229	TEST DATA TRANSFER OF EOP 0351 IN T228, SSID=>GTC012*=0->QUB000->BREG, MSHD=A AFTER SHIFT	
45 93			COMPARE THE B REGISTER TO A	
	2	F229.1	FAULT LOC WITHIN TEST T229- DATA EB -> BREG SATURATED	
			INDICATORS: TEST SET FAULT / DISPLAY: 2000 / REPLACE ASSEMBLIES: 2A1A1A(2,3)	AEC028* Sal
	1	T229(CONT)	BRANCH TO MAJOR 45 MINOR 94 ON NO-GO BRANCH TO MAJOR 45 MINOR 98	
45 94	2	F229.2	FAULT IN EB -> BREG DATA TRANSFER ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 2452525252 / REPLACE ASSEMBLIES: 2A1A2A16	INPUT TO AEC521 OPEN
45 95			SPARE	
45 96			SPARE	
45 97			SPARE	
45 98			ENABLE VERTICAL PARITY CHECK	
45 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
46 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 46 MINOR 3	
46 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
46 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
46 03	1	T230	TEST EOP 0356 I/O CMPLT -> RESET TST2, PJB REC -> BREG THEN BREG -> DIHR	
46 04			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A38A00	EA = 0356
			SERIALLY LOAD THE B REGISTER WITH A3B8	LOAD BREG WITH EA 0356 CODE AND I/O REQ FOR TRANS TO DIHR ON NEXT LDSI
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF47FF	BREG->ROM, ROM->WD1*DR, SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH AFA58	DATA->WD1* DR ON "PJB->8"
			BRANCH TO MAJOR 46 MINOR 5 ON NO-GO BRANCH TO MAJOR 46 MINOR 11	
46 05	2	T230.N	TEST EOP 0370 I/O CMPLT -> RESET TST2(SIM NO-GO)	
46 06			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF	SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E200	EA = 0370
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E200	I/O REQ
			BRANCH TO MAJOR 46 MINOR 7 ON NO-GO	
	3	F230.NG	FAULT IN ECP 0356 => SHORT I/O CMPLT LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A(1,12,14,15,16)	IEC069* Sa1
46 07	3	F230.NN	FAULT IN "SHORT I/O CMPLT" LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(1,12,13,16)	AEC089* S@1
46 08			SPARE	
46 09			SPARE	
46 10			SPARE	
46 11 46 12	1	T231	TEST PARALLEL DATA TRANSFER IN T230, TEST FOR DIHR <- AA500 <- AREG=AA580 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOFEF COMPARE THE B REGISTER TO AFA5 LOGICALLY 'AND' C REGISTER AND AFFFF4 - RESULT IN B & C REGISTER BRANCH TO MAJOR 46 MINOR 13 ON NO-GO BRANCH TO MAJOR 46 MINOR 23	MTW2->RIM
46 13 46 14	2	T231.N	TEST FOR NO "EN PJB -> BREG" COMPARE THE B REGISTER TO A3EA74 BRANCH TO MAJOR 46 MINOR 15 ON NO-GO	
	3	F231.NG	FAULT IN "EN PJB -> BREG " LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A03, 2A1A2A(18,20,25)	IEC332* S@1
46 15 46 16	3	T231.NN	TEST FOR NO INHIBIT BREG -> ROM DURING PJB -> BREG COMPARE THE B REGISTER TO AC158 BRANCH TO MAJOR 46 MINOR 17 ON NO-GO	
	4	F231.NNG	FAULT IN INHIBIT OF BREG -> ROM FROM S.T. CONTROL REG LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A07	INPUT TO AYR744* OPEN
46 17 46 18	4	T231.NNN	TEST FOR NO EN PJB -> RIM COMPARE THE B REGISTER TO A05AF4 BRANCH TO MAJOR 46 MINOR 19 ON NO-GO	
	5	F231.NNNG	FAULT IN EN PJB -> RIM	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A09	INPUT TO AAE211 OPEN
46 19	5	F231.NNNN	NOT A NORMAL FAULT LOC - FAULT IN EOP 0356 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: 2A1A2A(12,14,15,16,20,26)	
46 20			SPARE	
46 21			SPARE	
46 22			SPARE	
46 23 46 24	1	T232	TEST EOP0353 I/O CMPLT -> RESET TST2(SIM NO-GO), PJB -> BREG PARALLEL SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8FBFFF4FFF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3AE00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3AC00 BRANCH TO MAJOR 46 MINOR 25 ON NO-GO BRANCH TO MAJOR 46 MINOR 29	ROM->WD1* OR, SIM NO-GO EA = 0353 I/O REQ, DATA -> ROM
46 25	2	F232.N	FAULT IN EOP 0353 DECODE -> SHORT I/O CMPLT LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(14,15,16)	BED253* S@1
46 26			SPARE	
46 27			SPARE	
46 28			SPARE	
46 29 46 30	1	T233	TEST DATA TRANSFER IN T232 COMPARE THE B REGISTER TO AC53FFFF BRANCH TO MAJOR 46 MINOR 31 ON NO-GO BRANCH TO MAJOR 46 MINOR 35	
46 31	2	F233.N	FAULT PJB -> BREG OF EOP 0353 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1424777777 — REPLACE ASSEMBLIES: 2A1A2A(14,15,16,20)	AEC019
46 32			SPARE	
46 33			SPARE	
46 34			SPARE	
46 35	1	T234	TEST EOP 0352 I/C CMPLT -> RESET TST2(SIM NO-GO), JEB -> BREG PARALLEL	
46 36			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 2F8FFF4FFF	ROM->MB DR, SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3AA00	EA=0352
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3A800	I/O REQ
			BRANCH TO MAJOR 46 MINOR 37 ON NO-GO	
			BRANCH TO MAJOR 46 MINOR 41	
46 37	2	F234.N	FAULT IN EOP 0352 DECODE -> SHORT I/O CMPLT	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A2A(1,12,15)	BED252* S@1
46 38			SPARE	
46 39			SPARE	
46 40			SPARE	
46 41	1	T235	TEST DATA TRANSFER IN T234	
46 42			COMPARE THE B REGISTER TO A3A8	
			BRANCH TO MAJOR 46 MINOR 43 ON NO-GO	
			BRANCH TO MAJOR 46 MINOR 51	
46 43	2	T235.N	TEST FOR NO DATA TRANSFER => BREG UNCHANGED	
46 44			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 46 MINOR 45 ON NO-GO	
	3	F235.NG	FAULT IN JEB -> BREG	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A03, 2A1A2A(16,20)	AEC311* Sa1
46 45 46 46	3	T235.NN	TEST FOR NO EN JEB -> INMX COMPARE THE B REGISTER TO A BRANCH TO MAJOR 46 MINOR 47 ON NO-GO	
	4	F235.NNG	FAULT IN EOP 0352 EN JEB -> INMX LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A4A19	INPUT TO CAC101 OPEN
46 47	4	F235.NNN	NOT A NORMAL FAULT-LOCATION - FAULT IN IN EOP 0352 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: 2A1A2A(1,12,14,15,16,20)	
46 48			SPARE	
46 49			SPARE	
46 50			SPARE	
46 51 46 52	1	T236	TEST EOP 0371 I/O CMPLT -> RESET TST2(SIM NO-GO), STOP COMPUTER CLOCK INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E400 BRANCH TO MAJOR 46 MINOR 53 ON NO-GO BRANCH TO MAJOR 46 MINOR 59	SIM NO-GO EA=0371 I/O REQ
46 53 46 54	2	T236.N	TEST EOP 0370 I/O CMPLT -> RESET TST2(SIM NO-GO) LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E000 ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 46 MINOR 55 ON NO-GO	 EA=0370 I/O REQ
	3	F236.NG	FAULT IN EOP 0371 DECODE -> SHORT I/O CMPLT LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A8(1,12)	CED270* S@1
46 55	3	F236.NN	FAULT IN EA DECODE NET LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A8(14,15,16)	IED053 OR IED137 S@0
46 56			SPARE	
46 57			SPARE	
46 58			SPARE	
46 59 46 60	1	T237	TEST FOR RESET OF GTC001* TO 0 IN T236 - READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 46 MINOR 61 ON NO-GO BRANCH TO MAJOR 46 MINOR 65	
46 61			FAULT IN RESET OF KKB022 FF LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 300 / REPLACE ASSEMBLIES: 1A1A3A12, 2A1A2A8(16,20)	AEC317* S@1
46 62			SPARE	
46 63			SPARE	
46 64			SPARE	
46 65 46 66	1	T238	TEST EOP 0362 I/O CMPLT -> RESET TST2(SIM NO-GO), INL TEST CLK STP WITH QUT029(ASG25)=1 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF ENABLE CONTINUOUS HIGH LEVEL ON GTC001* LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3CA40 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3C840 BRANCH TO MAJOR 46 MINOR 67 ON NO-GO BRANCH TO MAJOR 46 MINOR 71	SIM NO-GO EA=0362, QUT029=0 I/O REQ

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
46 67	2	F238.N	FAULT EOP 0362 DECODE -> SHORT I/O CMPLT LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A1(1,12,14)	CED262* SA1
46 68			SPARE	
46 69			SPARE	
46 70			SPARE	
46 71 46 72	1	T239	TEST FOR NO RESET OF GTC001* TO 0 READ & COMPARE MISCELLANEOUS WORD 1 WITH A00000C LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 46 MINOR 73 ON NO-GO BRANCH TO MAJOR 46 MINOR 77	
46 73	2	F239.N	FAULT IN INHIBIT STP CLK WITH QUT029 = 0 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO / DISPLAY: 3001 / REPLACE ASSEMBLIES: 2A1A2A1(8,26)	QUT029
46 74			SPARE	
46 75			SPARE	
46 76			SPARE	
46 77 46 78	1	T240	TEST EOP 0362 RESET OF GTC001* TO 0, QUT029 = 1 ENABLE CONTINUOUS HIGH LEVEL ON GTC001* LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3CA00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3C800 READ & COMPARE MISCELLANEOUS WORD 1 WITH A LOGICALLY 'AND' C REGISTER AND A00000C - RESULT IN B & C REGISTER BRANCH TO MAJOR 46 MINOR 79 ON NO-GO BRANCH TO MAJOR 46 MINOR 83	EA=0362, QUT029 = 1 I/O REQ
46 79	2	T240.N	FAULT IN EOP 0362 -> RESET KKB022 FF ENABLE LOW LEVEL ON GTC001* LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: 300 / REPLACE ASSEMBLIES: 2A1A2A(8,12,26)	AEI030* S@1
46 80			SPARE	
46 81			SPARE	
46 82			SPARE	
46 83	1	T241	TEST EOP 0370 I/O CMPLT -> RESET TST2(SIM NO-GO)	
46 84			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF	SIM NO-GO
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E200	EA=0370
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3E000	I/O REQ
			BRANCH TO MAJOR 46 MINOR 85 ON NO-GO	
			BRANCH TO MAJOR 46 MINOR 98	
46 85	1	F241.N	FAULT IN EOP 0370 DECODE -> SHORT I/O CMPLT	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A(12,15,16)	CED270* S@1
46 86			SPARE	
46 87			SPARE	
46 88			SPARE	
46 89			SPARE	
46 90			SPARE	
46 91			SPARE	
46 92			SPARE	
46 93			SPARE	
46 94			SPARE	
46 95			SPARE	
46 96			SPARE	
46 97			SPARE	
46 98			ENABLE VERTICAL PARITY CHECK	
46 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
*****************************************************************************************************
*                                                                                                   *
*                    THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99                  *
*                                                                                                   *
*****************************************************************************************************

47 00                       BRANCH TO MAJOR 47 MINOR 3
47 01                       STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
47 02                       STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
47 03                       END OF MAJOR TEST
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
48 00	2	F242.2	BBC133* S@0	
			| INDICATORS | DISPLAY | REPLACE ASSEMBLIES |	
			|TEST SET FAULT |2100000000011A1A1A(21,23)|	
			PUNCH TAPE LEADER 12 INCHES LONG	
			BRANCH TO MAJOR 48 MINOR 3	
48 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
48 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
48 03	1	T242	TEST 2SB OF MABC	
			BRANCH TO MAJOR 49 MINOR 2	
48 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
49 00			BRANCH TO MAJOR 49 MINOR 3	
49 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
49 02				
49 03			END OF MAJOR TEST	

```
|TEST|DECISION | TEST/FAULT |                          SELF-TEST PROGRAM                          |          REMARKS          |
| NO.|  LEVEL  |   NUMBER   |                                                                     |                           |

            ********************************************************************************************************
            *                                                                                                      *
            *                                TESTS OF MEMORY CONTROL - MAJORS 50 & 51                              *
            *                                          TEST T245 - T280                                            *
            *                                                                                                      *
            ********************************************************************************************************

50 00                       INITIALIZE
                              DEFINE SELF TEST TAPE
                              SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                (GTC003*)
                              ENABLE LOW LEVEL ON GTC001*
                              BRANCH TO MAJOR 50 MINOR 3

50 01                         STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
50 02                         STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

50 03   1       T245        TEST MFIL => RESET TST2(SIM NO-GO) ON CMA121
                            PREVIOUS TEST = (48)T242
50 04                         INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFDFOFOFFF      MTW1 REC->INMX ON CMA121,
                                                                                                      SIM CM7
                              ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA:
                                0
                              PUNCH TAPE LEADER 12 INCHES LONG
                              BRANCH TO MAJOR 50 MINOR 5  ON NO-GO
                              INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FFF      SIM NO-GO
                              RESET MEMORY FILL MODE
                              SERIALLY LOAD THE B REGISTER FROM THE A REGISTER
                              PUNCH TAPE LEADER 12 INCHES LONG
                              BRANCH TO MAJOR 50 MINOR 6  ON NO-GO
                              BRANCH TO MAJOR 50 MINOR 8

50 05   2       F245.1      FAULT IN MFIL IBT => CMA121
                              RESET MEMORY FILL MODE
                              PUNCH TAPE LEADER 12 INCHES LONG
                              ENABLE VERTICAL PARITY CHECK
                              SET THE I/O COMPLETE FLAG (GTC010*)                                    RESET TST2
                              RESET THE I/O COMPLETE FLAG (GTC010*)
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A15, 1A1A3A(1,7,26)	KMA111* Sa1
50 06	2	F245.2	FAULT IN INH OF HMFL SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A1A(10,18), 1A1A3A01	KMA118* Sa1
50 07			SPARE	
50 08	1	T246	TEST FOR MFIL FF RESET	
50 09			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF8FOF4FFF	RESET TST2 ON CMA121, SIM NO-GO
			BRANCH TO MAJOR 50 MINOR 13 ON NO-GO PUNCH TAPE LEADER 12 INCHES LONG	NO-GO = PASS
50 10	2	F246.G	MFIL NOT RESET ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON COMPARE THE B REGISTER TO 0	SET UP AREG SAT FAULT TO STOP TAPE
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A15	AAD101* Sa1
			INDICATORS: TEST SET FAULT / DISPLAY: 4000 / REPLACE ASSEMBLIES: 1A1A3A01	KMA111* Sa0
50 11			SPARE	
50 12			SPARE	
50 13	1	T247	TEST FOR SIGNALS PRESET DURING MFIL CMA121, CFLG* OR -> MTW1 REC ON CMA121 IN T246 SIGNAL ROUTING: GTC002* -> QUT007 GTC021* -> QUT016 GTC022* -> QUT017 GTW001* -> QUT018	
50 14			COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0201C - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 15 ON NO-GO BRANCH TO MAJOR 50 MINOR 18	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
50 15	2	F247.N	FAULT IN SIGNALS PRESENT DURING MFIL CMA121 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	10000000	1A1A2A09 1A1A3A02	AMA115* Sa1
NO GO	10000	1A1A2A10 (1A1A3A(1,3) OR 1A1A3A(4,5)	IMA155* Sa1
NO GO	4000	1A1A2A(10,20) 1A1A3A(1,3)	BMA174* Sa1
NO GO	2000	1A1A3A02 1A1A4A04	GTW001* Sa1

50 16			SPARE	
50 17			SPARE	
50 18	1	T248	TEST FOR NO RESET OF KMA081 OR KMV011 FFS	
50 19			ENABLE CONTINUOUS HIGH LEVEL ON GTC001* READ & COMPARE MISCELLANEOUS WORD 1 WITH AFEFFFC LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 50 MINOR 20 ON NO-GO BRANCH TO MAJOR 50 MINOR 23	
50 20	2	F248.N	FAULT IN RESET OF KMA081 OR KMV011 FFS ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	2400001	1A1A3A(6,7,14,16,23)	AKB111* Sa1
NO GO	200300	1A1A3A(1,2)	AMA028* Sa1
NO GO	200000	1A1A3A09	KMA091 Sa1
NO GO	40300	1A1A3A06	KMV011 Sa1
NO GO	300	1A1A3A01	KMA081 Sa1

50 21			SPARE	
50 22			SPARE	
50 23	1	T249	TEST INHIBIT OF SHORT DATA TO AREG DURING MFIL	
50 24			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF COMPARE THE B REGISTER TO THE A REGISTER RESET MEMORY FILL MODE BRANCH TO MAJOR 50 MINOR 25 ON NO-GO BRANCH TO MAJOR 50 MINOR 28	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
50 25	2	F249.N	FAULT IN IMA124* ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 2400000000001 — REPLACE ASSEMBLIES: 1A1A3A(1,2,8)	
50 26			SPARE	
50 27			SPARE	
50 28	1	T250	TEST FOR "CLEAR MB" PULSE DURING MFIL, GT8000* -> QUT006 ON BMA165	
50 29			*SERIALLY LOAD THE B REGISTER WITH AFFFFFFF* INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F1FOFFF	MTW1 REC -> INMX ON BMAI65
			ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A04 - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 30 ON NO-GO BRANCH TO MAJOR 50 MINOR 37	
50 30	2	T250.N	TEST CFLG* DR -> MTW1 REC ON KMA091	
			SIGNAL ROUTING: GTC013* -> QUT012 GTC020* -> QUT014	
50 31			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF *INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FOBOFFF*	*MTW1 REC -> INMX ON KMA091*
			PUNCH TAPE CODES - /0 /4 #0 &C #0 &C #0 &C #0 &C	MFIL (ADDR=0 DATA=0,0,0)
			RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0014 - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 32 ON NO-GO	
	2	F250.NG	FAULT IN "CLEAR MB" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A2A10 1A1A3A(2,3,19,20)	BMA165* S@1
50 32	3	T250.NN	*TEST LOAD CM8 ON KMA061*	
50 33			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF3F2F4FFF	RESET SIM NO-GO ON KMA061
			ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE BRANCH TO MAJOR 50 MINOR 34 ON NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	4	F250.NNG	FAULT IN NYK012* -> RESET TST2 OR KMA071 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(1,20) 2A1A3A15	
50 34	4	F250.NNN	FAULT IN INITIALIZE SEQUENCE ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(1,2)	KMA061
50 35			SPARE	
50 36			SPARE	
50 37	1	T251	TEST CFLG* DR -> MTW1 REC ON KMA091 SIGNAL ROUTING: GTC013* -> QUT012 GTC020* -> QUT014	
50 38			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F080FFF PUNCH TAPE CODES - /0 /4 #0 &C #0 &C #0 &C #0 &C RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A00000C LOGICALLY 'AND' C REGISTER AND A00140C - RESULT IN B & C REGISTER	MTW1 REC -> INMX ON KMA091 MFIL (ADDR=0 DATA=0,0,0)
	2	F251.1	FAULT LOC WITHIN TEST T251 - BREG SATURATED DURING VERIFY COMPARE	
			INDICATORS: TEST SET FAULT — DISPLAY: 2000 — REPLACE ASSEMBLIES: 1A1A3A(14,23)	
	1	T251(CONT)	ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 50 MINOR 39 ON NO-GO BRANCH TO MAJOR 50 MINOR 44	
50 39	2	T251.2	REPEAT TEST T251 EXCEPT ON KMV011 SIGNAL ROUTING: GTC013* -> QUT012 GTC020* -> QUT014	
50 40			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F070FFF PUNCH TAPE CODES - /0 /4 #0 &C #0 &C #0 &C #0 &C RESET MEMORY FILL MODE	MTW1 REC -> INMX ON KMV011 MFIL (ADDR=0 DATA=0,0,0)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A00000C LOGICALLY 'AND' C REGISTER AND A00140C - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 41 ON NO-GO ENABLE LOW LEVEL ON GTC001*	
	3	F251.2.G	KMA091 OR KYR021* Sa0 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A(9,20,23)	
50 41	3	F251.2.N	FAULT IN LOAD MB CONTROL ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) ENABLE LOW LEVEL ON GTC001* STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO — DISPLAY: 240300 — REPLACE ASSEMBLIES: 1A1A3A(1,2,3,6)	MMA036* Sa1 OR KMV011 Sa0
			INDICATORS: NO GO — DISPLAY: 200000 — REPLACE ASSEMBLIES: 1A1A3A(2,9)	GTC013* Sa1
			INDICATORS: NO GO — DISPLAY: 40000 — REPLACE ASSEMBLIES: 1A1A2A11, 1A1A3A06	KMV011* Sa1
			INDICATORS: NO GO — DISPLAY: 300 — REPLACE ASSEMBLIES: 1A1A3A(3,7)	IMA055* Sa1
50 42			SPARE	
50 43			SPARE	
50 44	1	T252	TEST REPETATIVE LOAD MB WITH DATA, AREG->MBDR->JEBREC->INMX->BREG ON KMA091	
50 45			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0B3F0B0FFF PUNCH TAPE CODES - /0 /4 #0 &C #0 &C #0 &C #0 &C #F #F #F #F #F #F #F #A &C RESET MEMORY FILL MODE COMPARE THE B REGISTER TO AFFFFFFF BRANCH TO MAJOR 50 MINOR 46 ON NO-GO BRANCH TO MAJOR 5U MINOR 49	JEB->INMX ON KMA091 MFIL (ADDR=0 DATA=0,0,0,AFFFFFFF)
50 46	2	F252.N	AMA053* Sa1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A2A04, 1A1A3A(1,2,9,20)	
50 47			SPARE	
50 48			SPARE	
50 49	1	T253	TEST CLEAR CM & CP, CFLG* DR -> MTW1 REC ON KMA051	
			SIGNAL ROUTING: GTM010* -> QUT005 GTP000* -> QUT004	
50 50			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F4F0FFF ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A18 - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 51 ON NO-GO BRANCH TO MAJOR 50 MINOR 54	MTW1->INMX ON KMA051
50 51	2	F253.N	FAULT IN CLEAR CM & CP ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO — DISPLAY: 100000000 — REPLACE ASSEMBLIES: 1A1A2A19	CTM110 S@0
			INDICATORS: NO GO — DISPLAY: 140000000 — REPLACE ASSEMBLIES: 1A1A3A20 OR 1A1A3A01	KMA051* S@1
			INDICATORS: NO GO — DISPLAY: 40000000 — REPLACE ASSEMBLIES: 1A1A2A19	CTP100 S@0
50 52			SPARE	
50 53			SPARE	
50 54	1	T254	TEST LOAD CM8 ON KMA061, CM* DR -> JCM* REC	
50 55			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF2F2F0FFF ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A808 BRANCH TO MAJOR 50 MINOR 56 ON NO-GO BRANCH TO MAJOR 50 MINOR 59	JCM*->INMX ON KMA061

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
50 56	2	F254.N	FAULT IN LOAD CM8 DURING MFIL ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1000000000 — REPLACE ASSEMBLIES: 1A1A2A07	ATM404 S@0
			INDICATORS: NO GO — DISPLAY: 1002000000 — REPLACE ASSEMBLIES: 1A1A3A20 OR 1A1A3A01	KMA061* S@1
			INDICATORS: NO GO — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 1A1A2A07	ATM403 S@0
50 57			SPARE	
50 58			SPARE	
50 59	2	T255	TEST LOAD CP, AREG -> CP* DR -> NAD* REC -> BREG ON KMA061	
50 60			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 073F2F0FFF ENABLE LO SPEED MEMORY MODE WITH ADDRESS: AFFFE DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO AFFFE BRANCH TO MAJOR 50 MINOR 61 ON NO-GO BRANCH TO MAJOR 50 MINOR 64	NAD*->INMX ON KMA061
50 61	2	F255.N	FAULT IN MFIL => EN CP* DR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A2A04	CPT203 INACTIVE
50 62			SPARE	
50 63			SPARE	
50 64	1	T256	TEST CFLG* DR -> MTW1 ON KMV011	
			SIGNAL ROUTING: GTC020* -> QUT014 GTI000* -> QUT003 GTE000* -> QUT002 GTA000* -> QUT001	
50 65			SERIALLY LOAD THE B REGISTER WITH AFFFFFFF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1F070FFF ENABLE LO SPEED MEMORY MODE WITH ADDRESS: 0 DATA: 0 RESET MEMORY FILL MODE COMPARE THE B REGISTER TO A	MTW1->INMX ON KMV011

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOGICALLY 'AND' C REGISTER AND AE004 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 50 MINOR 66 ON NO-GO	
			BRANCH TO MAJOR 50 MINOR 69	
50 66	2	F256.N	FAULT IN SIGNALS DURING KMV011	
			ENABLE VERTICAL PARITY CHECK	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / 1600040000011A1A3A20	KMV011
			NO GO / 1600000000011A1A2A06	INPUT TO OTW150 OPEN
50 67			SPARE	
50 68			SPARE	
50 69	1	T257	TEST LOAD MB DURING HMFL AND SPEED CHANGE	
50 70			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0B3F0B0FFF	JE8->INMX ON KMA091
			PUNCH TAPE CODES - /8 /4	
			PUNCH TAPE LEADER 12 INCHES LONG	
			PUNCH TAPE CODES - #0 &C #0 &C #0 &C #0 &C #F #F #F #F #F #F #F #A &C	HMFL (ADDR=0 DATA=0,0,0,AFFFFFFF)
			COMPARE THE B REGISTER TO AFFFFFFF	
			BRANCH TO MAJOR 50 MINOR 71 ON NO-GO	
			BRANCH TO MAJOR 50 MINOR 74	
50 71	2	F257.N	FAULT IN HMFL	
			ENABLE VERTICAL PARITY CHECK	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			RESET MEMORY FILL MODE	
			PUNCH TAPE LEADER 12 INCHES LONG	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / XXXXXXXXXXX / 1A1A2A15	AAD101* S@1
			/ / 1A1A3A26	
50 72			SPARE	
50 73			SPARE	
50 74	1	T258	TEST SPEED CHANGE DURING HMFL	
			RESET MEMORY FILL MODE	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
	2	F258.1	FAULT LOC WITHIN TEST T257 - NO CHANGE OF SPEED IN HMFL	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A1A(10,16,18) OR 1A1A3A(1,8,14) OR 1A1A1A11	
	1	T258(CONT)	PUNCH TAPE LEADER 12 INCHES LONG BRANCH TO MAJOR 50 MINOR 76	
50 75			SPARE	
50 76	1	T259	TEST DECODE OF CM1, AREG=CM1->CM*DR->JCM*REC->CM1 DECODE->GREG->DSPL->INMX->RIM ->BREG	
50 77			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F87DF0FFF PULSE THE CM DRIVERS WITH 03 COMPARE THE B REGISTER TO A4 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 50 MINOR 78 ON NO-GO BRANCH TO MAJOR 50 MINOR 84	GREG->DSPL, DSPL->INMX, INMX->BREG ON KTL501 DATA = CM1
50 78	2	T259.N	TEST DECODE OF CP1023	
50 79			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F87DF0FFF PULSE THE MB DRIVERS WITH 07FE COMPARE THE B REGISTER TO A8 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 50 MINOR 80 ON NO-GO	GREG->DSPL, DSPL->INMX, INMX->BREG ON KTL501 DATA = CP1023 CODE
	3	F259.NG	FAULT IN CM1 DECODE -> GREG STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A3A18	IKD041
50 80	3	F259.NN	FAULT IN EN GREG -> DSPL STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1000000000 — REPLACE ASSEMBLIES: 1A1A3A(21,26)	GVM137 S30
50 81			SPARE	
50 82			SPARE	
50 83			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
50 84 50 85	1	T260	TEST DECODE OF CM7, AREG=CM7->CM*DR->JCM*REC->GREG->DSPL->INMX->BREG SERIALLY LOAD THE B REGISTER WITH AF INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFB7DFOFFF PULSE THE CM DRIVERS WITH C COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A2 - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 86 ON NO-GO BRANCH TO MAJOR 50 MINOR 89	GREG->DSPL, DSPL->INMX, INMX->BREG ON KTL501 DATA = CM7 CODE
50 86	2	F260.N	FAULT IN CM7 DECCDE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	200000000	1A1A3A18 1A1A4A(12,20)	AMD031* Sa1

50 87		SPARE	
50 88		SPARE	
50 89 50 90	1	T261	TEST DECODE OF CP1023 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFB7DFOFFF PULSE THE MB DRIVERS WITH 07FE COMPARE THE B REGISTER TO A8 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 50 MINOR 91 ON NO-GO BRANCH TO MAJOR 50 MINOR 93	GREG->DSPL, DSPL->INMX, INMX->BREG ON KTL501 DATA = CP1023 CODE
50 91	2	F261.N	FAULT IN DECODE OF CP1023 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES	
NO GO	1000000000	1A1A3A18 1A1A4A(16,20)	IMD042 Sa0

50 92		SPARE	
50 93 50 94	1	T262	TEST FOR CM1 CM7 & CP1023 DECODES INACTIVE INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFB7DFOFFF COMPARE THE B REGISTER TO A2 LOGICALLY 'AND' C REGISTER AND AE - RESULT IN B & C REGISTER BRANCH TO MAJOR 50 MINOR 95 ON NO-GO BRANCH TO MAJOR 50 MINOR 98	GREG->DSPL, DSPL->INMX
50 95	2	F262	CM1 CM7 OR CP1023 DECODE ACTIVE STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO DISPLAY: 1000000000 REPLACE ASSEMBLIES: 1A1A3A18, 1A1A4A20	IMD042 Sa1
			INDICATORS: NO GO DISPLAY: 400000000 REPLACE ASSEMBLIES: 1A1A3A18, 1A1A4A(12,20)	IKD041 Sa1
			INDICATORS: NO GO DISPLAY: 200000000 REPLACE ASSEMBLIES: 1A1A3A18, 1A1A4A(12,20)	AMD031 Sa0
50 96			SPARE	
50 97			SPARE	
50 98			ENABLE VERTICAL PARITY CHECK	
50 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
51 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 51 MINOR 3	
51 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
51 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
51 03 51 04	1	T263	TEST FOR LVWC SELF TEST CYCLE HANGUP, EN MB -> STE INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F0F0FFF ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 0	INH ALL MEM LD, MEM EN MB->STE
	2	F263.1	LVWC SELF TEST CYCLE HANGUP INDICATORS: NONE; DISPLAY: XXXXXXXXXXX; REPLACE ASSEMBLIES: PROCEED PER PARAGRAPH 3-6D	
	1	T263(CONT)	BRANCH TO MAJOR 51 MINOR 7	
51 05			SPARE	
51 06			SPARE	
51 07 51 08	1	T264	TEST FOR RESET OF ALL MEMORY EN LD BREG SIGNALS SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F9FF10FFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 51 MINOR 9 ON NO-GO BRANCH TO MAJOR 51 MINOR 12	MTW1->INMX ON ANY MEMORY LD BREG SIGNAL
51 09	2	F264.N	FAULT IN RESET OF MEM LD BREG SIGNALS ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO; DISPLAY: XXXXXXXXXXX; REPLACE ASSEMBLIES: 1A1A3A(1,4,23)	RESET TST2 IMV061 OR KMA152
51 10			SPARE	
51 11			SPARE	
51 12	1	T265	TEST FOR RESET OF TST2(SIM NO-GO) ON CMA121 DURING LVWC, CFLG*->MTW1	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
51 13			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF9FOF4FFF	MTW1->INMX, RESET SIM NO-GO ON CMA121
			ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 0	
	2	F265.1	FAULT LOC WITHIN T265 - LVWC SELF TEST CYCLE, WITH NO TST2 CONTROL, HANGUP	
			INDICATORS: NONE / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A3A(4,16,23,24)	AMV174* Sa1
	1	T265(CONT)	BRANCH TO MAJOR 51 MINOR 14 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 18	
51 14	2	F265.N	FAULT IN LVWC IBT OR FF	
			ENABLE VERTICAL PARITY CHECK	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A15, 1A1A3A(1,7,8)	KMA114* Sa1
51 15			SPARE	
51 16			SPARE	
51 17			SPARE	
51 18	1	T266	TEST FOR RESET OF "MEMORY VERIFY MODE"	
51 19			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A0001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 51 MINOR 20 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 23	
51 20	2	F266.N	NO RESET OF MEMORY VERIFY MODE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 10000 / REPLACE ASSEMBLIES: 1A1A3A(1,4)	CMB074 Sa1
51 21			SPARE	
51 22			SPARE	
51 23	1	T267	TEST "WORST CASE LOAD STROBE" => GTB000* -> QUT006 ON CMV053*	
51 24			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1F1FOFFF	MTW1->INMX ON CMV053*
			ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 0	
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A0401 - RESULT IN B & C REGISTER	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			BRANCH TO MAJOR 51 MINOR 25 ON NO-GO BRANCH TO MAJOR 51 MINOR 29	
51 25	2	F267.N	FAULT IN CMV053* => LD BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 20000000 — REPLACE ASSEMBLIES: 1A1A3A19	CMV053*
51 26			SPARE	
51 27			SPARE	
51 28			SPARE	
51 29	1	T268	TEST SHIFT OF AREG ONCE DURING LOAD PORTION OF LVWC S.T. CYCLE	
51 30			SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 083F0B0FFF ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: AFFFFFFF COMPARE THE B REGISTER TO D7FFFFFF BRANCH TO MAJOR 51 MINOR 31 ON NO-GO BRANCH TO MAJOR 51 MINOR 34	JEB->INMX ON KMA091
51 31	2	F268.N	FAULT IN SHIFT AREG DURING LOAD PORTION OF LVWC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 740000000 — REPLACE ASSEMBLIES: 1A1A3A(4,5,12), 2A1A1A04	INPUT TO AMC022 OR IMB135*
			INDICATORS: NO GO — DISPLAY: 700000000 — REPLACE ASSEMBLIES: 1A1A3A05, 2A1A2A19	IMB135* S@1
51 32			SPARE	
51 33			SPARE	
51 34	1	T269	TEST GTC020* -> OUT014 ON KMV011 DURING LVWC, TEST FOR 2 SHIFTS OF AREG	
51 35			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F1F070FFF ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 80000002 COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0004 - RESULT IN B & C REGISTER BRANCH TO MAJOR 51 MINOR 36 ON NO-GO BRANCH TO MAJOR 51 MINOR 40	MTW1->INMX ON KMV011
51 36	2	F269.N	FAULT IN VERIFY PORTION OF LVWC, SHIFT OF AREG ENABLE VERTICAL PARITY CHECK	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 4000000000 — REPLACE ASSEMBLIES: 1A1A3A(3,8)	BMA162* Sa1
			INDICATORS: NO GO — DISPLAY: 1340000000000 — REPLACE ASSEMBLIES: 1A1A3A(1,3)	KMA152
51 37			SPARE	
51 38			SPARE	
51 39			SPARE	
51 40	1	T270	TEST COMPLETE LVWC S.T. CYCLE, CREG->ROM->WD1*DR->NAD*REC->BREG 3 TIMES, 3COMPARES- 2NO-GO THEN GO	
51 41			SERIALLY LOAD THE B REGISTER WITH A5555555	
			COMPARE THE B REGISTER TO A	CREG = 0AAAAAAA
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F0F08FF	CREG->ROM, ROM->WD1*DR/MB->STE, INH ALL MEM LD BREG
			ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 2AAAAAA8	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			BRANCH TO MAJOR 51 MINOR 43 ON NO-GO	
51 42	2	F270.N	FAULT IN ENABLE OF VERIFY FUNCTION	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 1A1A3A(14,21)	CAR019 OR AYR200
51 43	1	T271	TEST COMPLETE LVWC S.T. CYCLE, CLEAR NO-GO FROM T269, AREG->ROM->WD1*DR->NAD*REC->BREG 3 TIMES GO	
51 44			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F0F0FFF	EN MEM MB->STE, INH ALL MEM LD BREG
			ENABLE WORST CASE MEMORY MODE-ADDRESS: 00000 PATTERN: AAAAAAAA	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			BRANCH TO MAJOR 51 MINOR 45 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 49	
51 45	2	F271.N	FAULT IN RESET OF NO-GO, OR VERIFY MALFUNCTION	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: 1A1A3A(8,17,23), 1A1A4A16, 2A1A1A02	
51 46			SPARE	
51 47			SPARE	
51 48			SPARE	
51 49	1	T272	TEST EN MB->NAD PULSE, XTD104*->QUT021 (MTW2) ON IMV061	
51 50			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 8F3F0D0FEF	EN MEM MB->STE, MTW2->RIM ON IMV061
			ENABLE WORST CASE MEMORY MODE-ADDRESS: 0 PATTERN: 00000001	CHECK QUT021 DURING VERIFY
			LOGICALLY 'AND' C REGISTER AND A00008 - RESULT IN B & C REGISTER	MASK FOR QUT021
			BRANCH TO MAJOR 51 MINOR 51 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 54	
51 51	2	F272.N	FAULT IN AMV161* => XTD104*	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 4000 / REPLACE ASSEMBLIES: 1A1A3A20, 1A1A4A19	
51 52			SPARE	
51 53			SPARE	
51 54	1	T273	TEST SMFA => GTC021* = 0	
51 55			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F9F0F0FFF	MTW1->INMX ON CMA121
			ENABLE SINGLE MEMORY MODE WITH ADDRESS: 0 DATA: 0	
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A0001 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 51 MINOR 56 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 60	
51 56	2	F273.N	INPUT TO CMA145 OPEN	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: 10000[1A1A3A03 — REPLACE ASSEMBLIES	
51 57			SPARE	
51 58			SPARE	
51 59			SPARE	
51 60	1	T274	TEST FOR NO SET OF SINGLE LOAD MEMORY FF WITH CM7 PRESENT & SLMC	
51 61			SERIALLY LOAD THE B REGISTER WITH A62FFFFF	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFDFOFOFFF	SIM CM7, 0->BREG ON CMA121
			PULSE THE CP DRIVERS WITH 0; MB DRIVERS WITH THE C REGISTER	
			COMPARE THE B REGISTER TO A62FFFFF	
			BRANCH TO MAJOR 51 MINOR 62 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 65	
51 62	2	F274.N	NO INH OF SLMC LATCH WITH CM7	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 17777777771[1A1A3A(1,2,8) — REPLACE ASSEMBLIES	AMA129* S@1
51 63			SPARE	
51 64			SPARE	
51 65	1	T275	TEST SET OF "SINGLE LOAD MEM FROM CREG" LATCH, CHECK AFFECT ON DATA IN AREG WITH COMPARE	
51 66			SERIALLY LOAD THE B REGISTER WITH A	
			COMPARE THE B REGISTER TO AAAAAAAA	CREG = 0AAAAAAA
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 083F070FFF	JEB->INMX ON KMA011
			PULSE THE CP DRIVERS WITH THE A REGISTER & MB DRIVERS WITH THE C REG.	
			PUNCH TAPE CODES - &C	
			COMPARE THE B REGISTER TO A0AAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF7FOFOFFF	CM7 TO RESET SLMC LATCH, ALL MEM LD BREG INACTIVE
			LOGICALLY 'AND' C REGISTER AND FFFFFFFF - RESULT IN B & C REGISTER	
			COMPARE THE B REGISTER TO A0A	
			BRANCH TO MAJOR 51 MINOR 67 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 70	
51 67	2	F275.N	SLMC I8T OR LATCH FAULT	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: 1A1A2A17, 1A1A3A(1,2)	AMA033* S@1
51 68			SPARE	
51 69			SPARE	
51 70	1	T276	TEST ACTUAL DATA TRANSFER DURING SLMC, SETS UP CM7 CODE WHICH RESETS AMA033, BREG + CREG -> ROM -> MB DR -> JEB REC + BIT 27(DIHR->MTW2) -> BREG -> ROM -> CM*DR -> JCM REC = CM7	
51 71			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A8FF7F	BIT 27 OF MTW2 = 1
			SERIALLY LOAD THE B REGISTER WITH A000FFFF	
			COMPARE THE B REGISTER TO A807AAAA	CREG = 08075555, C+B REG = A807FFFF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 483F0707EF	BREG->ROM, ROM->CM*DR, JEB->INMX, MTW2->RIM, ON KMV011
			PULSE THE CP DRIVERS WITH THE A REGISTER & MB DRIVERS WITH THE C REG.	
			PUNCH TAPE CODES - &C	ON KMV011 ROM = AC07FFFF -> CM*DR -> JCM* = CM7 => RESET SLMC LATCH
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			BRANCH TO MAJOR 51 MINOR 76	IF SLMC LATCH NOT RESET GO TO MIN 80
51 72			SPARE	
51 73			SPARE	
51 74			SPARE	
51 75			SPARE	
51 76	1	T277	TEST FOR SREM RESET OF TST2 ON CMA121	
51 77			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBF0F4FFF	RESET SIM NO-GO ON CMA121
			SINGLE READ MEMORY MODE-READ MB LINES-ADDRESS 0	
			BRANCH TO MAJOR 51 MINOR 78 ON NO-GO	
			BRANCH TO MAJOR 51 MINOR 83	
51 78	2	F277,N	FAULT IN SREM IBT OR FF => CMA121	
			ENABLE VERTICAL PARITY CHECK	
			SET THE I/O COMPLETE FLAG (GTC010*)	RESET TST2
			RESET THE I/O COMPLETE FLAG (GTC010*)	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A2A05, 1A1A3A(1,7,8)	KMA112* Sa1
51 79			SPARE	
51 80	2	F276.N	FAULT IN SLMC INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F7F0F0FFF COMPARE THE B REGISTER TO AC07FFFF STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	CM7 TO RESET SLMC LATCH, ALL MEM LD BREG INACTIVE CHECK FOR CORRECT CM7 CODE IN BREG
			INDICATORS: NO GO / DISPLAY: 1000000000 / REPLACE ASSEMBLIES: 1A1A3A22	AMA043* => CVM632
			INDICATORS: NO GO / DISPLAY: 1401777777 / REPLACE ASSEMBLIES: 1A1A2A04, 1A1A3A02	AMA054* Sa1
			INDICATORS: NO GO / DISPLAY: 25401777777 / REPLACE ASSEMBLIES: 1A1A3A(13,22), 2A1A1A19	GVM551* Sa1
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A3A08	AMD031* INPUT TO CMA109 OPEN
51 81			SPARE	
51 82			SPARE	
51 83	1	T278	TEST FOR RESET OF KMA112	
51 84			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F8FFF4FFF BRANCH TO MAJOR 51 MINOR 87 ON NO-GO	SIM NO-GO
51 85	2	F278.N	NO RESET OF KMA112 ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A3A(1,7)	
51 86			SPARE	
51 87	1	T279	TEST FOR INH OF LOAD MB DURING SREM	
51 88			SERIALLY LOAD THE B REGISTER WITH A INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F3F0B0F7F SINGLE READ MEMORY MODE-READ MB LINES-ADDRESS FFFFFFF COMPARE THE B REGISTER TO A BRANCH TO MAJOR 51 MINOR 89 ON NO-GO BRANCH TO MAJOR 51 MINOR 92	ROM->RIM ON KMA091

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
51 89	2	F279	IMA132* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 1A1A3A03	
51 90			SPARE	
51 91			SPARE	
51 92	1	T280	TEST FOR "INITIATE CI" DURING SREM ON IMV061	
51 93			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF1FODOFFF SINGLE READ MEMORY MODE-READ MB LINES-ADDRESS 0 COMPARE THE B REGISTER TO A LOGICALLY 'AND' C REGISTER AND A0004 - RESULT IN B & C REGISTER BRANCH TO MAJOR 51 MINOR 94 ON NO-GO BRANCH TO MAJOR 51 MINOR 98	MTW1->INMX ON IMV061
51 94	2	F280.N	INPUT TO AMV042 OR CMA025 OPEN ENABLE VERTICAL PARITY CHECK SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	RESET TST2
			INDICATORS: NO GO — DISPLAY: 400001 — REPLACE ASSEMBLIES: 1A1A3A(7,16)	
51 95			SPARE	
51 96			SPARE	
51 97			SPARE	
51 98			ENABLE VERTICAL PARITY CHECK	
51 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
52 00			BRANCH TO MAJOR 52 MINOR 3	
52 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
52 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
52 03	1	T281	TEST LSB OF MABC BRANCH TO MAJOR 44 MINOR 1	
52 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
53 00			BRANCH TO MAJOR 53 MINOR 3	
53 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
53 02	1	T283	TEST 3SB OF MABC PREVIOUS TEST = (44)T282 BRANCH TO MAJOR 60 MINOR 2	
53 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
54 00			BRANCH TO MAJOR 54 MINOR 3	
54 01	1	T331	TEST 5SB OF MABC PREVIOUS TEST = (75)T330 BRANCH TO MAJOR 79 MINOR 2	
54 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
54 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
55 00			BRANCH TO MAJOR 55 MINOR 3	
55 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
55 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
55 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
56 00			BRANCH TO MAJOR 56 MINOR 3	
56 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
56 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
56 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99	
57 00			BRANCH TO MAJOR 57 MINOR 3	
57 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
57 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
57 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
58 00			BRANCH TO MAJOR 58 MINOR 3	
58 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
58 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
58 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
59 00			BRANCH TO MAJOR 59 MINOR 3	
59 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
59 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
59 03			END OF MAJOR TEST	

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|TEST|DECISION | TEST/FAULT  |                                                                                    SELF-TEST PROGRAM                                                                                    |          REMARKS          |
| NO.|  LEVEL   |   NUMBER   |                                                                                                                                                                                         |                           |

            ********************************************************************************************************************************
            *                                                                                                                              *
            *                                                        GSPU SECTION TESTS                                                    *
            *                                                   MAJORS 60 & 61  TESTS T285 - T304                                          *
            *                                                                                                                              *
            ********************************************************************************************************************************

60 00                                 INITIALIZE
                                        DEFINE SELF TEST TAPE
                                        SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                          (GTC003*)
                                        ENABLE LOW LEVEL ON GTC001*
                                        BRANCH TO MAJOR 60 MINOR 3

60 01                                   STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON

60 02                                 INITIALIZE
                                        DEFINE SELF TEST TAPE
                                        SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE
                                          (GTC003*)
                                        ENABLE LOW LEVEL ON GTC001*

60 03   1       T285                  TEST +DELTA_VX --> DELTA_WX => COUNT UP AT 6.25 KHZ TO = 3
                                      PREVIOUS TEST = (53)T283
60 04                                   INITIATE GSPU CONTROL # 1
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200                    EA=0374
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000                    I/O REQ
                                        SERIALLY LOAD THE B REGISTER WITH A0000088                             SET UP GSPU CONTROL WORD =
                                                                                                                G1G2**G5
                                        INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD       GSPU CLK TEST
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40600                    EA=0401
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40400                    I/O REQ
                                        INITIATE GSPU CONTROL # 3
                                        ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600                    EA=0375
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400                    I/O REQ
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00                    EA=0376
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800                    I/O REQ
                                        COMPARE THE B REGISTER TO A0000003                                     CHECK COUNT -> BREG
                                        BRANCH TO MAJOR 60 MINOR 5  ON NO-GO
                                        BRANCH TO MAJOR 60 MINOR 59

60 05   2       T285.N                REPEAT TEST T285
60 06                                   INITIATE GSPU CONTROL # 1
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200                    EA=0374
                                        LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000                    I/O REQ
                                        SERIALLY LOAD THE B REGISTER WITH A0000088                             SET UP GSPU CONTROL WORD =
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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				G1G2*+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40600	EA=0401
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40400	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 7 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 59	
60 07	3	T285.NN	CHECK FOR NO TRANS GSPU -> BREG	
60 08			COMPARE THE B REGISTER TO A0000088	CONTROL CODE OF T285
			BRANCH TO MAJOR 60 MINOR 43 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 12	
60 09			SPARE	
60 10			SPARE	
60 11			SPARE	
60 12	4	T285.NNG	TEST +DELTA_VY --> DELTA_WZ => COUNT UP AT 6.25 KHZ TO = 3	
60 13			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000028	GSPU CONTROL WD = G3G4*+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 14 ON NO-GO	
	5	F285.NNGG	FAULT IN +DELTA_VX --> DELTA WX => COUNT = 3	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A2A(14,16), 2A1A3A(5,6,7)	AGB211* S@1
60 14 60 15	5	T285.NNGN	TEST DECODE OF COUNTER = 66, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG SERIALLY LOAD THE B REGISTER WITH A0000008 INITIATE GSPU CONTROL # 2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800 COMPARE THE B REGISTER TO A0000043 BRANCH TO MAJOR 60 MINOR 16 ON NO-GO BRANCH TO MAJOR 60 MINOR 37	GSPU CONTROL WD = G5 EA=0374 I/O REQ EA=0375 I/O REQ EA=0376 I/O REQ
60 16 60 17	6	T285.NNGNN	TEST FOR NO TRANS GSPU -> BREG COMPARE THE B REGISTER TO A0000008 BRANCH TO MAJOR 60 MINOR 21 ON NO-GO BRANCH TO MAJOR 60 MINOR 31	*CONTROL CODE OF T285.NNNN*
60 18 60 19 60 20			SPARE SPARE SPARE	
60 21 60 22	7	T285.NNGNN --->N	TEST DECODE OF COUNTER = 223, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG, CONTROL WD INACTIVE SERIALLY LOAD THE B REGISTER WITH A INITIATE GSPU CONTROL # 2 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00 LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800 COMPARE THE B REGISTER TO A00000E0 BRANCH TO MAJOR 60 MINOR 23 ON NO-GO	GSPU CONTROL WD INACTIVE EA=0374 I/O REQ EA=0375 I/O REQ EA=0376 I/O REQ
	8	F285.NNGNN --->NG	FAULT IN EN OF GSPU CONTROL WORD ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A1A18, 2A1A3A04	AGC110
60 23	8	T285.NNGNN ---->NN	TEST -DELTA_VY --> QUU223*(S.T.REC) => COUNT DOWN AT FULL RATE OF 100 KHZ	
60 24			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000CF	
			BRANCH TO MAJOR 60 MINOR 25 ON NO-GO	
	9	F285.NNGNN ---->NNG	NO RESET OF GSP3 LATCH	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A05	AGC010 Sa1
60 25	9	F285.NNGNN ---->NNN	FAULT IN EOP RESET GSPU OR AGC309* TIMING	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 317 — REPLACE ASSEMBLIES: 2A1A2A14, 2A1A3A(5,10)	AGC613* Sa1
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A3A(4,6,16)	AGC309*
60 26			SPARE	
60 27			SPARE	
60 28			SPARE	
60 29			SPARE	
60 30			SPARE	
60 31	7	T285.NNGNN ---->G	TEST AGC309* => I/O CMPLT, GTC010 -> QUT009 ON AGC309*	
60 32			SERIALLY LOAD THE B REGISTER WITH A0080008	GSPU CONTROL WD = G5

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF9FFFOFFF	MTW1->INMX ON AGC309*
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A008 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 60 MINOR 33 ON NO-GO	
	8	F285.NNGNN		
		--->GG	INPUT TO ARK019 OPEN	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A1A02	
60 33	8	F285.NNGNN		
		--->GN	FAULT IN GSPU -> BREG	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 2000000 — REPLACE ASSEMBLIES: 2A1A2A(14,16)	AGC309* S@1
			REPLACE ASSEMBLIES: 2A1A3A(3,5,6,7,16)	
60 34			SPARE	
60 35			SPARE	
60 36			SPARE	
60 37	6	T285.NNGNG	TEST -DELTA_VY --> QUU223*(S.T.REC) => COUNT DOWN AT FULL RATE OF 100 KHZ	
60 38			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000CF	
			BRANCH TO MAJOR 60 MINOR 39 ON NO-GO	
	7	F285.NNGNG		
		--->G	FAULT IN GSP1 IBT OR LATCH	
			ENABLE VERTICAL PARITY CHECK	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A12, 2A1A3A(2,3,4,5)	AGC624 OR CGB028 S@0
60 39	7	F285.NNGNG		
		--->N	FAULT IN GSP3 IBT OR LATCH => EN GSPU CONTROL WD	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A2A12, 2A1A3A(4,5)	BGC009* S@1
60 40			SPARE	
60 41			SPARE	
60 42			SPARE	
60 43	4	T285.NNN	TEST DECODE OF COUNTER = 66, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG	
60 44			SERIALLY LOAD THE B REGISTER WITH A0000008	GSPU CONTROL WD = G5
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000043	
			BRANCH TO MAJOR 60 MINOR 45 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 51	
60 45	5	T285.NNNN	TEST -DELTA_VY --> QUU223*(S.T.REC) => COUNT DOWN AT FULL RATE OF 100 KHZ	
60 46			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000CF	
			BRANCH TO MAJOR 60 MINOR 47 ON NO-GO	
	6	F285.NNNNG	FAULT IN GENERATION OF 6.25 KHZ & 50 KHZ, OR UP/DOWN CONTROL	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(1,2,3,4,5,16)	
60 47	6	T285.NNNNN	TEST DECODE OF COUNTER = 223, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG, CONTROL WD INACTIVE	
60 48			SERIALLY LOAD THE B REGISTER WITH A	GSPU CONTROL WD INACTIVE
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000E0	
			BRANCH TO MAJOR 60 MINOR 49 ON NO-GO	
	7	F285.NNNNN ---->G	FAULT IN GSPU CONTROL WORD	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A18	
60 49	7	F285.NNNNN ---->N	FAULT IN GSPU COUNTER, CLOCK GENERATOR, OR COUNTER RESET	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A2A(21,22)	
			2A1A3A(1,2,3,4,6)	
			INDICATORS: NO GO / DISPLAY: 60 / REPLACE ASSEMBLIES: 2A1A3A(2,4,5,7,10)	"COUNT UP" S@1
60 50			SPARE	
60 51	5	T285.NNNG	TEST -DELTA_VY --> QUU223*(S.T.REC) => COUNT DOWN AT FULL RATE OF 100 KHZ	
60 52			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A00000CF BRANCH TO MAJOR 60 MINOR 53 ON NO-GO	
	6	F285.NNNGG	FAULT IN 6.25 KHZ CLOCK RATE ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES NO GO / BLANK / 2A1A3A(1,2)	BGC305*
60 53	6	F285.NNNGN	FAULT IN CLOCK COUNTER,OR CLOCK WINDOW EN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES NO GO / 317 / 2A1A1A07	GYP011
			/ / 2A1A2A12	
			/ / 2A1A3A(3,4,6)	
			NO GO / XXX / 1A1A3A(6,7,8,9,10,11)	BKF034*
60 54			SPARE	
60 55			SPARE	
60 56			SPARE	
60 57			SPARE	
60 58			SPARE	
60 59	1	T286 T285.NG	TEST -DELTA_VX --> DELTA WY => COUNT UP AT 6.25 KHZ TO = 3	
60 60			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A00000C8	GSPU CONTROL WD = G1G2+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40A00	EA=0402
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40800	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 61 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 67	
60 61	2	T286.N	REPEAT TEST T286	
60 62			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A00000C8	GSPU CONTROL WD = G1G2+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40A00	EA=0402
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40800	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 63 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 67	
60 63	3	F286.NN	FAULT IN -DELTA_VX --> DELTA WY => COUNT = 3	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 313 / REPLACE ASSEMBLIES: 2A1A1A18; 2A1A2A(14,16); 2A1A3A(5,6,7,10)	AGB213* S@1
60 64			SPARE	
60 65			SPARE	
60 66			SPARE	
60 67	1	T287		
		T286.NG	TEST +DELTA_VY --> DELTA_WZ => COUNT UP AT 6.25 KHZ TO = 3	
60 68			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000028	GSPU CONTROL WD = G3G4*+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 69 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 75	
60 69	2	T287.N	REPEAT TEST T287	
60 70			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000028	GSPU CONTROL WD = G3G4*+G5

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 71 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 75	
60 71	3	F287.NN	FAULT IN +DELTA_VY --> DELTA_WZ => COUNT = 3	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 53 / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A2A(14,16), 2A1A3A(1,5,6,7)	AGB215* Sa1
60 72			SPARE	
60 73			SPARE	
60 74			SPARE	
60 75	1	T288		
		T287.NG	TEST GSPU CONTROL WORD = G3G4**G6 => +DELTA_VY -> DELTA_WZ => COUNT = 3	
60 76			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000024	GSPU CONTROL WD = G3G4**G6
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 77 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 80	
60 77	2	T288.N	REPEAT TEST T288	
60 78			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000024	GSPU CONTROL WD = G3G4**G6

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000003	CHECK COUNT -> BREG
			BRANCH TO MAJOR 60 MINOR 79 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 80	
60 79	3	F288.NN	FAULT IN GSPU G6	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 47 / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A3A05	AGD006* Sa1
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A3A05	AGD006*
60 80	1	T289		
		T288.NG	TEST AGC309* => I/O CMPLT, GTC010 -> OUT009 ON AGC309*	
60 81			SERIALLY LOAD THE B REGISTER WITH A0000008	GSPU CONTROL WD = G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OF9FFFOFFF	MTW1->INMX ON AGC309*
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A	
			LOGICALLY 'AND' C REGISTER AND A0080008 - RESULT IN B & C REGISTER	
			BRANCH TO MAJOR 60 MINOR 82 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 93	
60 82	2	T289.N	TEST FOR NO GSPU -> BREG	
60 83			COMPARE THE B REGISTER TO A0000008	
			BRANCH TO MAJOR 60 MINOR 84 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 88	
60 84	3	F289.NN	FAULT IN GSPU I/O ACKNOWLEDGE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: 2000000 / REPLACE ASSEMBLIES: 2A1A2A12, 2A1A3A(4,5)	IGC503* S@1
60 85			SPARE	
60 86			SPARE	
60 87			SPARE	
60 88	3	T289.NG	TEST GSPU UP/DOWN COUNTER DECODE AT 60, COUNT UP AT 50 KHZ	
60 89			SERIALLY LOAD THE B REGISTER WITH A0000004	GSPU CONTROL WD = G6
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A000003D	
			BRANCH TO MAJOR 60 MINOR 90 ON NO-GO	
	4	F289.NGG	FAULT IN COUNTER	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(2,3,4)	KGA002 OR KGA007
60 90	4	F289.NGN	FAULT IN COUNTER DECODE SEQUECE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 71 / REPLACE ASSEMBLIES: 2A1A2A01, 2A1A3A(2,4,5,6,7,16)	KGC210* S@0
60 91			SPARE	
60 92			SPARE	
60 93	1	T290	TEST DECODE OF COUNTER = 223, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG, CONTROL WD INACTIVE	
60 94			SERIALLY LOAD THE B REGISTER WITH A	GSPU CONTROL WD INACTIVE
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000E0	
			BRANCH TO MAJOR 60 MINOR 95 ON NO-GO	
			BRANCH TO MAJOR 60 MINOR 98	
60 95	2	F290.N	FAULT IN DECODE OF 223	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 341 / REPLACE ASSEMBLIES: 2A1A3A(2,4,5,7)	AGC204*
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A3A(2,3,4,5,7)	
60 96			SPARE	
60 97			SPARE	
60 98			ENABLE VERTICAL PARITY CHECK	
60 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
61 00			INITIALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* BRANCH TO MAJOR 61 MINOR 3	
61 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
61 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
61 03	1	T291	TEST DECODE OF COUNTER = 66, COUNT UP AT 50 KHZ => TRANS COUNT -> BREG	
61 04			SERIALLY LOAD THE B REGISTER WITH A0000008	GSPU CONTROL WD = G5
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000043	
			BRANCH TO MAJOR 61 MINOR 5 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 9	
61 05	2	F291.N	FAULT IN DECODE OF COUNT 66 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXX	2A1A1A18
	--	2A1A3A(4,5,7)

61 06			SPARE	
61 07			SPARE	
61 08			SPARE	
61 09	1	T292	TEST GSPU UP/DOWN COUNTER DECODE AT 60, COUNT UP AT 50 KHZ	
61 10			SERIALLY LOAD THE B REGISTER WITH A0000004	GSPU CONTROL WD = G6
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A000003D	
			BRANCH TO MAJOR 61 MINOR 11 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 15	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
61 11	2	F292.N	FAULT IN DECODE OF 60 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A1A18 2A1A3A(2,4,5,7)	
61 12			SPARE	
61 13			SPARE	
61 14			SPARE	
61 15	1	T293	TEST GSPU UP/DOWN COUNTER DECODE AT 111, COUNT UP AT 50 KHZ	
61 16			SERIALLY LOAD THE B REGISTER WITH A0000002	GSPU CONTROL WD = G7
			INITIATE GSPU CONTROL # 2	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000070	
			BRANCH TO MAJOR 61 MINOR 17 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 21	
61 17	2	F293.N	FAULT IN DECODE OF 111 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A1A18 2A1A3A(2,4,5)	
61 18			SPARE	
61 19			SPARE	
61 20			SPARE	
61 21	1	T294	TEST -DELTA_VY --> QUU223*(S.T.REC) => COUNT DOWN AT FULL RATE OF 100 KHZ	
61 22			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			COMPARE THE B REGISTER TO A00000CF BRANCH TO MAJOR 61 MINOR 23 ON NO-GO BRANCH TO MAJOR 61 MINOR 29	
61 23	2	T294.N	TEST FOR COUNTER AT ZERO	
61 24			COMPARE THE B REGISTER TO A BRANCH TO MAJOR 61 MINOR 25 ON NO-GO	
	3	F294.NG	FAULT IN COUNT DOWN CONTROL OR 100 KHZ CLK TO COUNTER ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	2A1A1A18
		2A1A3A(5,6,7,8)

61 25	3	F294.NN	COUNTER FAULT WHEN COUNT DOWN ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXX	2A1A3A(2,3,4)

61 26			SPARE	
61 27			SPARE	
61 28			SPARE	
61 29	1	T295	TEST COUNT DOWN AT 1/2 RATE, -DELTA_VY --> QUU223*(S.T.REC)	
61 30			SERIALLY LOAD THE B REGISTER WITH A0000032	GSPU CONTROL WD = G3G4+G7
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 951 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000E5	
			BRANCH TO MAJOR 61 MINOR 31 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 37	
61 31	2	T295.N	REPEAT TEST T295	
			TEST COUNT DOWN AT 1/2 RATE, -DELTA_VY --> QUU223*(S.T.REC)	
61 32			SERIALLY LOAD THE B REGISTER WITH A0000032	GSPU CONTROL WD = G3G4+G7
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 951 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000E5	
			BRANCH TO MAJOR 61 MINOR 33 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 37	
61 33	3	F295.NN	FAULT IN 1/2 RATE CONTROL	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS / DISPLAY / REPLACE ASSEMBLIES	
			NO GO / XXX12A1A3A(1,5,8)	AGB024*
61 34			SPARE	
61 35			SPARE	
61 36			SPARE	
61 37	1	T296		
		T296.NG	TEST COUNT DOWN AT 1/16 RATE, -DELTA_VY --> QUU223*(S.T. REC)	
61 38			SERIALLY LOAD THE B REGISTER WITH A0000031	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 951 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000FD	
			BRANCH TO MAJOR 61 MINOR 39 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 43	
61 39	2	F296.N	FAULT IN 1/16 RATE CONTROL	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A3A(1,5,8,13)	CGB025* Sa1
61 40			SPARE	
61 41			SPARE	
61 42			SPARE	
61 43	1	T297	TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION	
			-->DELTA_WX , -DELTA_VY -->	
61 44			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40600	EA=0401
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40400	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000038	
			BRANCH TO MAJOR 61 MINOR 45 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 49	
61 45	2	F297.N	XTK220* OR CGB006* ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A3A(6,7,8)	
61 46			SPARE	
61 47			SPARE	
61 48			SPARE	
61 49	1	T298	TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION	
			--> DELTA_WY , -DELTA_VX -->	
61 50			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A00000C8	GSPU CONTROL WD = G1G2+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40600	EA=0+01

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40400	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000C8	
			BRANCH TO MAJOR 61 MINOR 51 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 55	
61 51	2	F298.N	XTK220* OR IED402 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A2A(14,16); 2A1A3A(6,10)	
61 52			SPARE	
61 53			SPARE	
61 54			SPARE	
61 55	1	T299	TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION	
			--> DELTA_WY , +DELTA_VX -->	
61 56			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000088	SET UP GSPU CONTROL WORD = G1G2*+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0F8FFF0FD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40A00	EA=0402
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40800	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000088	
			BRANCH TO MAJOR 61 MINOR 57 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 61	
61 57	2	F299.N	XTK221* OR IED401	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A1A18; 2A1A2A(14,16); 2A1A3A(6,7)	
61 58			SPARE	
61 59			SPARE	
61 60			SPARE	
61 61	1	T300	TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION	
			--> DELTA_WY , G2* => NO DRIVER ACTIVE	
61 62			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000048	GSPU CONTROL WD = G2+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40A00	EA=0402
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40800	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000048	
			BRANCH TO MAJOR 61 MINOR 63 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 67	
61 63	2	F300.N	INPUT TO CGB021* OPEN	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX — REPLACE ASSEMBLIES: 2A1A3A06	
61 64			SPARE	
61 65			SPARE	
61 66			SPARE	
61 67	1	T301	TEST FOR ACTIVE RECEIVERS GR DRIVERS OF GSPU SECTION	
			--> DELTA_WZ , -DELTA_VY	
61 68			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A0000038	GSPU CONTROL WD = G3G4+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A0000038	
			BRANCH TO MAJOR 61 MINOR 69 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 73	
61 69	2	F301.N	INPUT TO CGB022* OPEN	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: XXX12A1A3A06 — REPLACE ASSEMBLIES	
61 70			SPARE	
61 71			SPARE	
61 72			SPARE	
61 73	1	T302	TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION	
			--> DELTA_WZ , -DELTA_VX -->	
61 74			INITIATE GSPU CONTROL # 1	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			SERIALLY LOAD THE B REGISTER WITH A00000C8	GSPU CONTROL WD = G1G2+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41200	EA=0404
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A41000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A00000C8	
			BRANCH TO MAJOR 61 MINOR 75 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 79	
61 75	2	F302.N	XTK222* OR IED402 ACTIVE	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXX	2A1A2A(14,16) 2A1A3A06

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61 76                       SPARE
61 77                       SPARE
61 78                       SPARE

61 79   1       T303        TEST FOR ACTIVE RECEIVERS OR DRIVERS OF GSPU SECTION
                            --> DELTA_WX , +DELTA_VY -->
61 80                         INITIATE GSPU CONTROL # 1
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200          EA=0374
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000          I/O REQ
                              SERIALLY LOAD THE B REGISTER WITH A0000028                   GSPU CONTROL WD = G3G4*+G5
                              INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD   GSPU CLK TEST
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40600          EA=0401
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A40400          I/O REQ
                              INITIATE GSPU CONTROL # 3
                              ENABLE CONTROLLED TIMING PULSE INTERVAL 959 ON GTC001*
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600          EA=0375
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400          I/O REQ
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00          EA=0376
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800          I/O REQ
                              COMPARE THE B REGISTER TO A0000028
                              BRANCH TO MAJOR 61 MINOR 81 ON NO-GO
                              BRANCH TO MAJOR 61 MINOR 85

61 81   2       F303.N      XTK220* OR IED404 ACTIVE
                              ENABLE VERTICAL PARITY CHECK
                              STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
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INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXX	2A1A2A(14,16) 2A1A3A01

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61 82                       SPARE
61 83                       SPARE
61 84                       SPARE

61 85   1       T304        TEST INPUTS TO CGB023* AND INH OF DELTA_W RECEIVERS
61 86                         SERIALLY LOAD THE B REGISTER WITH A00000D8                   GSPU CONTROL WD =
                                                                                          G1G2+G3*G4+G5
                              INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD   GSPU CLK TEST
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200          EA=0374
                              LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000          I/O REQ
                              INITIATE GSPU CONTROL # 3
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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 61 MINOR 87 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 91	
61 87	2	F304.N	FAULT IN CG8023* OR DELTA_WX RECEIVER	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	XXX	2A1A1A18
		2A1A2A(14,16)
		2A1A3A06

61 88			SPARE	
61 89			SPARE	
61 90			SPARE	
61 91	1	T305	TEST INPUTS TO CG8023* AND INH OF DELTA_W RECEIVERS	
61 92			SERIALLY LOAD THE B REGISTER WITH A00000A8	GSPU CONTROL WD = G1G2*+G3G4*+G5
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFFD	GSPU CLK TEST
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F200	EA=0374
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F000	I/O REQ
			INITIATE GSPU CONTROL # 3	
			ENABLE CONTROLLED TIMING PULSE INTERVAL 971 ON GTC001*	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F600	EA=0375
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F400	I/O REQ
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3FA00	EA=0376
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A3F800	I/O REQ
			COMPARE THE B REGISTER TO A	
			BRANCH TO MAJOR 61 MINOR 93 ON NO-GO	
			BRANCH TO MAJOR 61 MINOR 98	
61 93	2	F305.N	FAULT IN CG8023* OR DELTA_WY OR DELTA_WZ REC	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: XXX / REPLACE ASSEMBLIES: 2A1A1A18, 2A1A2A(14,16), 2A1A3A06	
61	94		SPARE	
61	95		SPARE	
61	96		SPARE	
61	97		SPARE	
61	98		ENABLE VERTICAL PARITY CHECK	
61	99		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
62 00			BRANCH TO MAJOR 62 MINOR 3	
62 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
62 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
62 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
63 00			BRANCH TO MAJOR 63 MINOR 3	
63 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
63 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
63 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
64	00		BRANCH TO MAJOR 64 MINOR 3	
64	01		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
64	02		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
64	03		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
65 00			BRANCH TO MAJOR 65 MINOR 3	
65 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
65 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
65 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
66 00			BRANCH TO MAJOR 66 MINOR 3	
66 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
66 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
66 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
67 00			BRANCH TO MAJOR 67 MINOR 3	
67 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
67 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
67 03			END OF MAJOR TEST.	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
68 00			BRANCH TO MAJOR 68 MINOR 3	
68 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
68 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
68 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
69 00			BRANCH TO MAJOR 69 MINOR 3	
69 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
69 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
69 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			********** CIU AND TACAN TEST CONTROL TESTS MAJORS 70 & 71, TEST T310 - T329 **********	
70 00			INITALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) BRANCH TO MAJOR 70 MINOR 3	
70 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
70 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
70 03	1	T310	TEST EOPA, TO TACAN, AREG->GTC902->QUN902->BREG, LSHD=VALID TAC ADDR=4, CHECK FOR CORRECT DECODE, CHECK FOR CIU MODE 2 RESET TST2(SIM NO-GO) PREVIOUS TEST = (61)T305	
70 04			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF4FBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555554 FROM A REGISTER TO B REGISTER	EA3 ACTIVE = TACAN INTF SIM NO-GO, POSFIX PRESENT TEST
	2	F310.1	FAULT LOC WITHIN TEST T310 - FAULT IN CIU1 CONTROL	
			INDICATORS: NO GO / NO GO DISPLAY: 1000000 / 4 REPLACE ASSEMBLIES: 2A1A1A05 / 1A1A3A25 / 2A1A1A05 / 2A1A3A(10,11)	KCC053* KCC013* S@0
	1	T310(CONT)	BRANCH TO MAJOR 70 MINOR 5 ON NO-GO BRANCH TO MAJOR 70 MINOR 19	
70 05	2	T310.2	ISOLATE BETWEEN NO RESET OF TST2 & INVALID CIU OR TAC ADDR DECODE	
70 06			SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) BRANCH TO MAJOR 70 MINOR 7 ON NO-GO BRANCH TO MAJOR 70 MINOR 13	RESET TST2 IF NOT RESET IN T310
70 07	3	T310.2.N	TEST DATA TRANSFER IN T310	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
70 08			COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 70 MINOR 9 ON NO-GO	
	4	F310.2.NG	DECODE OF INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A8(1,5,9)	CCI094
70 09	4	F310.2.NN	FAULT IN DATA TRANSFER OF T310 => INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 5252525252 — REPLACE ASSEMBLIES: 2A1A3A8(4,7,9,10,11)	ACI031 S@0
			INDICATORS: NO GO — DISPLAY: 1252525252 — REPLACE ASSEMBLIES: 2A1A1A04	KCC047* => MRK031 OR ACI031 S@1
			REPLACE ASSEMBLIES: 2A1A3A8(7,9,11)	
70 10			SPARE	
70 11			SPARE	
70 12			SPARE	
70 13	3	F310.2.G	TEST FOR DATA TRANSFER	
70 14			COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 70 MINOR 15 ON NO-GO	
	4	F310.2.GG	FAULT IN RESET OF TST2 BUT NO FAULT IN DATA TRANSFER ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A8(13,15)	
70 15	4	F310.2.GN	FAULT IN CIU1 IBT OR ACC023 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1777777777 — REPLACE ASSEMBLIES: 2A1A2A06	ACC023 S@0
			REPLACE ASSEMBLIES: 2A1A3A8(7,10)	
70 16			SPARE	
70 17			SPARE	
70 18			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
70 19 70 20	1	T311	TEST DATA TRANSFER IN T310 COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 70 MINOR 21 ON NO-GO BRANCH TO MAJOR 70 MINOR 37	
70 21 70 22	2	T311.N	TEST FOR NO TRANSFER OF DATA TO BREG COMPARE THE B REGISTER TO AAAAAAAA BRANCH TO MAJOR 70 MINOR 23 ON NO-GO BRANCH TO MAJOR 70 MINOR 26	
70 23	3	F311.NN	FAULT IN DATA TRANSFERED QUN902 -> BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 12525252521 2A1A1A16 — REPLACE ASSEMBLIES: 2A1A3A(5,7,9,12,16)	ARB171*
			INDICATORS: NO GO — DISPLAY: 525252525111A1A3A09 — REPLACE ASSEMBLIES: A09	ACI031 INPUT TO CCI111* S@1
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX12A1A3A(9,11,16) — REPLACE ASSEMBLIES:	IYC035* S@1
70 24			SPARE	
70 25 70 26 70 27	3	T311.NG	SPARE TEST FOR AKA343* S@0 => FAULT IN TAC INTF CLK C READ & COMPARE MISCELLANEOUS WORD 1 WITH A000002 LOGICALLY 'AND' C REGISTER AND A REGISTER-RESULT IN B & C REGISTERS BRANCH TO MAJOR 70 MINOR 28 ON NO-GO BRANCH TO MAJOR 70 MINOR 31	
70 28	4	F311.NGN	FAULT IN INTF CLK C ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 4011A1A3A(24,25,27,28) — REPLACE ASSEMBLIES:	AKA343* S@0
70 29 70 30			SPARE SPARE	
70 31 70 32	4	T311.NGG	TEST EOPA, AREG->GTC902->QUC902->BREG SERIALLY LOAD THE B REGISTER WITH AAAAAAAA LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF0FBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555551 FROM A REGISTER TO B REGISTER COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 70 MINOR 33 ON NO-GO	EA3 NOT ACTIVE = CIU INTF POSFIX PRESENT TEST

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
	5	F311.NGGG	FAULT IN TACAN INTF CLK C OR GDATC ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A3A1(4,7,9,13)	BCI025* OR BCI026*
70 33	5	F311.NGGN	FAULT IN "TAC + CIU INTF SHIFT CLK" ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: 1777777777; REPLACE ASSEMBLIES: 1A1A3A24, 2A1A1A03,2A3(7,8,13)	GCI076* S@1
70 34			SPARE	
70 35			SPARE	
70 36			SPARE	
70 37	1	T312	TEST EOPA TO TACAN WITH INVALID TACAN ADDR = C, TEST GENERATION OF POSFIX GTC904 -> QUC904 -> ICP202* => SET NO-GO FLAG	
70 38			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200	EA3 ACTIVE = TACAN INTF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 5555555C FROM A REGISTER TO B REGISTER	
	2	F312.1	FAULT LOC WITHIN TEST T312- FAULT IN DC SET OF NO-GO FLAG	
			INDICATORS: TEST SET FAULT; DISPLAY: 600001; REPLACE ASSEMBLIES: 2A1A1A13	
	1	T312(CONT)	BRANCH TO MAJOR 70 MINOR 48 ON NO-GO	
70 39	2	T312.2	TEST EOPA TO TAC, INVALID TAC ADDR = 6 => POSFIX => NO-GO	
70 40			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555556 FROM A REGISTER TO B REGISTER	
			BRANCH TO MAJOR 70 MINOR 41 ON NO-GO	
			BRANCH TO MAJOR 70 MINOR 42	
70 41	3	F312.2.N	FAULT IN DECODE OF INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(5,9)	ICB081* S@1
70 42 70 43	3	T312.2.G	TEST INVALID ADDR = 0 => POSIFX => NO-GO SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555550 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 44 ON NO-GO BRANCH TO MAJOR 70 MINOR 45	POSFIX PRESENT TEST
70 44	4	F312.2.GN	FAULT IN DECODE OF INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A09	BCI085* S@1
70 45 70 46	4	T312.2.GG	TEST FOR CORRECT SIZE POSFIX PULSE, INVALID ADDR = 0 SERIALLY LOAD THE B REGISTER WITH AAAAAAAA INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF1FFF SIMULATE CIU EIP SERIAL TRANSFER OF 55555550 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 47 ON NO-GO	INH PROCEED RESET OF POSFIX CNTR
	5	F312.2.GGG	FAULT IN GEN OF POSFIX ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(7,8,9)	ICP202* S@1
70 47	5	F312.2.GGN	FAULT IN POSFIX PRESENT => NO-GO ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A1A07, 2A1A3A(8,9)	CYC002* S@1
70 48 70 49	1	T313	TEST MSB OF ADDR INH OF DATA TRANSFER => TRANSFER ALL ZEROS, MSHD OF BREG BYPASSED => A COMPARE THE B REGISTER TO A BRANCH TO MAJOR 70 MINOR 50 ON NO-GO BRANCH TO MAJOR 70 MINOR 53	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
70 50	2	F313.N	FAULT IN INH OF CCI111* ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 1252525252 — REPLACE ASSEMBLIES: 2A1A3A(7,8)	KCI036* S@1
			INDICATORS: NO GO — DISPLAY: 2525252521 — REPLACE ASSEMBLIES: 2A1A3A(5,7,9)	ICI101 S@1
70 51			SPARE	
70 52				
70 53	1	T314	TEST EOPA TO TAC, INVALID TAC ADDR = 6 => POSFIX => NO-GO	
70 54			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555556 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 61 ON NO-GO BRANCH TO MAJOR 70 MINOR 55	EA3 ACTIVE = TACAN INTF POSFIX PRESENT TEST
70 55	2	T314.G	TEST CIU VALID ADDR = 2 => NO POSFIX => GO	
70 56			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555552 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 57 ON NO-GO	EA3 NOT ACTIVE = CIU INTF POSFIX PRESENT TEST
	3	F314.GG	ICI053* INPUT TO BCI075 S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A09	
70 57	3	F314.GN	ICI053* S@1 ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A05	
70 58			SPARE	
70 59			SPARE	
70 60			SPARE	
70 61	1	T315	TEST INVALID TACAN ADDR = 5 => POSFIX => NO-GO	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200	EA3 ACTIVE = TACAN INTF
70 62			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555555 FROM A REGISTER TO B REGISTER	
	2	F315.1	FAULT LOC WITHIN TEST T315 - FAULT IN RESET OF NO-GO FLAG	
			INDICATORS: TEST SET FAULT / DISPLAY: 600001 / REPLACE ASSEMBLIES: 2A1A1A14	
	1	T315(CONT)	BRANCH TO MAJOR 70 MINOR 68 ON NO-GO	
70 63	2	T315.2	TEST CIU VALID ADDR = 1 => NO POSFIX => GO	
70 64			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200	EA3 NOT ACTIVE = CIU INTF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555551 FROM A REGISTER TO B REGISTER	
			BRANCH TO MAJOR 70 MINOR 65 ON NO-GO	
	3	F315.2.G	IC1054* INPUT TO BC1075 S@1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A09	
70 65	3	F315.2.N	IC1054* S@1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A05	
70 66			SPARE	
70 67			SPARE	
70 68	1	T316	TACAN + CIU INVALID ADDR = 8 => POSFIX => NO-GO	
70 69			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555558 FROM A REGISTER TO B REGISTER	
			BRANCH TO MAJOR 70 MINOR 73 ON NO-GO	
70 70	2	F316.G	FAULT IN DECODE OF INVALID ADDR	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A(1,4,9,13)	CCI084* S@1 OR BCI026*
70 71			SPARE	
70 72			SPARE	
70 73	1	T317	TEST TACAN VALID ADDR = 4 => NO POSFIX, CHECK RESET OF NO-GO FLAG	
70 74			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200	EA3 ACTIVE = TACAN INTF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555554 FROM A REGISTER TO B REGISTER	
			BRANCH TO MAJOR 70 MINOR 75 ON NO-GO	
			BRANCH TO MAJOR 70 MINOR 78	
70 75	2	F317.N	CYC004* S@1	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1J3A13	
70 76			SPARE	
70 77			SPARE	
70 78	1	T318	TEST EOPA TO CIU, AREG->GTC902->QUC902->BREG, LSHD = VALID CIU ADDR = 1	
			=>NO POSFIX => GO	
70 79			SERIALLY LOAD THE B REGISTER WITH AAAAAAAA	
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200	EA3 NOT ACTIVE = CIU INTF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF	POSFIX PRESENT TEST
			SIMULATE CIU EIP SERIAL TRANSFER OF 55555551 FROM A REGISTER TO B REGISTER	
			BRANCH TO MAJOR 70 MINOR 80 ON NO-GO	
			BRANCH TO MAJOR 70 MINOR 83	
70 80	2	T318.N	TEST DATA TRANSFER IN T318	
70 81			COMPARE THE B REGISTER TO A5555555	
			BRANCH TO MAJOR 70 MINOR 82 ON NO-GO	
	3	F318.NG	FAULT IN DECODE OF INVALID ADDR	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A3A09	BCI084* INPUT TO BCI086* OR BCI054* INPUT TO BCI084 SA1
70 82	3	F318.NN	FAULT IN DATA TRANSFER QUC902 -> BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: 125252525212A1A3A09	BCI102*
			INDICATORS: NO GO; DISPLAY: 52525252512A1A3A(4,7,9)1	BCI102* SA1
70 83 70 84	1	T319	TEST DATA TRANSFER IN T318 COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 70 MINOR 85 ON NO-GO BRANCH TO MAJOR 70 MINOR 88	
70 85	2	F319.N	FAULT IN DATA TRANSFER QUC902 -> BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: XXXXXXXXXX12A1A3A07	ACI014*
70 86 70 87			SPARE SPARE	
70 88 70 89	1	T320	TEST CIU INVALID ADDR = 4 => POSFIX => NO-GO LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOFBF SIMULATE CIU EIP SERIAL TRANSFER OF 55555554 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 93 ON NO-GO	EA3 NOT ACTIVE = CIU INTF POSFIX PRESENT TEST
70 90	2	F320.G	FAULT IN DECODE OF INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO; DISPLAY: BLANK; REPLACE ASSEMBLIES: 2A1A3A09	BCI086*
70 91 70 92			SPARE SPARE	
70 93	1	T321	TEST FOR GENERATION OF PROPER WIDTH POSFIX PULSE, INVALID CIU ADDR = 4	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
70 94			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF1FFF SIMULATE CIU EIP SERIAL TRANSFER OF 55555554 FROM A REGISTER TO B REGISTER BRANCH TO MAJOR 70 MINOR 98 ON NO-GO	EA3 NOT ACTIVE = CIU INTF INH PROCEED RESET OF POSFIX CNTR
70 95	2	F321.G	FAULT POSFIX GENERATOR OR RECEIVER => NO SET OF NO-GO ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	12A1A3A(7,8,9,10,12)

70 96			SPARE	
70 97			SPARE	
70 98			ENABLE VERTICAL PARITY CHECK	
70 99			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
71 00			INITALIZE DEFINE SELF TEST TAPE SET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST NCU CLOCK MODE (GTC003*) ENABLE LOW LEVEL ON GTC001* RESET INHIBIT INCREMENT CP FLAG & ENABLE SELF TEST CIU CLOCK MODE (GTC003*) BRANCH TO MAJOR 71 MINOR 3	
71 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
71 02	2	F331.1	FAULT IN 5SR OF MABC STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 1A1A1A(21,23)	
71 03	1	T322	TEST BIOPB => RESET TST2(SIM NO-GO), BREG=0FFFFFFF->GTC903->QUC903->BREG,	
71 04			MSHD AREG = VALID CIU ADDR = B => NO POSFIX => GO LOAD A REGISTER WITH 05555555 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH 0FBFFF0F7F LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH 0FBFFF57FF SERIAL SHIFT B TO B REGISTER-CHECK ADDRESS B	ROM->RIM EA3 NOT ACTIVE = CIU INTF INH PROCEED RESET OF POSFIX CNTR, CIU BCLK EN INH, SIM NO GO
	2	F322.1	FAULT LOC WITHIN TEST T322 - CIU2 HANGUP INDICATORS: TEST SEL FAULT — DISPLAY: — REPLACE ASSEMBLIES: 12A1A3A10	KCC014* S@0
	1	T322(CONT)	BRANCH TO MAJOR 71 MINOR 5 ON NO-GO BRANCH TO MAJOR 71 MINOR 11	
71 05 71 06	2	T322.2	ISOLATE BETWEEN NO RESET OF TST2 AND GEN POSFIX SET THE I/O COMPLETE FLAG (GTC010*) RESET THE I/O COMPLETE FLAG (GTC010*) BRANCH TO MAJOR 71 MINOR 7 ON NO-GO	RESET TST2 IF NO RESET IN T322
	3	F322.2.6	FAULT IN CIU2 IBT OR FF ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A2A06, 2A1A3A17,10	KCC014*
71 07	2	F322.2.N	FAULT IN TRANSFER OF AREG -> CIU ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 2A1A3A11	CCC025*
71 08			SPARE	
71 09			SPARE	
71 10			SPARE	
71 11	1	T323	TEST DATA TRANSFER IN T322	
71 12			COMPARE THE B REGISTER TO A5555555 BRANCH TO MAJOR 71 MINOR 13 ON NO-GO BRANCH TO MAJOR 71 MINOR 20	
71 13	2	F323.N	FAULT IN DATA TRANSFER BREG->GTC903->QUC903->BREG ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: 2400000000 / REPLACE ASSEMBLIES: 2A1A1A03, 2A1A3A08	ACC016* S@1
			INDICATORS: NO GO / DISPLAY: 1252525252 / REPLACE ASSEMBLIES: 2A1A1A(16,20), 2A1A3A(9,16)	IAT025
			INDICATORS: NO GO / DISPLAY: 525252525 / REPLACE ASSEMBLIES: 2A1A1A(16,20), 2A1A3A(5,8,9,16)	ARB063* S@1
			INDICATORS: NO GO / DISPLAY: XXXXXXXXXXX / REPLACE ASSEMBLIES: 2A1A1A07, 2A1A3A(13,16)	CYC015* S@1
71 14			SPARE	
71 15			SPARE	
71 16			SPARE	
71 17			SPARE	
71 18			SPARE	
71 19			SPARE	
71 20	1	T324	TEST EIOPB BOTH "CIU BCLK" AND "TAC+CIU INTF SHIFT CLK, CHECK ADDR DECODE OF VALID CIU ADDR = A	
71 21			LOAD A REGISTER WITH 00055555 INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFFOF7F LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200	ROM->RIM EA3 NOT ACTIVE = CIU INTF

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF1FSF	INH PROCEED RESET OF POSFIX CNTR
			SERIAL SHIFT B TO B REGISTER-CHECK ADDRESS A BRANCH TO MAJOR 71 MINOR 22 ON NO-GO BRANCH TO MAJOR 71 MINOR 29	
71 22	2	F324.N	FAULT IN DECODE OF INVALID ADDR ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 12A1A3A09	ICI053* INPUT TO CCI084 S@1
71 23			SPARE	
71 24			SPARE	
71 25			SPARE	
71 26			SPARE	
71 27			SPARE	
71 28			SPARE	
71 29		T325	SPARE TEST NUMBER AND LOCATION BRANCH TO MAJOR 71 MINOR 38	
71 30			SPARE	
71 31			SPARE	
71 32			SPARE	
71 33			SPARE	
71 34			SPARE	
71 35			SPARE	
71 36			SPARE	
71 37			SPARE	
71 38	1	T326	TEST EIOPB (NCU EOP), BREG->GTC902->QUN902->BREG, CIU BCLK EN, VALID TAC ADDR = 4	
71 39			LOAD A REGISTER WITH 00055555	
			INITIATE SELF TEST MODE 1-LOAD SELF TEST REGISTER WITH OFBFFF0F7F	ROM->RIM
			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A01200	EA3 ACTIVE = TACAN INTF
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFF1BFF	INH PROCEED RESET OF POSFIX CNTR, INH TAC+CIU INTF SHIFT CLK
			SERIAL SHIFT B TO B REGISTER-CHECK ADDRESS 4 BRANCH TO MAJOR 71 MINOR 40 ON NO-GO BRANCH TO MAJOR 71 MINOR 47	
71 40	2	F326.N	FAULT IN AREG -> TAC ADDR OR ADDR DECODE ENABLE VERTICAL PARITY CHECK	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: 2A1A3A(9,11)	
71 41				
71 42				
71 43				
71 44				
71 45				
71 46				
71 47	1	T327	TEST DATA TRANSFER IN T326	
71 48			COMPARE THE B REGISTER TO A0055555	
			BRANCH TO MAJOR 71 MINOR 49 ON NO-GO	
			BRANCH TO MAJOR 71 MINOR 56	
71 49	2	F327.N	FAULT IN BREG -> GTC902, OR INH OF TAC+CIU INTF SHIFT CLK	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: 177652525 — REPLACE ASSEMBLIES: 2A1A3A11	IRB144 INPUT TO CCC024* S@1
			INDICATORS: NO GO — DISPLAY: 125252 — REPLACE ASSEMBLIES: 2A1A3A11	CCC024* S@1
			INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A1A07	CYC019* S@1
			REPLACE ASSEMBLIES: 2A1A3A(13,16)	
71 50			SPARE	
71 51			SPARE	
71 52			SPARE	
71 53			SPARE	
71 54			SPARE	
71 55			SPARE	
71 56	1	T328	TEST SERIAL TRANSFER TO NCU TAC INTF, DATA REQ A,	
			BREG->GTN002->QUU002(S.T.	
			TAC REC)->ICT131->BREG, BREG UNCHANGED EXCEPT BIT #1 (0->1)	
71 57			LOAD DISCRETE INPUT WORD (EIP/EOP CODE) WITH A00200	EA3 NOT ACTIVE = CIU INTF
			SERIALLY LOAD THE B REGISTER WITH AAAAAAA0	
			INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFODFE	EN SIM TAC OD TO BREG, DATA REQ A
			SIMULATE CIU EIP SERIAL TRANSFER OF AAA55554 FROM A REGISTER TO B REGISTER	
			COMPARE THE B REGISTER TO AAAAAAA1	
			BRANCH TO MAJOR 71 MINOR 58 ON NO-GO	
			BRANCH TO MAJOR 71 MINOR 67	
71 58	2	F328.N	FAULT IN SERIAL TRANSFER TO NCU TAC INTF	
			ENABLE VERTICAL PARITY CHECK	
			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	

MAJOR	MINOR	TEST/FAULT LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
				INDICATORS: NO GO — DISPLAY: 125252524 — REPLACE ASSEMBLIES: 2A1A3A(12,14)	AYC008* S@1
				INDICATORS: NO GO — DISPLAY: 525252536 — REPLACE ASSEMBLIES: 2A1A3A(12,14)	QUU002 S@1
				INDICATORS: NO GO — DISPLAY: 37777761 — REPLACE ASSEMBLIES: 2A1A3A09	IYC007* S@1
				INDICATORS: NO GO — DISPLAY: 26 — REPLACE ASSEMBLIES: 2A1A3A05	BCI201
				INDICATORS: NO GO — DISPLAY: 1 — REPLACE ASSEMBLIES: 2A1A1A(3,4,7); 2A1A3A(12,13)	ANI043* S@1 OR ANK021
				INDICATORS: NO GO — DISPLAY: XXXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A3A(5,9,11,13,14,16)	
71	59			SPARE	
71	60			SPARE	
71	61			SPARE	
71	62			SPARE	
71	63			SPARE	
71	64			SPARE	
71	65			SPARE	
71	66			SPARE	
71	67	1	T329	TEST SERIAL TRANSFER TO NCU TAC INTF, DATA REQ B, BREG UNCHANGED EXCEPT BIT #2 (0->1)	
71	68			SERIALLY LOAD THE B REGISTER WITH AAAAAAA0 INITIATE SELF TEST MODE 2-LOAD SELF TEST REGISTER WITH OFBFFFOEFE SIMULATE CIU EIP SERIAL TRANSFER OF AAA55554 FROM A REGISTER TO B REGISTER COMPARE THE B REGISTER TO AAAAAAA2 BRANCH TO MAJOR 71 MINOR 69 ON NO-GO BRANCH TO MAJOR 71 MINOR 98	EN SIM TAC OC TO BREG, DATA REQ B
71	69	2	F329.N	FAULT IN SERIAL TRANSFER TO NCU TAC INTF ENABLE VERTICAL PARITY CHECK STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
				INDICATORS: NO GO — DISPLAY: 2 — REPLACE ASSEMBLIES: 2A1A1A07; 2A1A3A(12,14)	ANI045* S@1 OR INI022
				INDICATORS: NO GO — DISPLAY: XXXXXXXXXXX — REPLACE ASSEMBLIES: 2A1A1A01; 2A1A3A(5,8,12,13,14)	
71	70			SPARE	
71	71			SPARE	
71	72			SPARE	
71	73			SPARE	
71	74			SPARE	
71	75			SPARE	
71	76			SPARE	
71	77			SPARE	
71	78			SPARE	
71	79			SPARE	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
71	80		SPARE	
71	81		SPARE	
71	82		SPARE	
71	83		SPARE	
71	84		SPARE	
71	85		SPARE	
71	86		SPARE	
71	87		SPARE	
71	88		SPARE	
71	89		SPARE	
71	90		SPARE	
71	91		SPARE	
71	92		SPARE	
71	93		SPARE	
71	94		SPARE	
71	95		SPARE	
71	96		SPARE	
71	97		SPARE	
71	98		ENABLE VERTICAL PARITY CHECK	
71	99		END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
72	00		BRANCH TO MAJOR 72 MINOR 3	
72	01		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
72	02		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
72	03		END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
73 00			BRANCH TO MAJOR 73 MINOR 3	
73 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
73 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
73 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
74 00			BRANCH TO MAJOR 74 MINOR 3	
74 01	2	F330.1	B8C234* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
74 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
74 03			END OF MAJOR TEST	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A1A(21,23)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
75 00			BRANCH TO MAJOR 75 MINOR 3	
75 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
75 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
75 03	1	T330	TEST 3SB OF MA8C BRANCH TO MAJOR 54 MINOR 1	
75 04			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
76 00			BRANCH TO MAJOR 76 MINOR 3	
76 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
76 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
76 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
77 00			BRANCH TO MAJOR 77 MINOR 3	
77 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
77 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
77 03			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
78 00			BRANCH TO MAJOR 78 MINOR 3	
78 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
78 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
78 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
79 00			BRANCH TO MAJOR 79 MINOR 3	
79 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
79 02				
79 03			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
80 00	2	F332.2	BBC032* S@0	
			INDICATORS | DISPLAY | REPLACE ASSEMBLIES	
			TEST SET FAULT 1210000000001 1A1A1A(21,23)	
			PUNCH TAPE LEADER 12 INCHES LONG	
			BRANCH TO MAJOR 80 MINOR 3	
80 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
80 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
80 03	1	T332	TEST MSB OF MABC	
			PREVIOUS TEST = (54)T331	
			BRANCH TO MAJOR 89 MINOR 2	
80 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
81 00			BRANCH TO MAJOR 81 MINOR 3	
81 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
81 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
81 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
82 00			BRANCH TO MAJOR 82 MINOR 3	
82 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
82 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
82 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
83 00			BRANCH TO MAJOR 83 MINOR 3	
83 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
83 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
83 03			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
84 00			BRANCH TO MAJOR 84 MINOR 3	
84 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
84 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
84 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
85 00			BRANCH TO MAJOR 85 MINOR 3	
85 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
85 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
85 03			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
86 00			BRANCH TO MAJOR 86 MINOR 3	
86 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
86 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
86 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
                ********************************************************************************************************
                *                                                                                                      *
                *                      THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99                   *
                *                                                                                                      *
                ********************************************************************************************************

87 00                           BRANCH TO MAJOR 87 MINOR 3
87 01                           STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
87 02                           STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
87 03                           END OF MAJOR TEST
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
88 00			BRANCH TO MAJOR 88 MINOR 3	
88 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
88 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
88 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
89 00			BRANCH TO MAJOR 89 MINOR 3	
89 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
89 02				
89 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
90 00			BRANCH TO MAJOR 90 MINOR 3	
90 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
90 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
90 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
91 00			BRANCH TO MAJOR 91 MINOR 3	
91 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
91 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
91 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
92 00			BRANCH TO MAJOR 92 MINOR 3	
92 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
92 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
92 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
93 00			BRANCH TO MAJOR 93 MINOR 3	
93 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
93 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
93 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
94 00			BRANCH TO MAJOR 94 MINOR 3	
94 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
94 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
94 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
95 00			BRANCH TO MAJOR 95 MINOR 3	
95 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
95 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
95 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
96 00	2	F337.1	BBC031* INPUT TO MBC061 S01	
			INDICATORS: TEST SET FAULT 1 2 1 0 0 0 0 0 0 0 0 0 0 1 1 A1 A1 A22 — DISPLAY — REPLACE ASSEMBLIES	
			PUNCH TAPE LEADER 12 INCHES LONG	
			BRANCH TO MAJOR 96 MINOR 3	
96 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
96 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
96 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			**********	
			* THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99 *	
			**********	
97 00			BRANCH TO MAJOR 97 MINOR 3	
97 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
97 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
97 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
98 00			BRANCH TO MAJOR 98 MINOR 3	
98 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
98 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
98 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

```
                ********************************************************************************************
                *                                                                                          *
                *                    THIS MAJOR NUMBER ALSO USED FOR TEST/FAULT LOC AFTER MAJOR 99         *
                *                                                                                          *
                ********************************************************************************************

99 00                           BRANCH TO MAJOR 99 MINOR 3
99 01                           STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
99 02                           STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
99 03                           END OF MAJOR TEST
```

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			**********	
			*	
			* MAJOR BRANCH TEST, MSB & 2SB OF MABC - FOLLOWING MAJORS ARE REPEATED:	
			* 17, 57, 87, 97, 99	
			* MAJORS HEX C7, C8, C9 WILL BE DISPLAYED IN MAJOR DISPLAY AS SMALL U7 U8 U9 RESPECTIVELY	
			*	
			**********	
17 00			BRANCH TO MAJOR 17 MINOR 3	
17 01	1	T337	TEST INPUT TO MBC061 FOR S@1 PREVIOUS TEST = (HEX C9)T336 BRANCH TO MAJOR 97 MINOR 2	
17 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
17 03	1	T335	TEST MSB & 2SB OF MABC PREVIOUS TEST = (80)T332 LOAD A REGISTER WITH 002C7 BRANCH TO ADDRESS LOCATION IN A REGISTER	BR ADDR = HEX C7 2
17 04			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
47 00			BRANCH TO MAJOR 3 MINOR 00	
47 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
47 02	2	F335.1	BBC031* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
47 03			END OF MAJOR TEST	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	1A1A1A21

TEST NO.	DIVISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
57 00			BRANCH TO MAJOR 57 MINOR 3	
57 01	2	F336.1	BBC133* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
57 02			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
57 03			END OF MAJOR TEST	

INDICATORS	DISPLAY	REPLACE ASSEMBLIES
NO GO	BLANK	A1A1A1A(21,23)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
87 00	2	F338.1	BBC132* INPUT TO MBC061 S@1	
			INDICATORS: TEST SET FAULT — DISPLAY: 2100000000001 — REPLACE ASSEMBLIES: A1A1A22	
			PUNCH TAPE LEADER 12 INCHES LONG BRANCH TO MAJOR 87 MINOR 3	
87 01			STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
87 02	2	F335.2	BBC132* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO — DISPLAY: BLANK — REPLACE ASSEMBLIES: A1A1A21	
87 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
97 00			BRANCH TO MAJOR 97 MINOR 3	
97 01	2	F336.2	BBC032* S@1 STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
			INDICATORS: NO GO / DISPLAY: BLANK / REPLACE ASSEMBLIES: 1A1A1A1A(21,23)	
97 02	1	T338	TEST INPUT TO MBC061 FOR S@1 PREVIOUS TEST = (2ND 17)T337 LOAD A REGISTER WITH 001C7 BRANCH TO ADDRESS LOCATION IN A REGISTER	BR ADDR = HEX C7 1
97 03			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
99 00				
99 01				
99 02				
99 03				
99 04				
99 05				
99 06				
99 07				
99 08				
99 09				
99 10				
99 11				
99 12				
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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
99 53				
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99 97				
99 98				
99 99	1	T340	END OF TAPE TEST, PREVIOUS TEST = (2ND 97)T338 END OF TAPE FLAG	
			END OF MAJOR TEST	

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE LEADER 12 INCHES LONG	
			PUNCH TAPE CODES - @7 @C	ADDR = HEX C7
99 00			BRANCH TO MAJOR 3 MINOR 00	
99 01			NOT A TEST LOC - BRANCH TO END OF TAPE TEST T340 BRANCH TO MAJOR 99 MINOR 00	BR TO SECOND MAJOR 99
99 02				
99 03			END OF MAJOR TEST	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
			PUNCH TAPE LEADER 12 INCHES LONG	
			PUNCH TAPE CODES - @8 @C	ADDR = HEX C8
99	00		BRANCH TO MAJOR 99 MINOR 3	
99	01		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
99	02		STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON	
99	03		END OF MAJOR TEST	

```
|TEST|DECISION | TEST/FAULT  |                                  SELF-TEST PROGRAM                                  |          REMARKS          |
| NO.|  LEVEL  |   NUMBER   |                                                                                     |                           |

                            PUNCH TAPE LEADER 12 INCHES LONG


                            PUNCH TAPE CODES - @9 @C                                                    ADDR = HEX C9
99 00                       BRANCH TO MAJOR 99 MINOR 3
99 01                       STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON
99 02                       STOP TAPE, DISPLAY C REGISTER, NO-GO LIGHT ON


99 03   1       T336      TEST MSB & 2SB OF MA8C
                          PREVIOUS TEST = (2ND 17)T335
                            BRANCH TO MAJOR 17 MINOR 1

                            PUNCH TAPE LEADER 12 INCHES LONG



          ***************************************************************************************************
          *                                                                                                 *
          *                              MAJOR ADDR = HEX FF => MAJOR DSPL = BLANK                          *
          *  THERE ARE 1023 NOOPS IN THIS MAJOR TO CAUSE PROCEED ERROR IF CONTROL IS LOST IN MAJOR BRANCH TESTS  *
          *                                                                                                 *
          ***************************************************************************************************

                            PUNCH TAPE CODES - @F @F                                                    ADDR = HEX FF
99 00
99 01
99 02
99 03
99 04
99 05
99 06
99 07
99 08
99 09
99 10
99 11
99 12
99 13
99 14
99 15
99 16
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99 19
99 20
99 21
99 22
99 23
99 24
99 25
```

SECTION II. SELF-TEST PROGRAM (CONT)

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
99	26			
99	27			
99	28			
99	29			
99	30			
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99	33			
99	34			
99	35			
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99	76			
99	77			
99	78			
99	79			

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS
99 80			GENERATE NO OPERATION CODE OCTAL 016	
99 81			GENERATE NO OPERATION CODE OCTAL 016	
99 82			GENERATE NO OPERATION CODE OCTAL 016	
99 83			GENERATE NO OPERATION CODE OCTAL 016	
99 84			GENERATE NO OPERATION CODE OCTAL 016	
99 85			GENERATE NO OPERATION CODE OCTAL 016	
99 86			GENERATE NO OPERATION CODE OCTAL 016	
99 87			GENERATE NO OPERATION CODE OCTAL 016	
99 88			GENERATE NO OPERATION CODE OCTAL 016	
99 89			GENERATE NO OPERATION CODE OCTAL 016	
99 90			GENERATE NO OPERATION CODE OCTAL 016	
99 91			GENERATE NO OPERATION CODE OCTAL 016	
99 92			GENERATE NO OPERATION CODE OCTAL 016	
99 93			GENERATE NO OPERATION CODE OCTAL 016	
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TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

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SECTION II. SELF-TEST PROGRAM (CONT)

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			GENERATE NO OPERATION CODE OCTAL 016	
			GENERATE NO OPERATION CODE OCTAL 016	
			PUNCH TAPE CODES - 20 70 F8 20 20 20 20 20 20 70 88 F8 00 F8 40 20	
			10 F8 00 88 A8 F8 00	TRAILER
			PUNCH TAPE LEADER 12 INCHES LONG	

TEST NO.	DECISION LEVEL	TEST/FAULT NUMBER	SELF-TEST PROGRAM	REMARKS

JOB RUN ON NCCITS FAULT ISOLATION COMPILER - E
JOB DATE: 02/18/71

By Order of the Secretary of the Army:

W. C. WESTMORELAND,
General, United States Army,
Chief of Staff.

Official:

VERNE L. BOWERS,
Major General, United States Army,
The Adjutant General.

Distribution:

To be distributed in accordance with DA Form 12-31, Direct and General Support maintenance requirements for OV-1D and U-21 aircrafts.

CHAPTER 5

FINAL ILLUSTRATIONS

This chapter contains the color code diagram for MIL-STD resistors and capacitors and all foldout illustrations referenced in previous chapters.

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Figure 5-2 NOT USED

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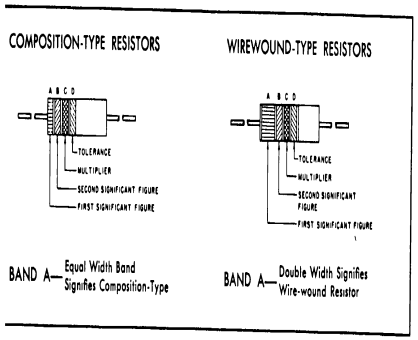
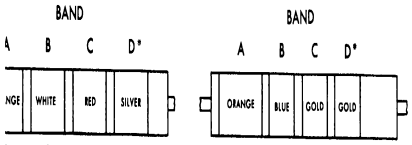
COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



COLOR CODE TABLE

BAND A		BAND B		BAND C		BAND D*	
OR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
CK	0	BLACK	0	BLACK	1		
WN	1	BROWN	1	BROWN	10		
D	2	RED	2	RED	100		
NGE	3	ORANGE	3	ORANGE	1,000		
OW	4	YELLOW	4	YELLOW	10,000	SILVER	± 10
EN	5	GREEN	5	GREEN	100,000	GOLD	± 5
UE	6	BLUE	6	BLUE	1,000,000		
PLE LET)	7	PURPLE (VIOLET)	7				
AY	8	GRAY	8	SILVER	0 01		
ITE	9	WHITE	9	GOLD	0 1		

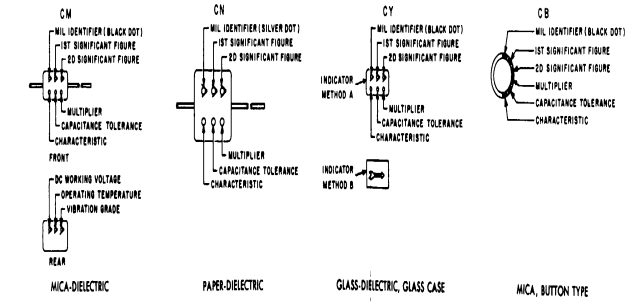
EXAMPLES OF COLOR CODING



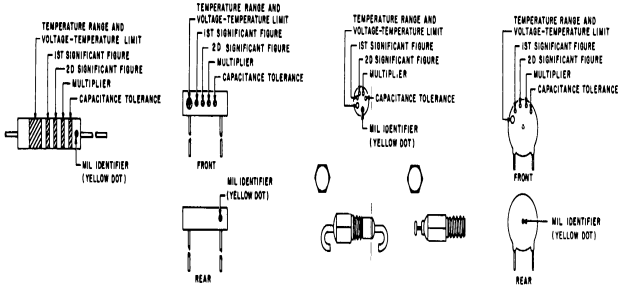
D is omitted, the resistor tolerance is ±20%, and the resistor is not Mil-Std.

COLOR CODE TABLES

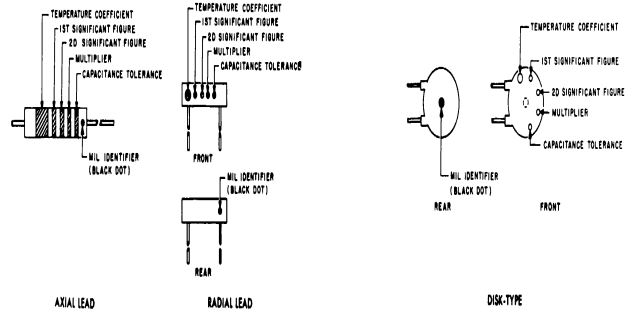
TABLE I - For use with Group I, Styles, CM, CN, CY and CB



GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK



GROUP III Capacitors, Fixed, Ceramic-Dielectric (Temperature Compensating) Style CC



COLOR CODE TABLES

TABLE I – For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM, CY CB	0	0	1			± 20%	± 20%		A				−55° to +70°C	10–55 cps
BROWN		1	1	10					B	E		B			
RED		2	2	100	± 2%		± 2%	± 2%	C		C			−55° to +85°C	
ORANGE		3	3	1,000		± 30%			D			D	300		
YELLOW		4	4	10,000					E					−55° to +125°C	10–2,000 cps
GREEN		5	5		± 5%				F				500		
BLUE		6	6											−55° to +150°C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0 1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

TABLE II For use with Group II, General Purpose, Style CK

COLOR	TEMP. RANGE AND VOLTAGE – TEMP LIMITS[3]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20%	
BROWN	AW	1	1	10	± 10%	
RED	AX	2	2	100		
ORANGE	BX	3	3	1,000		
YELLOW	AV	4	4	10,000		CK
GREEN	CZ	5	5			
BLUE	BV	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III - For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	−30	1	1	10	± 1%		
RED	−80	2	2	100	± 2%	± 0.25uuf	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5%	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0 01			
WHITE		9	9	0 1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.
2. Letters indicate the Characteristics designated in applicable specifications MIL-C-5, MIL-C-91, MIL-C-11272, and MIL-C-10950 respectively
3. Letters indicate the temperature range and voltage-temperature limits designated in MIL-C-11015
4. Temperature coefficient in parts per million per degree centigrade

Figure 5-1. MIL STD resistor and capacitor color code markings.

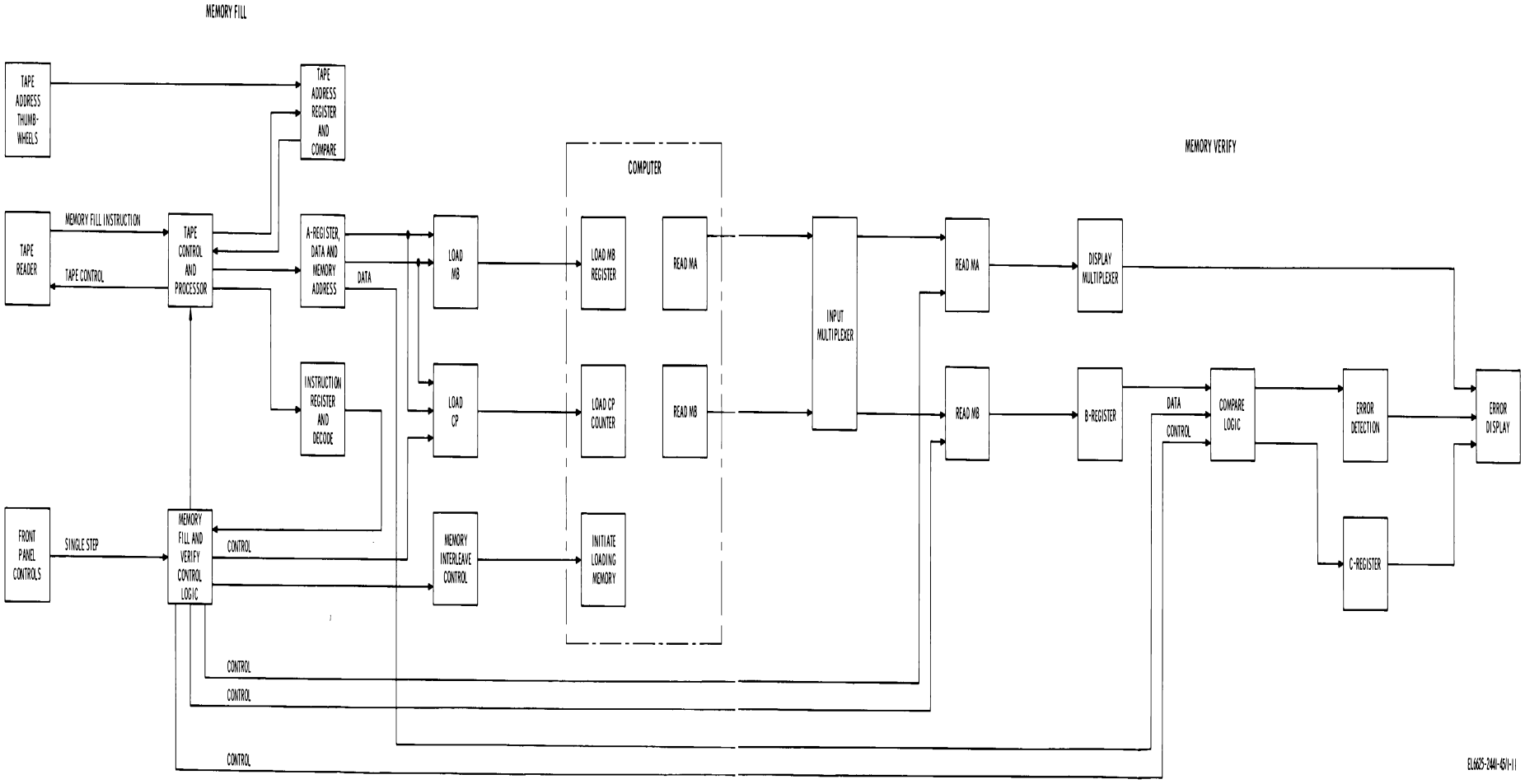


Figure 5-3. Memory fill and verify, block diagram.

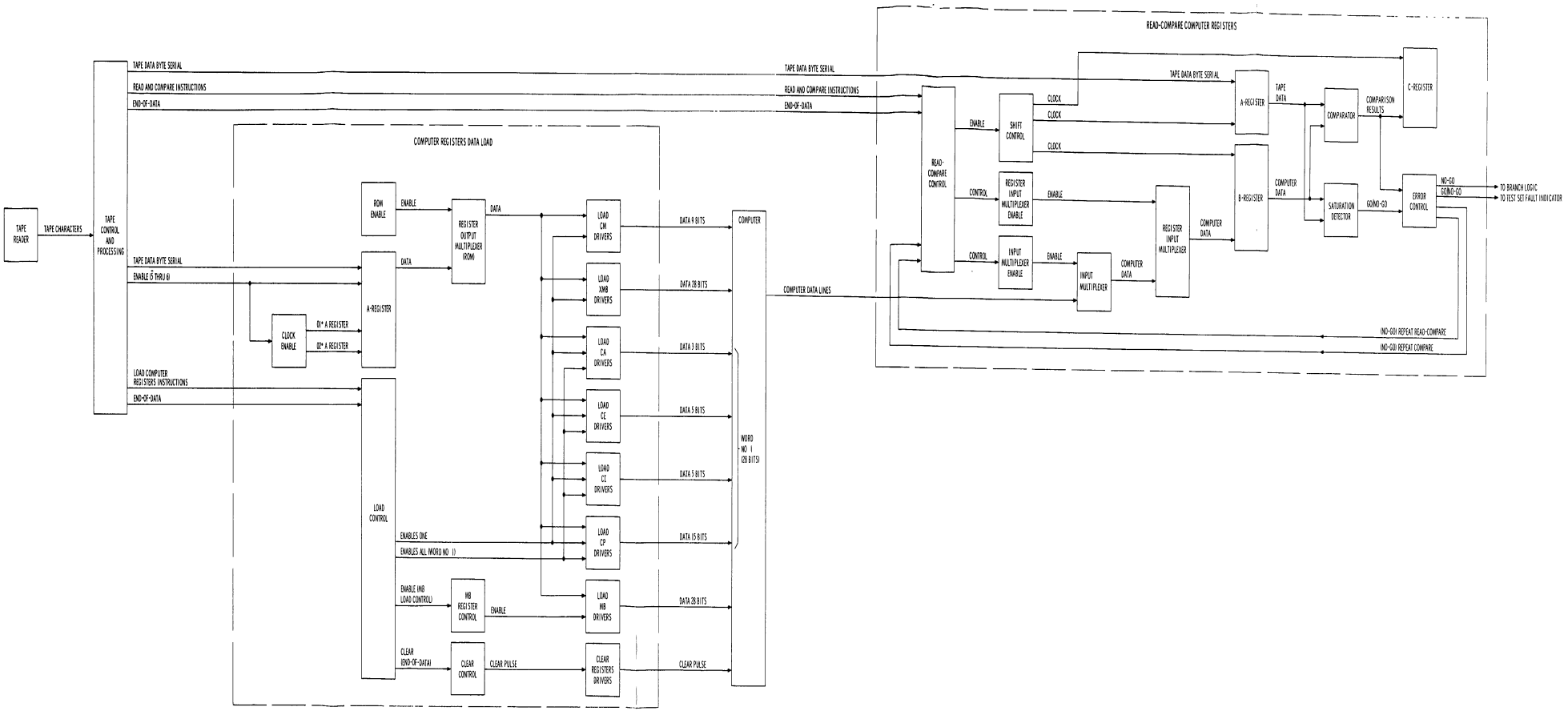


Figure 5-4. Load and read-compare, functional block diagram.

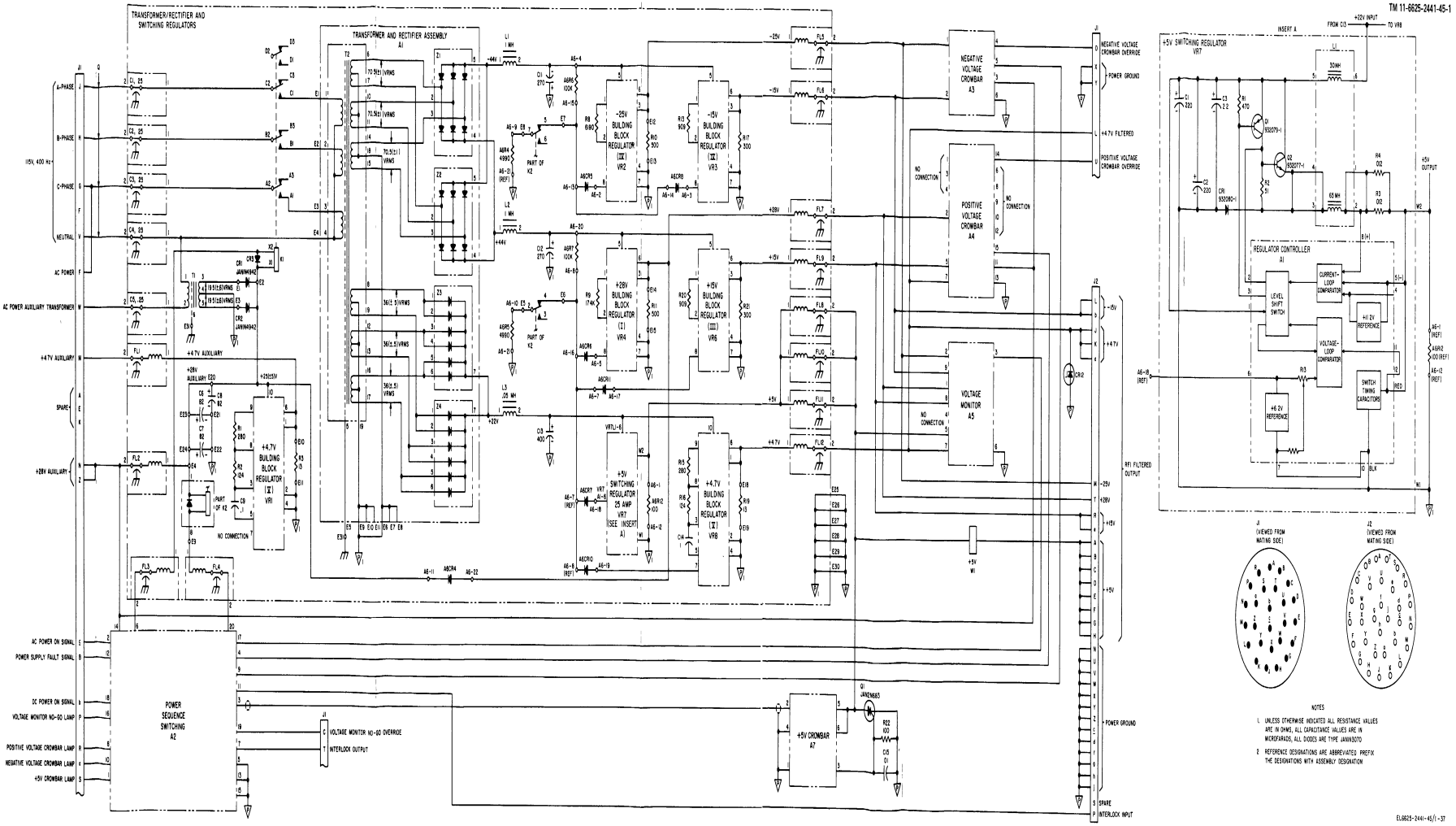


Figure 5-5. Power supply 2A1PS1, functional schematic diagram

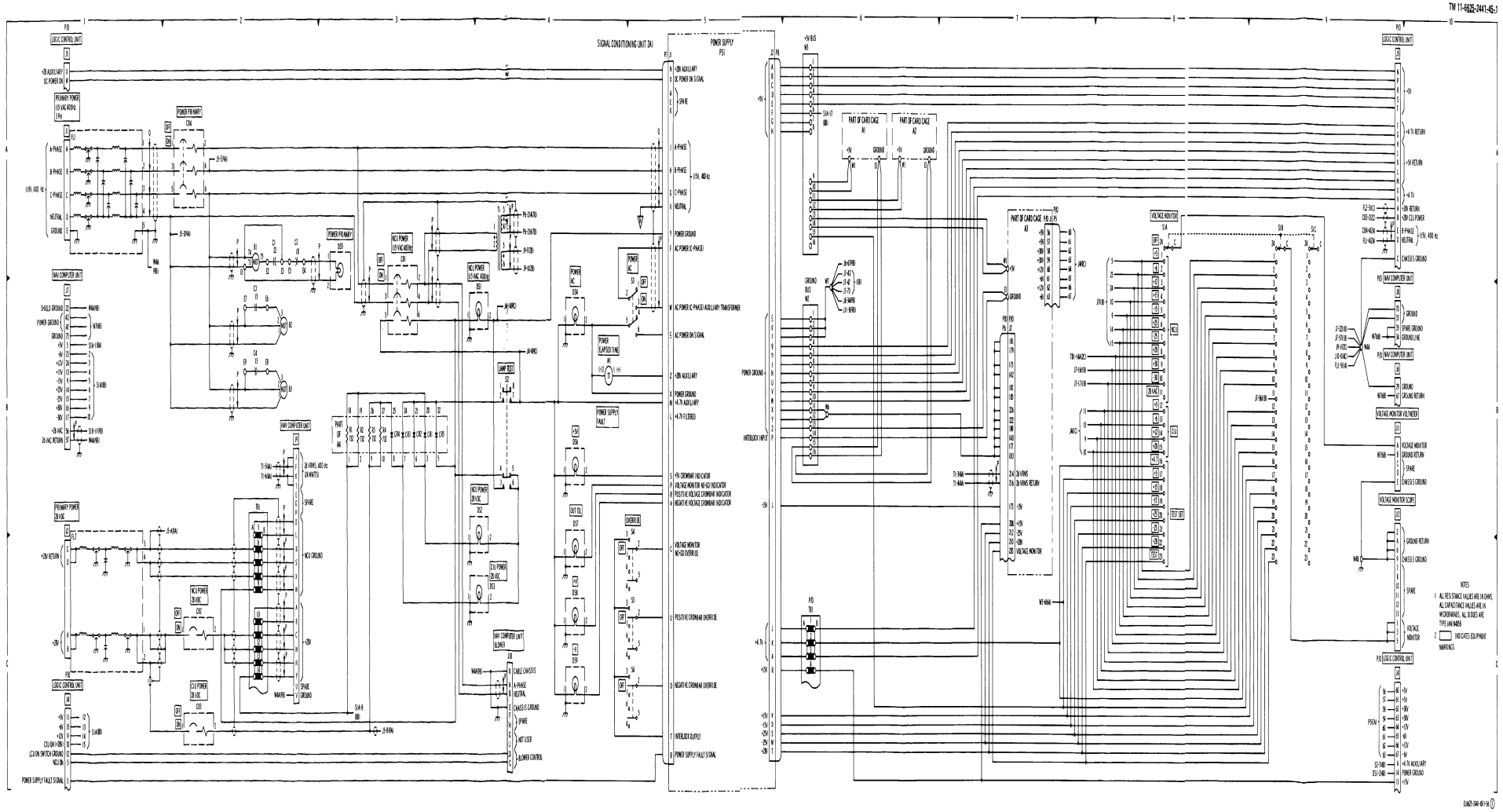


Figure 5-6 ①. Power control and distribution, functional schematic diagram (part 1 of 2)

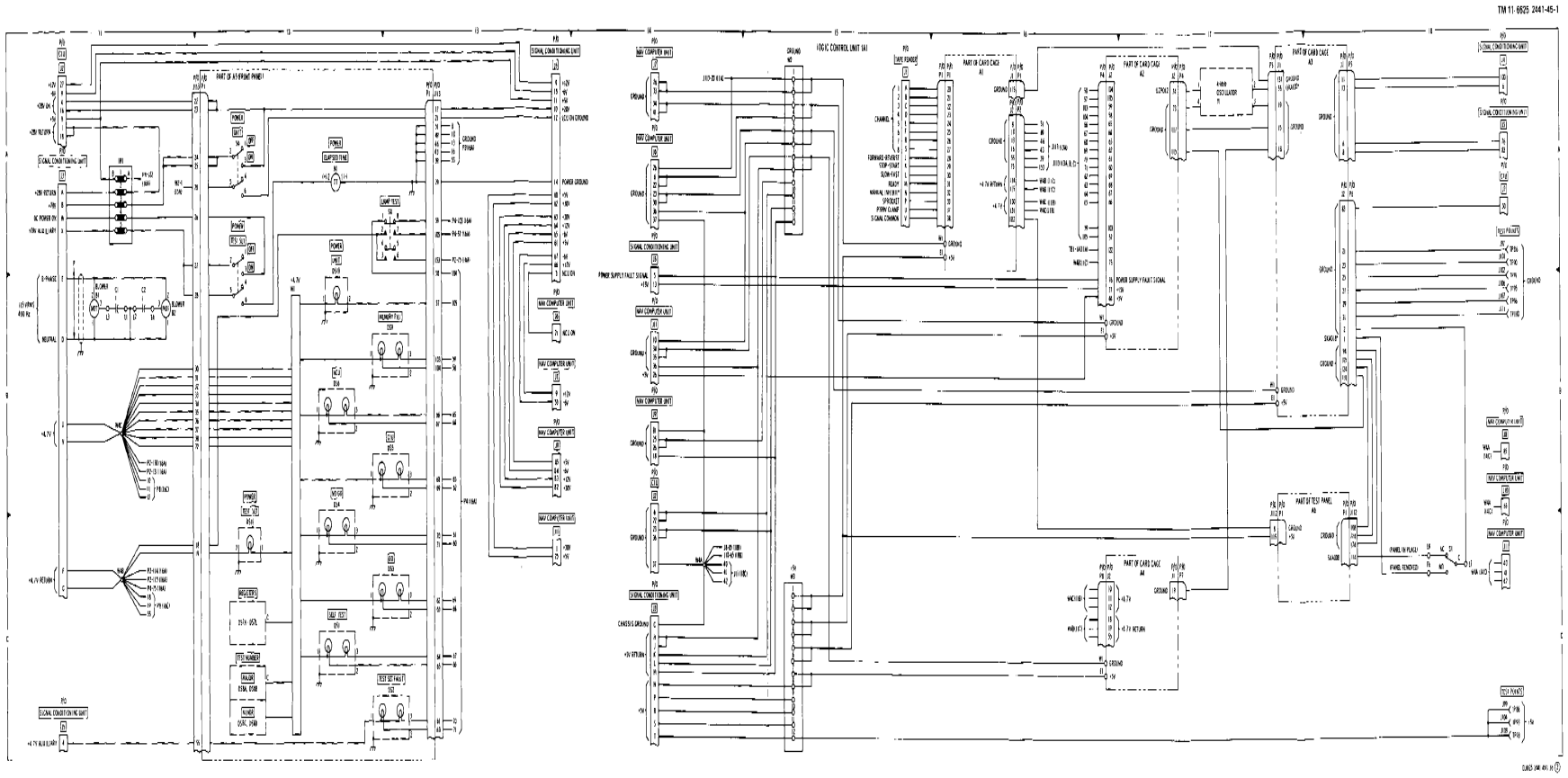


Figure 5-6 ②. Power control and distribution, functional schematic diagram (part 2 of 2).

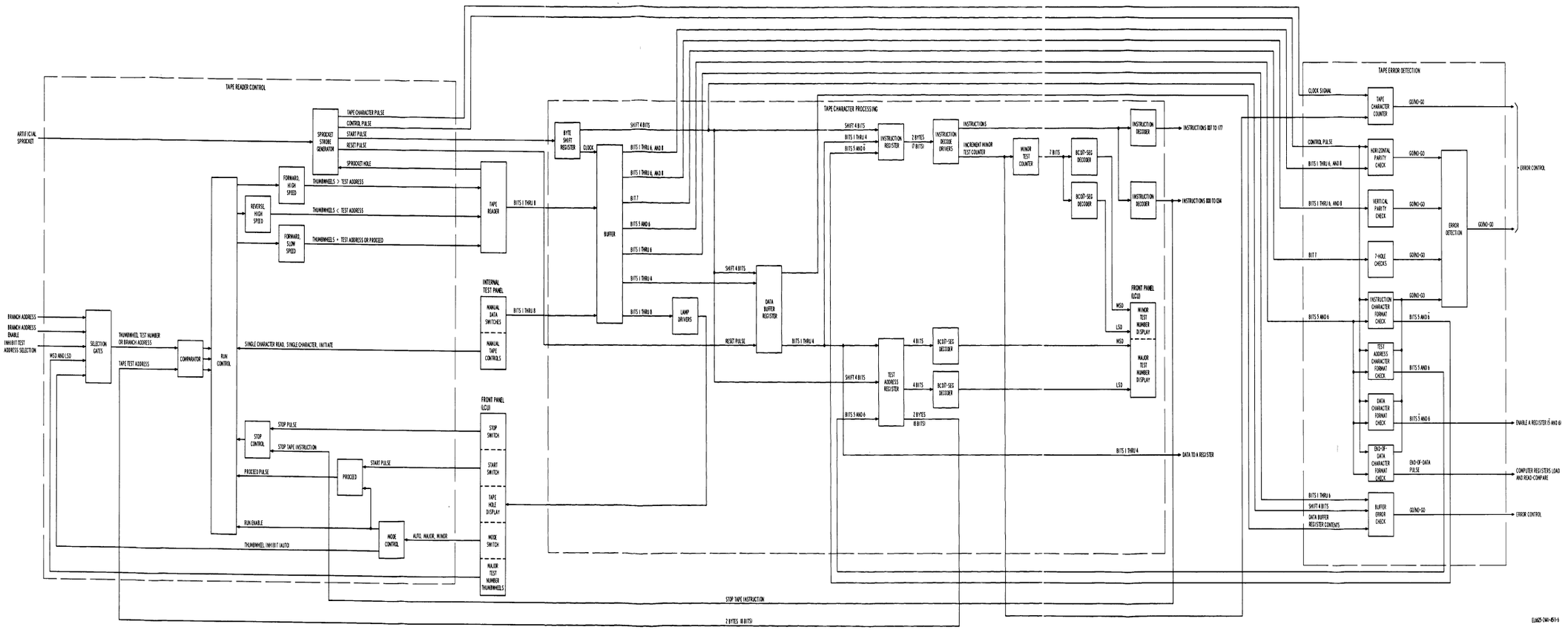


Figure 5-7. Tape control and processing, functional block diagram.

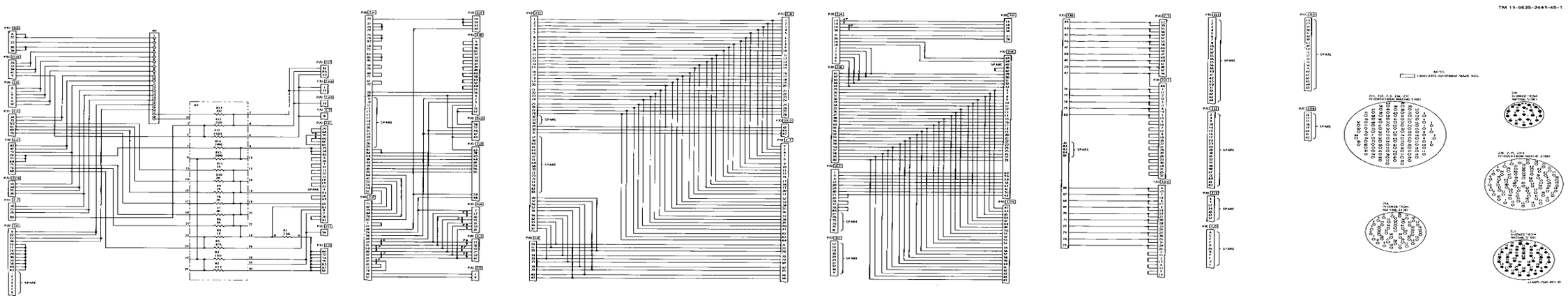


Figure 5-8. Adapter, Self Test MX-386 schematic diagram.

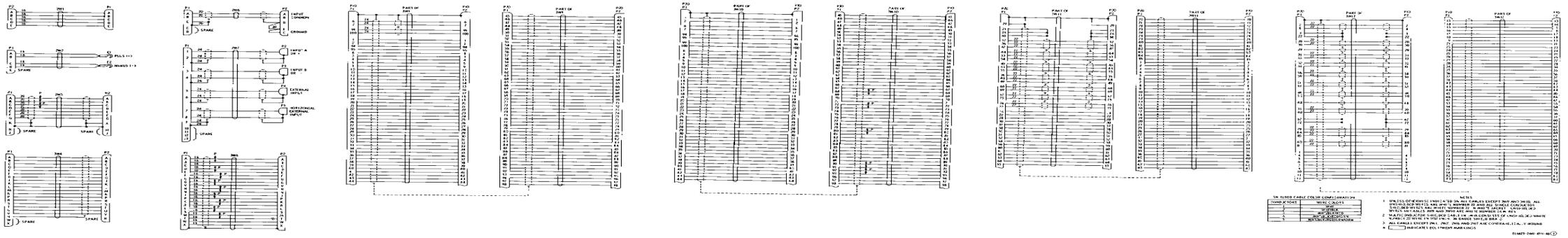


Figure 5-9 ①. Special purpose electrical cable assembly schematic diagram (part 1 of 3).

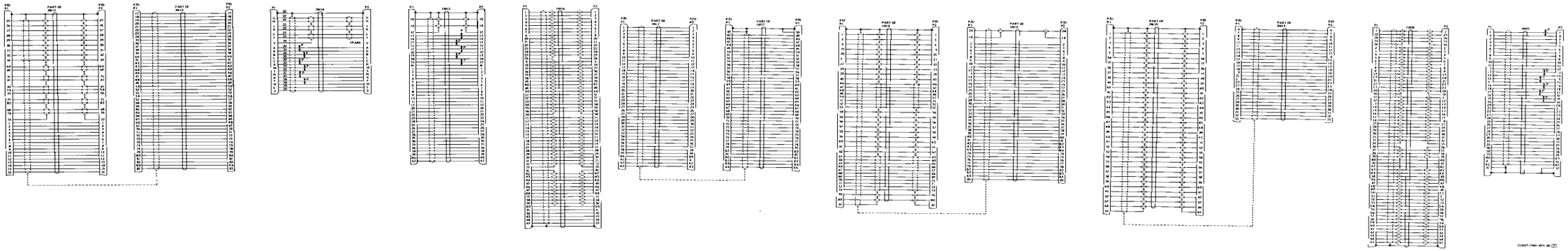


Figure 5-9 (2). Special purpose electrical cable assembly, schematic diagram (part 2 of 3).

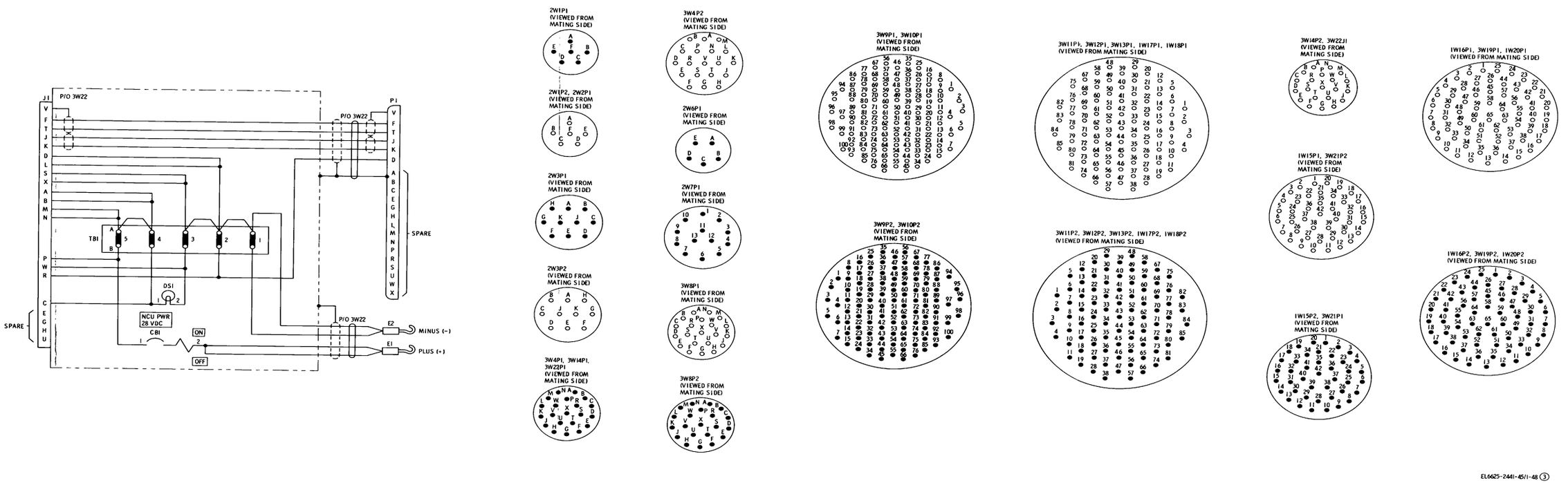


Figure 5-9 ③. Special purpose electrical cable assembly, schematic diagram (part 3 of 3).

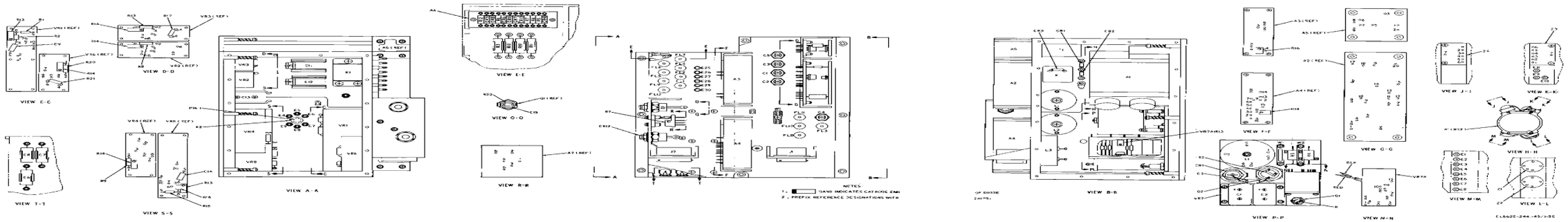


Figure 5-10. Power supply 2A1PS1, parts location diagram.